

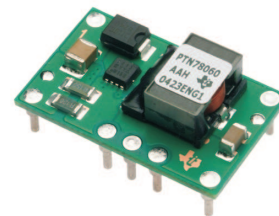
## 15-W, WIDE-INPUT ADJUSTABLE POSITIVE-TO-NEGATIVE VOLTAGE REGULATOR MODULE

### FEATURES

- Up to 3-A Output Current
- Wide-Input Voltage (9 V to 29 V)
- Wide-Output Voltage Adjust (–15 V to –3 V)
- High Efficiency (Up to 88%)
- Undervoltage Lockout
- Output Current Limit
- Overtemperature Shutdown
- Operating Temperature: –40°C to 85°C
- Surface-Mount Package Available

### APPLICATIONS

- General-Purpose, Industrial Controls, HVAC Systems
- Test and Measurement, Medical Instrumentation
- AC/DC Adaptors, Vehicles, Marine, and Avionics

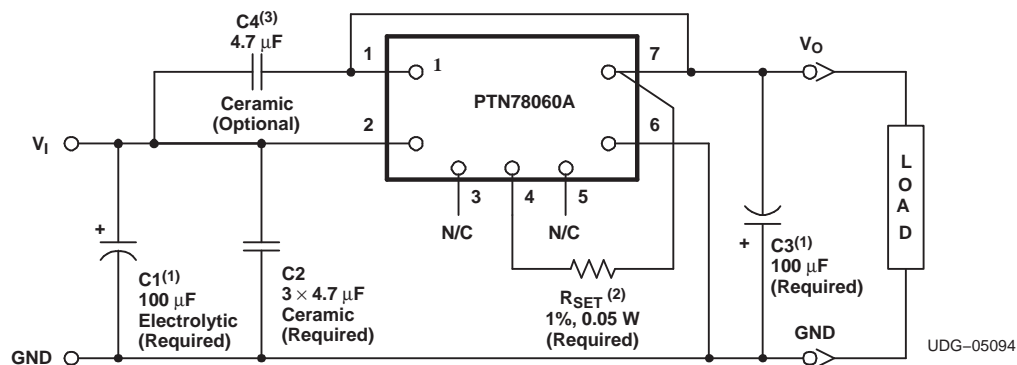


### DESCRIPTION

The PTN78060A is a series of high-efficiency, buck-boost, integrated switching regulators (ISR), that represent the third generation in the evolution of the (PT)78NR100 series of products. In new designs, the PTN78060A series should also be considered in place of the PT6640 series of single in-line pin (SIP) products. In all cases, the PTN78060A has either similar or improved electrical performance characteristics. The caseless, double-sided package has excellent thermal characteristics, and is compatible with TI's roadmap for RoHS and lead-free compliance.

Operating from a wide-input voltage range of 9 V to 29 V, the PTN78060A provides high-efficiency, positive-to-negative voltage conversion for loads of up to 3 A. The output voltage can be set to any value over a wide adjustment range using a single external resistor. The adjust range is –15 V to –3 V.

The PTN78060A is suited to a wide variety of general-purpose industrial applications that operate off 12-V, 24-V, or tightly regulated 28-V dc power.



- (1) See the *Application Information* section for capacitor recommendations
- (2)  $R_{SET}$  is required to adjust the output voltage lower than –3 V. See the *Application Information* section for values.
- (3) For reduced  $V_O$  ripple and noise, a ceramic capacitor is suggested.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

over operating free-air temperature range unless otherwise noted  
all voltages with respect to GND

			UNIT
T <sub>A</sub>	Operating free-air temperature	Over V <sub>I</sub> range	–40°C to 85°C
	Wave solder temperature	Surface temperature of module body or pins (5 seconds)	Horizontal TH (suffix AH) 260°C
	Solder reflow temperature	Surface temperature of module body or pins	Horizontal SMD (suffix AS) 235°C Horizontal SMD (suffix AZ) 260°C
T <sub>stg</sub>	Storage temperature		–40°C to 125°C
P <sub>O</sub>	Output power	V <sub>O</sub>   ≥ 5 V	15 W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V <sub>I</sub>	Input voltage	9	32 -  V <sub>O</sub>	V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

## PACKAGE SPECIFICATIONS

PTN78060x (Suffix AH, AS, and AZ)			
Weight			3.9 grams
Flammability	Meets UL 94 V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, ½ sine, mounted		500 G <sup>(1)</sup>
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Horizontal T/H (suffix AH)	20 G <sup>(1)</sup>
		Horizontal SMD (suffix AS & AZ)	20 G <sup>(1)</sup>

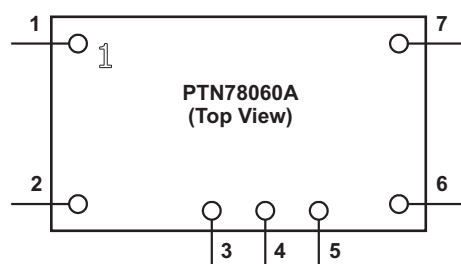
(1) Qualification limit.

## ELECTRICAL CHARACTERISTICS

operating at 25°C free-air temperature,  $V_I = 20\text{ V}$ ,  $V_O = -5\text{ V}$ ,  $I_O = I_O(\text{max})$ ,  $C_1 = 100\text{ }\mu\text{F}$ ,  $C_2 = 3 \times 4.7\text{ }\mu\text{F}$ ,  $C_3 = 100\text{ }\mu\text{F}$ , and  $C_4 = 4.7\text{ }\mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_O$	Output current	$T_A = 85^\circ\text{C}$ , natural convection airflow	$V_O = -15\text{ V}$	0.1	1 <sup>(1)</sup>	A
			$V_O = -12\text{ V}$	0.1	1.25 <sup>(1)</sup>	
			$V_O = -5\text{ V}$	0.1	3 <sup>(1)</sup>	
			$V_O = -3.3\text{ V}$	0.1	3 <sup>(1)</sup>	
$V_I$	Input voltage range	Over $I_O$ range	$V_O = -15\text{ V}$	9	17 <sup>(2)</sup>	V
			$V_O = -12\text{ V}$	9	20 <sup>(2)</sup>	
			$V_O = -5\text{ V}$	9	27 <sup>(2)</sup>	
			$V_O = -3.3\text{ V}$	9	28.7 <sup>(2)</sup>	
$V_O$	Set-point voltage tolerance	$T_A = 25^\circ\text{C}$			$\pm 2\%$ <sup>(3)</sup>	
	Temperature variation	$-40^\circ\text{C}$ to $+85^\circ\text{C}$		$\pm 0.5\%$		
	Line regulation	Over $V_I$ range		$\pm 10$		mV
	Load regulation	Over $I_O$ range		$\pm 10$		mV
	Total output voltage variation	Includes set point, line, load $-40 < T_A < 85^\circ\text{C}$			$\pm 3\%$ <sup>(3)</sup>	
$V_O$	Output voltage adjust range	$9\text{ V} \leq V_I \leq (32 -  V_O )\text{ V}$	-15		-3	V
$\eta$	Efficiency	$R_{\text{SET}} = 100\text{ }\Omega$ , $I_O = 1\text{ A}$ , $V_O = -15\text{ V}$		88%		
		$R_{\text{SET}} = 2\text{ k}\Omega$ , $I_O = 1.25\text{ A}$ , $V_O = -12\text{ V}$		87%		
		$R_{\text{SET}} = 28.7\text{ k}\Omega$ , $I_O = 3\text{ A}$ , $V_O = -5\text{ V}$		82%		
		$R_{\text{SET}} = 221\text{ k}\Omega$ , $I_O = 3\text{ A}$ , $V_O = -3.3\text{ V}$		77%		
	Output voltage ripple	20-MHz bandwidth		$2\% V_O$		$V_{(\text{PP})}$
$I_{O(\text{LIM})}$	Current limit threshold	$\Delta V_O = -50\text{ mV}$		5.5		A
	Transient response	1-A/ $\mu\text{s}$ load step from 50% to 100% $I_{O\text{max}}$	Recovery time	200		$\mu\text{s}$
			$V_O$ over/undershoot	2		$\%V_O$
$F_S$	Switching frequency	Over $V_I$ and $I_O$ ranges	440	550	660	kHz
UVLO	Undervoltage lockout	$V_I$ increasing		5.5		V
$C_I$	External input capacitance	Ceramic	14.1 <sup>(4)</sup>			$\mu\text{F}$
		Nonceramic	100 <sup>(4)</sup>			
$C_O$	External output capacitance	Ceramic			200	$\mu\text{F}$
		Nonceramic	100 <sup>(5)</sup>		1000	
		Equivalent series resistance (nonceramic)	14 <sup>(6)</sup>			m $\Omega$
MTBF	Calculated reliability	Per Telcordia SR-332, 50% stress, $T_A = 40^\circ\text{C}$ , ground benign	8.9			$10^6\text{ Hr}$

- (1) The maximum output current is 3 A or a maximum output power of 15 W, whichever is less.
- (2) The maximum input voltage is limited and defined to be  $(32 - |V_O|)$ .
- (3) The set-point voltage tolerance is affected by the tolerance and stability of  $R_{\text{SET}}$ . The stated limit is unconditionally met if  $R_{\text{SET}}$  has a tolerance of 1% with 100 ppm/ $^\circ\text{C}$  or better temperature stability.
- (4) A 100- $\mu\text{F}$  electrolytic capacitor and three 4.7- $\mu\text{F}$  ceramic capacitors are required across the input ( $V_I$  and GND) for proper operation. Locate the ceramic capacitors close to the module.
- (5) 100  $\mu\text{F}$  of output capacitance is required for proper operation. See the application information for further guidance.
- (6) This is the typical ESR for all the electrolytic (nonceramic) capacitance. Use 17 m $\Omega$  as the minimum when using max-ESR values to calculate.

**PIN ASSIGNMENT****TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$V_O$	1, 7	O	The negative output voltage power connection. It is also the reference for the $V_O$ <i>Adjust</i> control input. For proper operation, pins 1 and 7 must be connected.
$V_I$	2	I	The positive input voltage power node to the module, which is referenced to common GND.
N/C	3		This pin is active and must be isolated from any electrical connection.
$V_O$ Adjust	4	I	A 1% resistor must be connected between pin 4 and pin 7 to set the output voltage of the module. The adjust range is $-15\text{ V}$ to $-3\text{ V}$ . If left open-circuit, the output voltage defaults to $-3\text{ V}$ . The temperature stability of the resistor should be $100\text{ ppm}/^{\circ}\text{C}$ (or better). The standard resistor value for a number of common output voltages is provided in the application information.
N/C	5		This pin is active and must be isolated from any electrical connection.
GND	6	I/O	The common ground connection for both $V_I$ and $V_O$ power connections.

# TYPICAL CHARACTERISTICS (9-V INPUT)<sup>(1)(2)</sup>

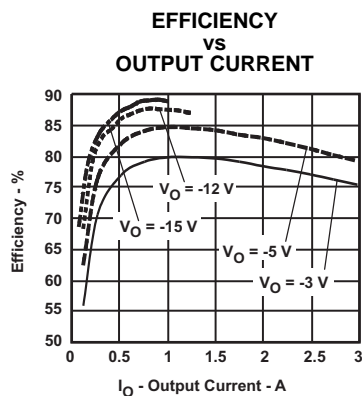


Figure 1.

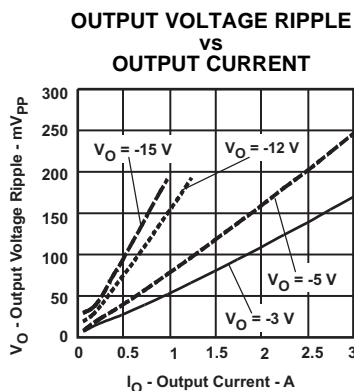


Figure 2.

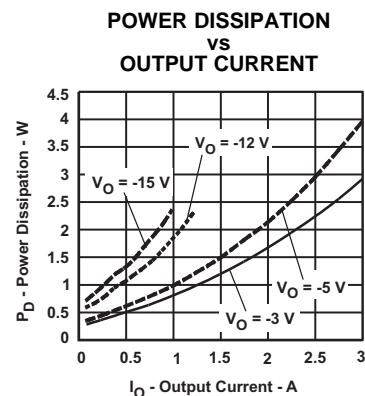


Figure 3.

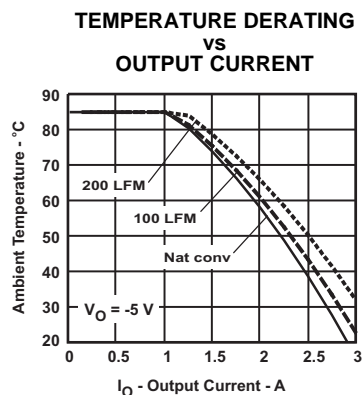


Figure 4.

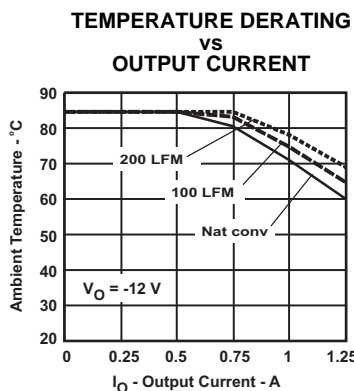


Figure 5.

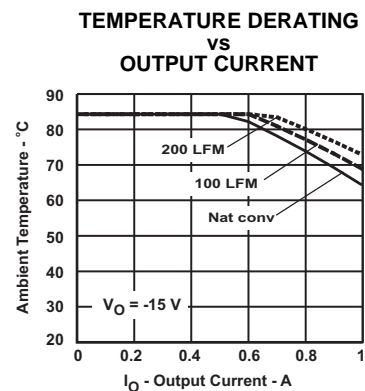


Figure 6.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 1](#), [Figure 2](#), and [Figure 3](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to [Figure 4](#), [Figure 5](#), and [Figure 6](#).

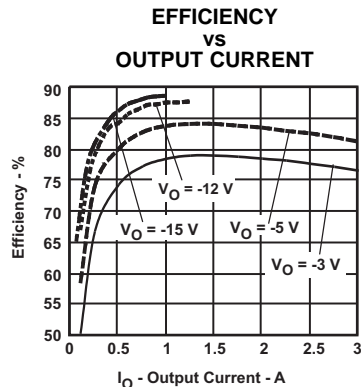
TYPICAL CHARACTERISTICS (12-V INPUT)<sup>(1) (2)</sup>

Figure 7.

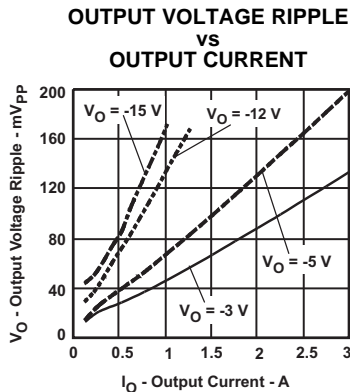


Figure 8.

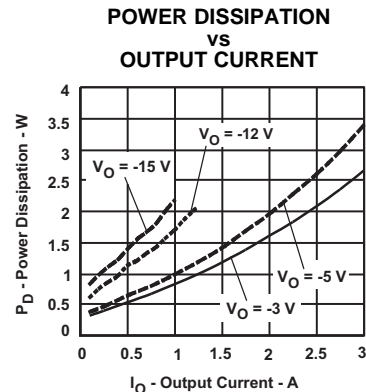


Figure 9.

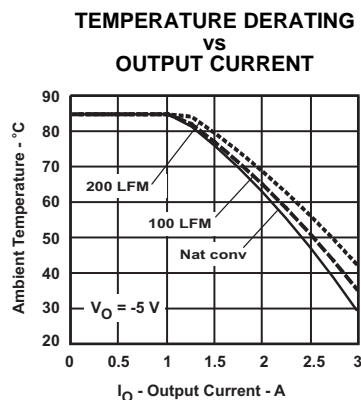


Figure 10.

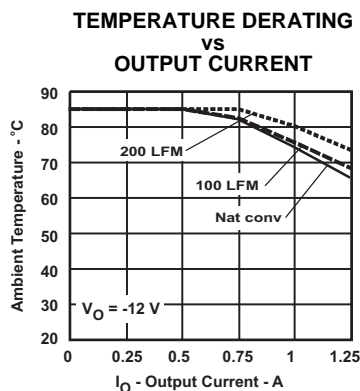


Figure 11.

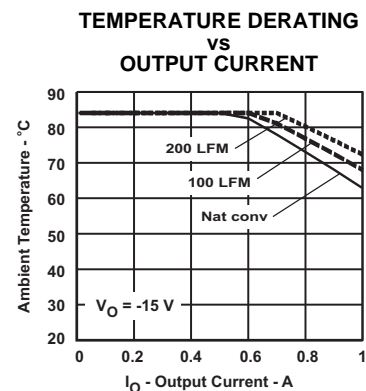


Figure 12.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 7](#), [Figure 8](#), and [Figure 9](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to [Figure 10](#), [Figure 11](#), and [Figure 12](#).

# TYPICAL CHARACTERISTICS (24-V INPUT)<sup>(1) (2)</sup>

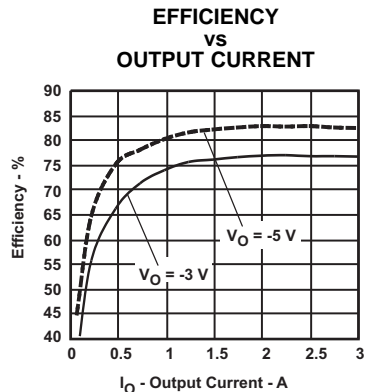


Figure 13.

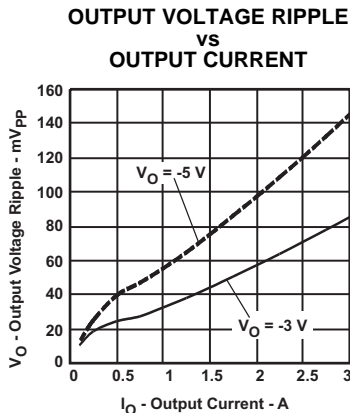


Figure 14.

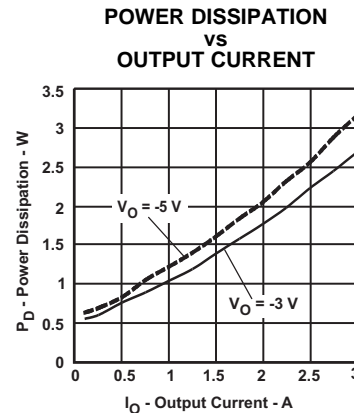


Figure 15.

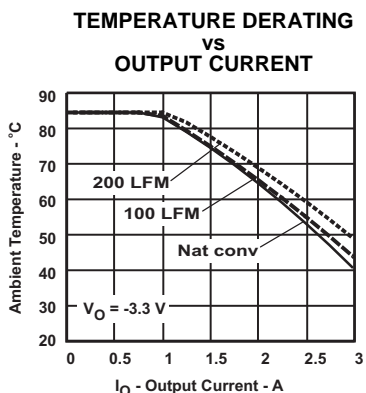


Figure 16.

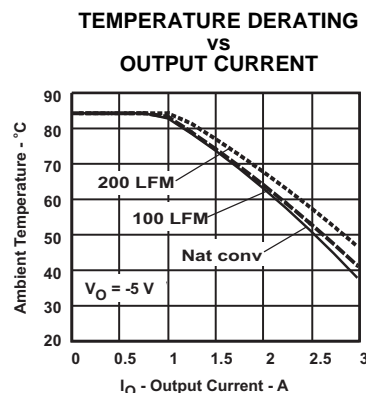


Figure 17.

- (1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to [Figure 13](#), [Figure 14](#), and [Figure 15](#).
- (2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm, double-sided PCB with 2 oz. copper. For surface mount packages (AS and AZ suffix), multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to [Figure 16](#), and [Figure 17](#).

## APPLICATION INFORMATION

### Adjusting the Output Voltage of the PTN78060A Wide-Output Adjust Power Modules

#### General

A resistor must be connected directly between the  $V_O$  *Adjust* control (pin 4) and the output voltage (pin 7) to set the output voltage lower than  $-3$  V. The adjustment range is from  $-15$  V to  $-3$  V. If pin 4 is left open, the output voltage defaults to the highest value,  $-3$  V.

Table 1 gives the standard resistor value for a number of common voltages, and with the actual output voltage that the value produces. For other output voltages, the resistor value can either be calculated using the following formula, or simply selected from the range of values given in Table 2. Figure 18 shows the placement of the required resistor.

$$R_{SET} = 54.9 \text{ k}\Omega \times \frac{1.25 \text{ V}}{|V_O| - 3 \text{ V}} - 5.62 \text{ k}\Omega \quad (1)$$

#### Input Voltage Considerations

The PTN78060A is a buck-boost switching regulator. In order that the output remains in regulation, the input voltage must not exceed the output by a maximum differential voltage.

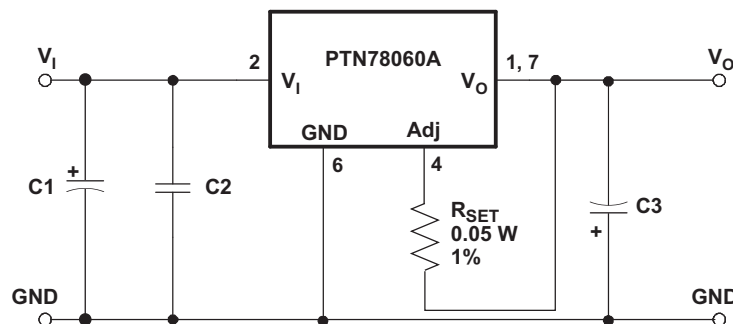
Another consideration is the pulse width modulation (PWM) range of the regulator's internal control circuit. For stable operation, its operating duty cycle should not be lower than some minimum percentage. This defines the maximum advisable ratio between the regulator's input and output voltage magnitudes.

For satisfactory performance, the maximum operating input voltage range must be equal to  $(32 - |V_O|)$  volts.

As an example, Table 1 gives the operating input voltage range for the common output bus voltages. In addition, the Electrical Characteristics define the available output voltage adjust range for various input voltages.

**Table 1. Standard Values of  $R_{SET}$  for Common Output Voltages**

$V_O$ (Required)	$R_{SET}$ (Standard Value)	$V_O$ (Actual)	Operating $V_I$ Range
$-15$ V	$100 \text{ }\Omega$	$-14.997$ V	9 V to 17 V
$-12$ V	$2 \text{ k}\Omega$	$-12.006$ V	9 V to 20 V
$-5$ V	$28.7 \text{ k}\Omega$	$-5.000$ V	9 V to 27 V
$-3.3$ V	$221 \text{ k}\Omega$	$-3.303$ V	9 V to 28.7 V



- (1) A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
- (2) Never connect capacitors from  $V_O$  *Adjust* to either GND or  $V_O$ . Any capacitance added to the  $V_O$  *Adjust* pin affects the stability of the regulator.

**Figure 18.  $V_O$  Adjust Resistor Placement**



**Table 2. Output Voltage Set-Point Resistor Values**

V <sub>O</sub> Required	R <sub>SET</sub>	V <sub>O</sub> Required	R <sub>SET</sub>	V <sub>O</sub> Required	R <sub>SET</sub>
–15.0 V	99 Ω	–11.9 V	2.09 kΩ	–8.8 V	6.21 kΩ
–14.9 V	147 Ω	–11.8 V	2.18 kΩ	–8.6 V	6.63 kΩ
–14.8 V	196 Ω	–11.7 V	2.27 kΩ	–8.4 V	7.09 kΩ
–14.7 V	245 Ω	–11.6 V	2.36 kΩ	–8.2 V	7.58 kΩ
–14.6 V	296 Ω	–11.5 V	2.45 kΩ	–8.0 V	8.11 kΩ
–14.5 V	347 Ω	–11.4 V	2.55 kΩ	–7.8 V	8.68 kΩ
–14.4 V	400 Ω	–11.3 V	2.65 kΩ	–7.6 V	9.30 kΩ
–14.3 V	453 Ω	–11.2 V	2.75 kΩ	–7.4 V	9.98 kΩ
–14.2 V	507 Ω	–11.1 V	2.82 kΩ	–7.2 V	10.7 kΩ
–14.1 V	562 Ω	–11.0 V	2.96 kΩ	–7.0 V	11.5 kΩ
–14.0 V	619 Ω	–10.9 V	3.07 kΩ	–6.8 V	12.4 kΩ
–13.9 V	676 Ω	–10.8 V	3.18 kΩ	–6.6 V	13.4 kΩ
–13.8 V	734 Ω	–10.7 V	3.29 kΩ	–6.4 V	14.6 kΩ
–13.7 V	794 Ω	–10.6 V	3.41 kΩ	–6.2 V	15.8 kΩ
–13.6 V	854 Ω	–10.5 V	3.53 kΩ	–6.0 V	17.3 kΩ
–13.5 V	916 Ω	–10.4 V	3.65 kΩ	–5.8 V	18.9 kΩ
–13.4 V	979 Ω	–10.3 V	3.78 kΩ	–5.6 V	20.7 kΩ
–13.3 V	1.04 kΩ	–10.2 V	3.91 kΩ	–5.4 V	22.9 kΩ
–13.2 V	1.11 kΩ	–10.1 V	4.04 kΩ	–5.2 V	25.6 kΩ
–13.1 V	1.18 kΩ	–10.0 V	4.18 kΩ	–5.0 V	28.7 kΩ
–13.0 V	1.24 kΩ	–9.9 V	4.33 kΩ	–4.8 V	32.5 kΩ
–12.9 V	1.31 kΩ	–9.8 V	4.47 kΩ	–4.6 V	37.2 kΩ
–12.8 V	1.38 kΩ	–9.7 V	4.62 kΩ	–4.4 V	43.4 kΩ
–12.7 V	1.46 kΩ	–9.6 V	4.78 kΩ	–4.2 V	51.6 kΩ
–12.6 V	1.52 kΩ	–9.5 V	4.94 kΩ	–4.0 V	63.0 kΩ
–12.5 V	1.60 kΩ	–9.4 V	5.10 kΩ	–3.8 V	80.1 kΩ
–12.4 V	1.68 kΩ	–9.3 V	5.27 kΩ	–3.6 V	109 kΩ
–12.3 V	1.76 kΩ	–9.2 V	5.45 kΩ	–3.4 V	166 kΩ
–12.2 V	1.84 kΩ	–9.1 V	5.63 kΩ	–3.2 V	338 kΩ
–12.1 V	1.92 kΩ	–9.0 V	5.82 kΩ	–3.0 V	OPEN
–12.0 V	2.01 kΩ	–8.9 V	6.01 kΩ		

## CAPACITOR RECOMMENDATIONS FOR THE PTN78060 WIDE-OUTPUT ADJUST POWER MODULES

### Input Capacitor

The minimum requirement for the input bus is 100  $\mu\text{F}$  of nonceramic capacitance and 14.1  $\mu\text{F}$  ( $3 \times 4.7 \mu\text{F}$ ) of ceramic capacitance, in either an X5R or X7R temperature characteristic. Ceramic capacitors should be located within 0.5 inch (1.27 cm) of the regulator's input pins. Electrolytic capacitors can be used at the input, but only in addition to the required ceramic capacitance. The minimum ripple current rating for any nonceramic capacitance must be 350 mA rms. The ripple current rating of electrolytic capacitors is a major consideration when they are used at the input. This ripple current requirement can be reduced by placing more ceramic capacitors at the input, in addition to the minimum required 14.1  $\mu\text{F}$ .

Tantalum capacitors are not recommended for use at the input bus, as none were found to meet the minimum voltage rating of  $2 \times$  (maximum dc voltage + ac ripple). The  $2 \times$  rating is standard practice for regular tantalum capacitors to ensure reliability. Polymer-tantalum capacitors are more reliable, and are available with a maximum rating of typically 20 V. These can be used with input voltages up to 16 V.

### Output Capacitor

The minimum capacitance required to ensure stability is a 100- $\mu\text{F}$  capacitor. Either ceramic or electrolytic-type capacitors can be used. The minimum ripple current rating for the nonceramic capacitance must be at least 200 mA rms. The stability of the module and voltage tolerances is compromised if the capacitor is not placed near the output bus pins. A high-quality, computer-grade electrolytic capacitor should be adequate. A ceramic capacitor can also be located within 0.5 inch (1.27 cm) of the output pin.

For applications with load transients (sudden changes in load current), the regulator response improves with additional capacitance. Additional electrolytic capacitors should be located close to the load circuit. These capacitors provide decoupling over the frequency range, 2 kHz to 150 kHz. Aluminum electrolytic capacitors are suitable for ambient temperatures above 0°C. For operation below 0°C, tantalum or Os-Con-type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 10 m $\Omega$  (17 m $\Omega$  using the manufacturer's maximum ESR for a single capacitor). A list of recommended capacitors and vendors are identified in [Table 3](#).

### Ceramic Capacitors

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further reduce the reflected input ripple current, or improve the output transient response, multilayer ceramic capacitors must be added. Ceramic capacitors have low ESR, and their resonant frequency is higher than the bandwidth of the regulator. When placed at the output, their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 200  $\mu\text{F}$ .

### Tantalum Capacitors

Tantalum-type capacitors may be used at the output and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/T510/T520 capacitors series are suggested over many other tantalum types due to their rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation, and lower ripple current capability. These capacitors are also less reliable as they have lower power dissipation and surge current ratings. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer-tantalum capacitors for the output, the minimum ESR limit is encountered well before the maximum capacitance value is reached.

### Capacitor Table

The capacitor table, [Table 3](#), identifies the characteristics of capacitors from vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type. This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The rms rating and ESR (at 100 kHz) are critical parameters necessary to ensure both optimum regulator performance and long capacitor life.

## Designing for Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a  $di/dt$  of 1 A/ $\mu$ s. The typical voltage deviation for this load transient is given in the data sheet specification table using the required value of output capacitance. As the  $di/dt$  of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation of any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher  $di/dt$  or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases, special attention must be paid to the type, value, and ESR of the capacitors selected.

If the transient performance requirements exceed those specified in the data sheet, the selection of output capacitors becomes more important. Review the minimum ESR in the characteristic data sheet for details on the capacitance maximum.

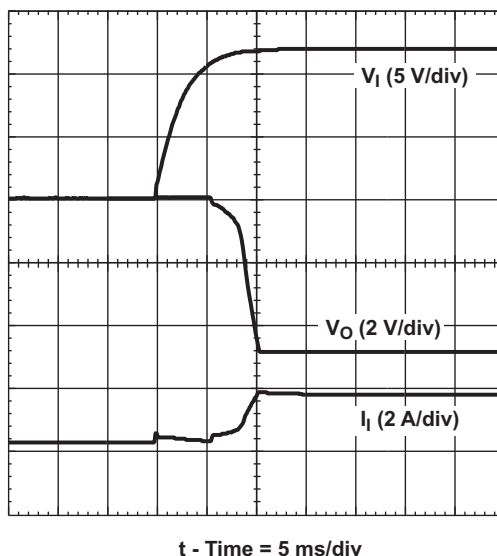
**Table 3. Recommended Input/Output Capacitors**

CAPACITOR VENDOR/ COMPONENT SERIES	CAPACITOR CHARACTERISTICS					QUANTITY		VENDOR NUMBER
	WORKING VOLTAGE (V)	VALUE ( $\mu$ F)	EQUIVALENT SERIES RESISTANCE (ESR) ( $\Omega$ )	85°C MAXIMUM RIPPLE CURRENT ( $I_{RMS}$ ) (mA)	PHYSICAL SIZE (mm)	INPUT BUS	OUTPUT BUS	
FC( Radial)	35	100	0.117	555	8 x 11,5	$\geq 1$	1	EEUFC1V01
FC (SMD)	35	100	0.015	670	10 x10,2	$\geq 1$	1	EEVFC1V101P
United Chemi-Con PXA (SMD)	16	180	0.016	4360	8 x 12	$\geq 1$ <sup>(1)</sup>	$\leq 1$	PXA16VC180MF60 ( $V_i$ , $ V_o  < 14$ V)
PS	25	100	0.020	4300	10 x 12,5	$\geq 1$ <sup>(1)</sup>	$\leq 1$	10PS100MJ12 ( $V_i < 22$ V)
LXZ	50	100	0.22	485	8 x 12,5	$\geq 1$ <sup>(1)</sup>	1	LXZ50VB101M8X12LL
MVY(SMD)	50	100	0.300	500	10 x 10	$\geq 1$	1	MVY50VC101M10X10TP
Nichicon UWG (SMD)	50	100	0.300	500	10 x 10	$\geq 1$	1	UWG1H101MNR1GS
F550 (Tantalum)	10	100	0.055	2000	7,7 x 4,3	N/R <sup>(1)</sup>	$\leq 3$ <sup>(2)</sup>	F551A107MN ( $ V_o  \leq 5$ V)
HD	50	120	0.072	979	10 x12,5	$\geq 1$	1	UHD1H151MHR
Sanyo Os-Con SVP (SMD)	20	100	0.024	2500	8 x 12	$\geq 1$ <sup>(1)</sup>	$\leq 1$	20SVP100M ( $V_i \leq 16$ V)
SP	16	100	0.032	2890	10 x 5	$\geq 1$ <sup>(1)</sup>	$\leq 1$	16SP100M ( $V_i$ , $ V_o  \leq 14$ V)
AVX Tantalum TPS (SMD)	20	100	0.085	1543	7,3 L x 4,3 W x 4,1 H	N/R <sup>(3)</sup>	$\leq 3$	TPSV107M020R0085 ( $ V_o  \leq 10$ V)
	20	100	0.200	> 817		N/R <sup>(3)</sup>	$\leq 3$	TPSE107M020R0200 ( $ V_o  \leq 10$ V)
Murata X5R Ceramic	16	47	0.002	>1000	3225	$\geq 3$ <sup>(1)</sup>	$\leq 3$	GRM32ER61C476M ( $V_i$ , $ V_o  \leq 13.5$ V)
Murata X5R Ceramic	6.3	47	0.002	>1000	3225	N/R <sup>(1)</sup>	$\leq 3$	GRM42-2X5R476M6.3 ( $ V_o  \leq 5.5$ V)
TDK X7R Ceramic	25	2.2	0.002	>1000	3225	$\geq 6$ <sup>(4)</sup>	1	C3225X7R1E225KT/MT ( $V_i \leq 20$ V)
Murata X7R Ceramic	25	2.2	0.002	>1000	3225	$\geq 6$ <sup>(4)</sup>	1	GRM32RR71E225K ( $V_i \leq 20$ V)
Kemet X7R Ceramic	25	2.2	0.002	>1000	3225	$\geq 6$ <sup>(4)</sup>	1	C1210C225K3RAC ( $V_i \leq 20$ V)
AVX X7R Ceramic	25	2.2	0.002	>1000	3225	$\geq 6$ <sup>(4)</sup>	1	C12103C225KAT2A ( $V_i \leq 20$ V)
Murata X7R Ceramic	50	4.7	0.002	>1000	3225	$\geq 3$	1	GRM32ER71H475KA88L
TDK X7R Ceramic	50	2.2	0.002	>1000	3225	$\geq 6$	1	C3225X7R1H225KT
Murata Radial Through-hole	50	2.2	0.004	>1000	10 H x 10 W x 4 D	$\geq 6$	1	RPER71H2R2KK6F03

- (1) The voltage rating of the input capacitor must be selected for the desired operating input voltage range of the regulator. To operate the regulator at a higher input voltage, select a capacitor with the next higher voltage rating.
- (2) The maximum voltage rating of the capacitor must be selected for the desired set-point voltage ( $V_o$ ). To operate at a higher output voltage, select a capacitor with a higher voltage rating.
- (3) Not recommended (N/R). The voltage rating does not meet the minimum operating limits in most applications.
- (4) The maximum rating of the ceramic capacitor limits the regulator's operating input voltage to 20 V. Select an alternative ceramic component to operate at a higher input voltage.

## Power-Up Characteristics

When configured per the standard application, the PTN78060A power module produces a regulated output voltage following the application of a valid input source voltage. During power up, internal soft-start circuitry slows the rate that the output voltage rises, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry introduces a short time delay (typically 5 ms – 10 ms) into the power-up characteristic. This is from the point that a valid input source is recognized. Figure 19 shows the power-up waveforms when operating from a 12-V input and with the output voltage adjusted to –5-V. The waveforms were measured with a 2.8-A resistive load.



**Figure 19. Power-Up Waveforms**

## Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the module from attempting to power up until the input voltage is above the UVLO threshold. This is to prevent the module from drawing excessive current from the input source at power up. Below the UVLO threshold, the module is held off.

## Current Limit Protection

The module is protected against load faults with a continuous current limit characteristic. Under a load-fault condition, the output current increases to the current limit threshold. Attempting to draw current that exceeds the current limit threshold causes the module to progressively reduce its output voltage. Current is continuously supplied to the fault until the fault is removed. Once it is removed, the output voltage promptly recovers. When limiting output current, the regulator experiences higher power dissipation, which increases its temperature. If the temperature increase is excessive, the module's overtemperature protection begins to periodically turn the output voltage off.

## Overtemperature Protection

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in temperature may be the result of a drop in airflow, a high ambient temperature, or a sustained current limit condition. If the internal temperature rises excessively, the module turns itself off, reducing the output voltage to zero. The module exercises a soft-start power up when the sensed temperature has decreased by about 10°C below the trip point.

**NOTE:** Overtemperature protection is a last-resort mechanism to prevent damage to the module. It should not be relied on as permanent protection against thermal stress. Always operate the module within its temperature derated limits, for the worst-case operating conditions of output current, ambient temperature, and airflow. Operating the module above these limits, albeit below the thermal shutdown temperature, reduces the long-term reliability of the module.

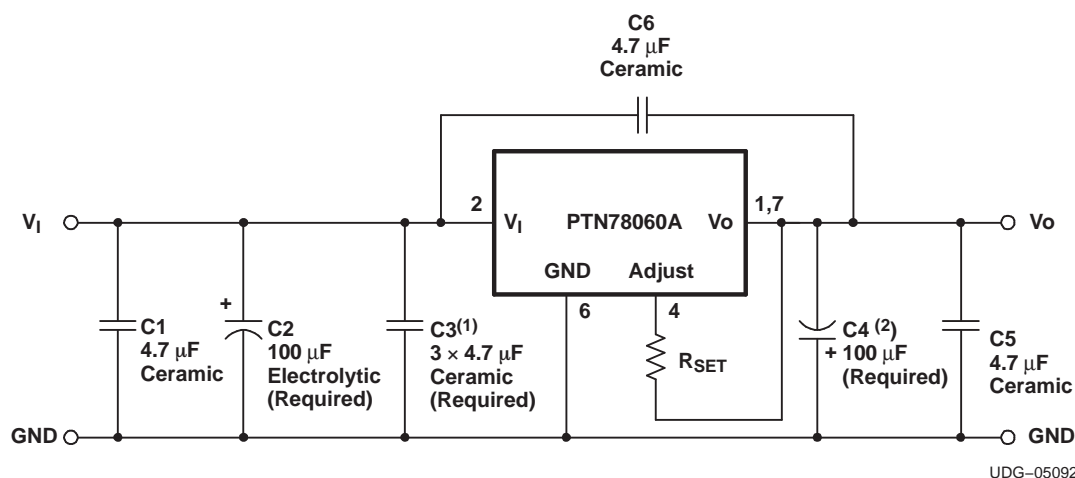
## Optional Input/Output Filters

Power modules include internal input and output ceramic capacitors in all of their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

### Input/Output Capacitors

The easiest way to reduce output ripple and noise is to add one or more 1- $\mu\text{F}$  ceramic capacitors, such as C5 shown in Figure 20. Ceramic capacitors should be placed close to the output power terminals. A single 4.7- $\mu\text{F}$  capacitor reduces the output ripple/noise by 10% to 30% for modules with a rated output current of less than 3 A. (Note: C4 is required to improve the regulators transient response, and does not reduce output ripple and noise.)

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of C1,  $\geq 4.7\text{-}\mu\text{F}$  ( $2 \times 2.2\text{ }\mu\text{F}$ ) ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by up to 20%.



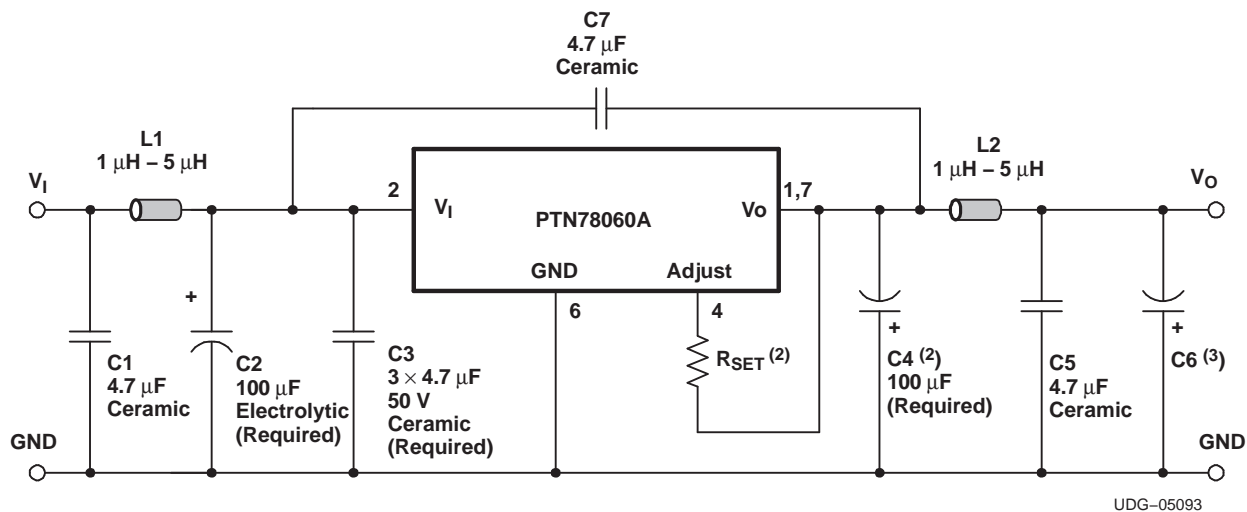
- (1) See the specifications for required value and type.
- (2) See the *Application Information* section for suggested value and type.

**Figure 20. Adding High-Frequency Bypass Capacitors to the Input and Output**

### $\pi$ Filters

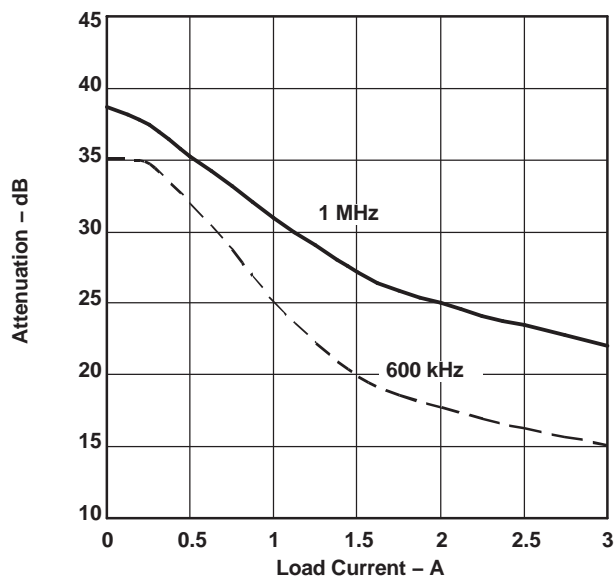
If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A  $\pi$  (pi) filter, employing a ferrite bead (Fair-Rite Pt. No. 2673000701 or equivalent) in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 21 and Figure 22). In order for the inductor to be effective ceramic capacitors are also required. (See the Capacitor Recommendations for additional information on vendors and component suggestions.)

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency (650 kHz - 1 MHz). The placement of this filter is critical. It must be located as close as possible to the input or output pins to be effective. The ferrite bead is small (12,5 mm  $\times$  3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite also manufactures a surface-mount bead (part number 2773021447). It is rated to 5 A, and can be used on the output bus. As an alternative, suitably rated 1- $\mu\text{H}$  to 5- $\mu\text{H}$  wound inductors can be used in place of the ferrite inductor bead.



- (1) See the specifications for required value and type.
- (2) See the *Application Information* section for suggested value and type.
- (3) Recommended when  $I_O > 2$  A..

**Figure 21. Adding  $\pi$  Filters ( $I_O \leq 3$  A)**



**Figure 22.  $\pi$ -Filter Attenuation vs. Load Current**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PTN78060AAH</a>	Active	Production	Through-Hole Module (EUW)   7	36   TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
PTN78060AAH.B	Active	Production	Through-Hole Module (EUW)   7	36   TIW TRAY	Exempt	SN	N/A for Pkg Type	-40 to 85	
<a href="#">PTN78060AAS</a>	Active	Production	Surface Mount Module (EUY)   7	36   TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTN78060AAS.B	Active	Production	Surface Mount Module (EUY)   7	36   TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
<a href="#">PTN78060AAST</a>	Active	Production	Surface Mount Module (EUY)   7	250   SMALL T&R	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTN78060AAST.B	Active	Production	Surface Mount Module (EUY)   7	250   SMALL T&R	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
<a href="#">PTN78060AAZ</a>	Active	Production	Surface Mount Module (EUY)   7	36   TIW TRAY	Exempt	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTN78060AAZ.B	Active	Production	Surface Mount Module (EUY)   7	36   TIW TRAY	Exempt	SNAGCU	Level-3-260C-168 HR	-40 to 85	
<a href="#">PTN78060AAZT</a>	Active	Production	Surface Mount Module (EUY)   7	250   SMALL T&R	Exempt	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTN78060AAZT.B	Active	Production	Surface Mount Module (EUY)   7	250   SMALL T&R	Exempt	SNAGCU	Level-3-260C-168 HR	-40 to 85	

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

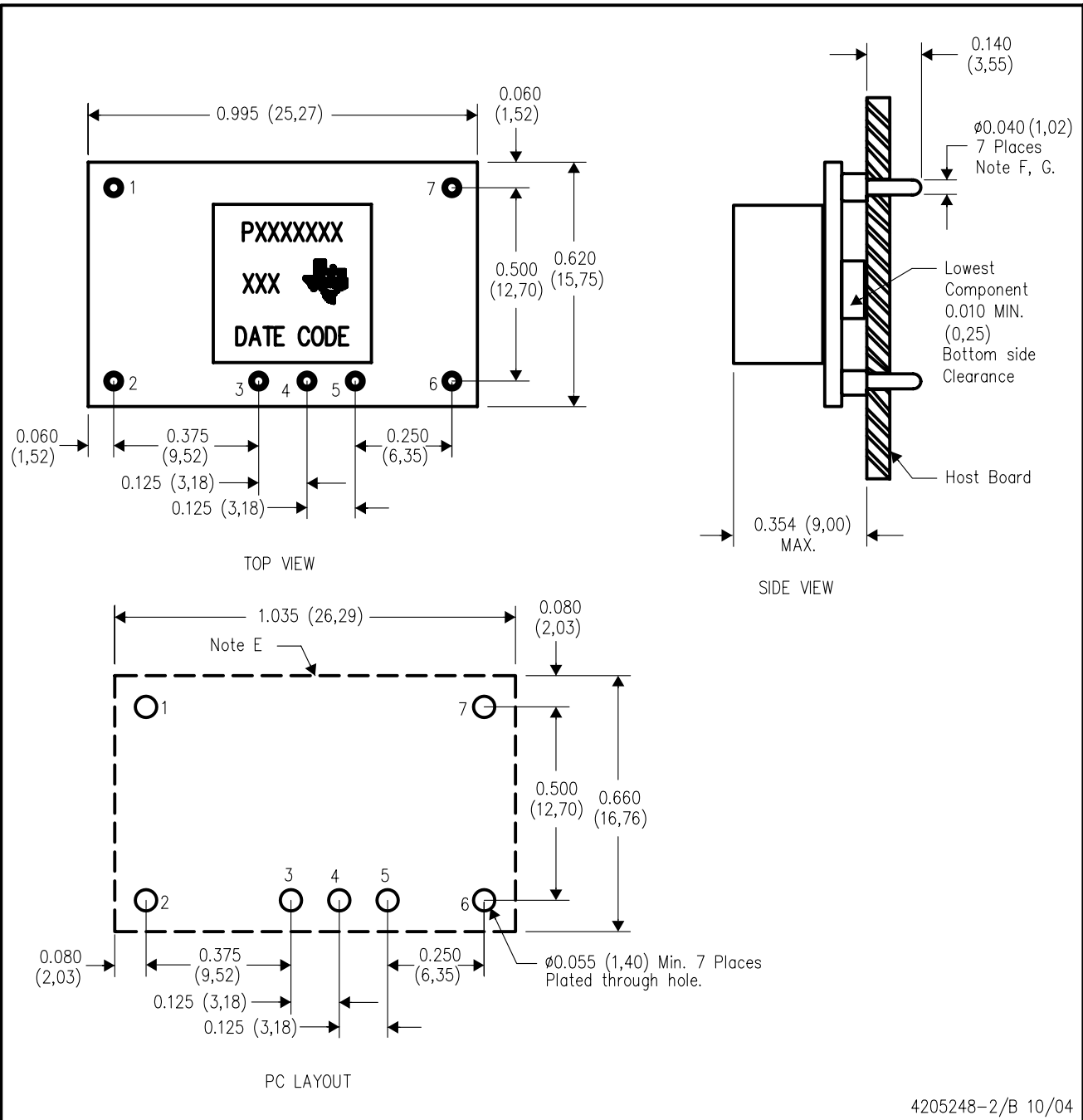
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## EUW (R-PDSS-T7)

## DOUBLE SIDED MODULE

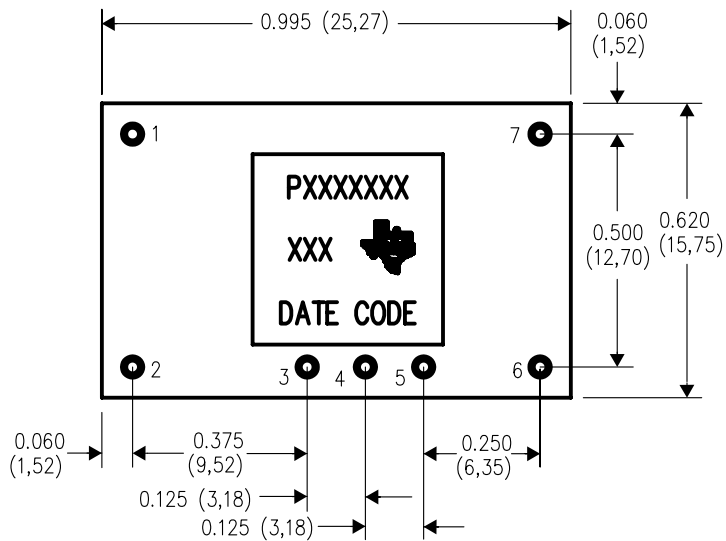


- NOTES:
- A. All linear dimensions are in inches (mm).
  - B. This drawing is subject to change without notice.
  - C. 2 place decimals are  $\pm 0.030$  ( $\pm 0,76$ mm).
  - D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - E. Recommended keep out area for user components

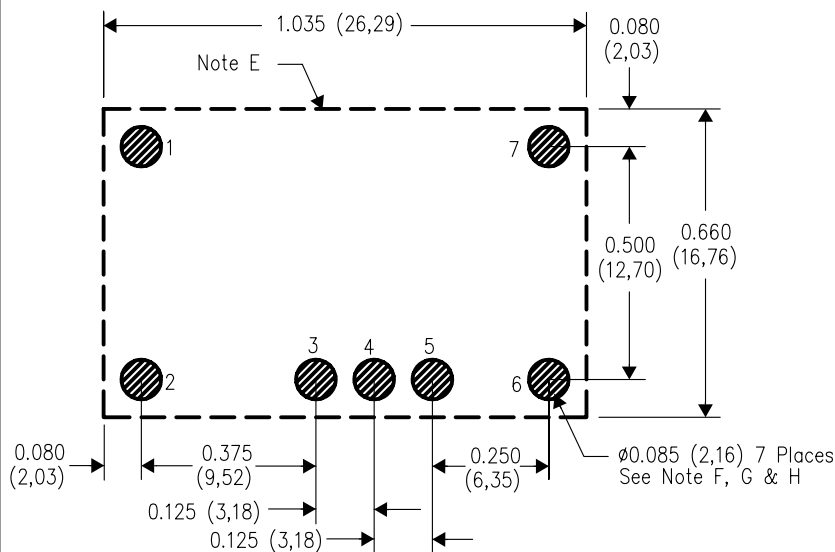
- F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- G. All pins: Material – Copper Alloy  
Finish – Tin (100%) over Nickel plate

## EUY (R-PDSS-B7)

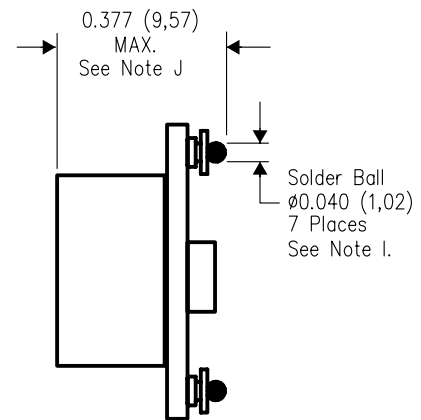
## DOUBLE SIDED MODULE



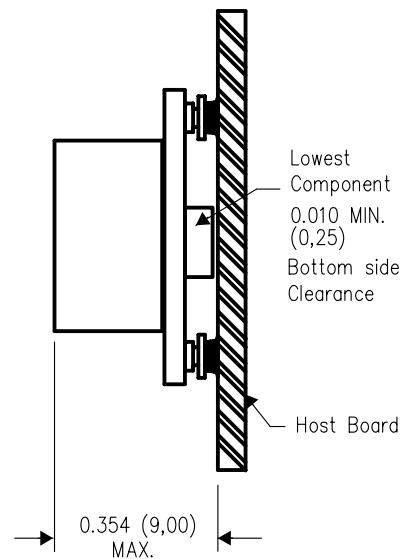
TOP VIEW



PC LAYOUT



SIDE VIEW



4205249-2/B 10/04

- NOTES:
- All linear dimensions are in inches (mm).
  - This drawing is subject to change without notice.
  - 2 place decimals are  $\pm 0.030$  ( $\pm 0,76$ mm).
  - 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - Recommended keep out area for user components.
  - Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).

- Paste screen opening: 0.080 (2,03) to 0.085 (2,16).  
Paste screen thickness: 0.006 (0,15).
- Pad type: Solder mask defined.
- All pins: Material – Copper Alloy  
Finish – Tin (100%) over Nickel plate  
Solder Ball – See product data sheet.
- Dimension prior to reflow solder.

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