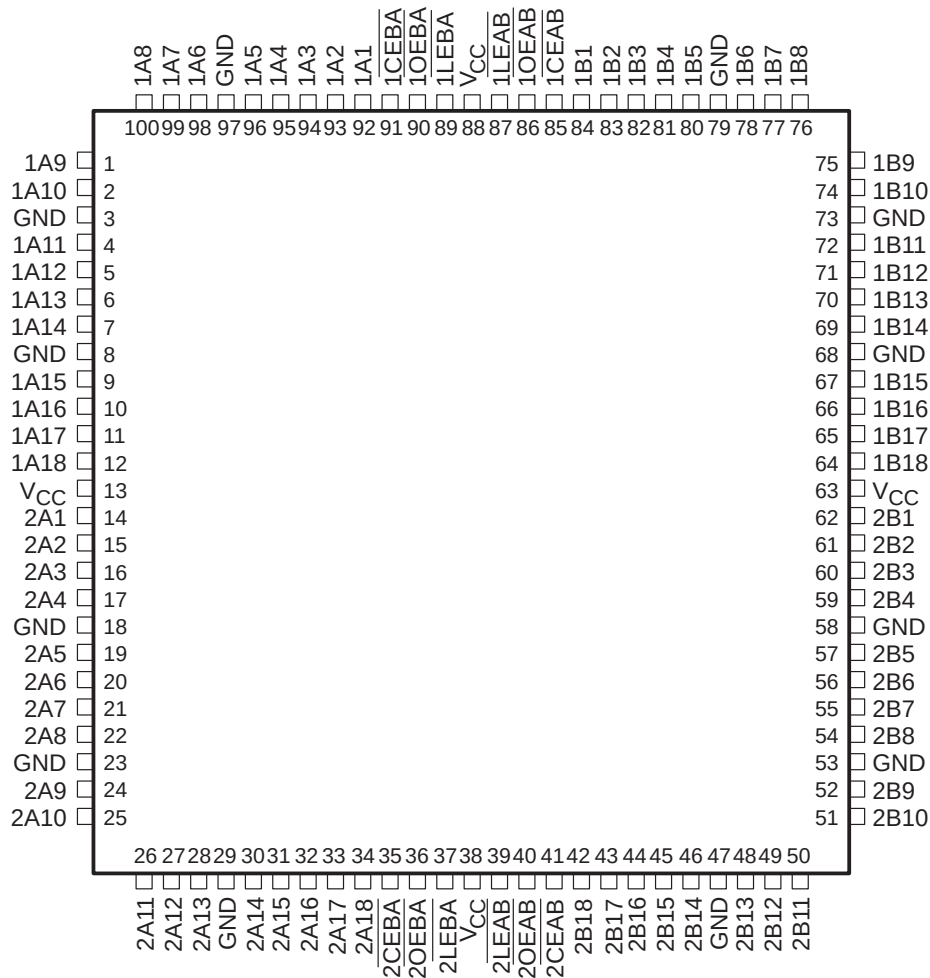


SN54ABTH32543, SN74ABTH32543 36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS230F – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus+™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Released as DSCC SMD 5962-9557801NXD
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With $14 \times 14\text{-mm}$ Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

'ABTH32543 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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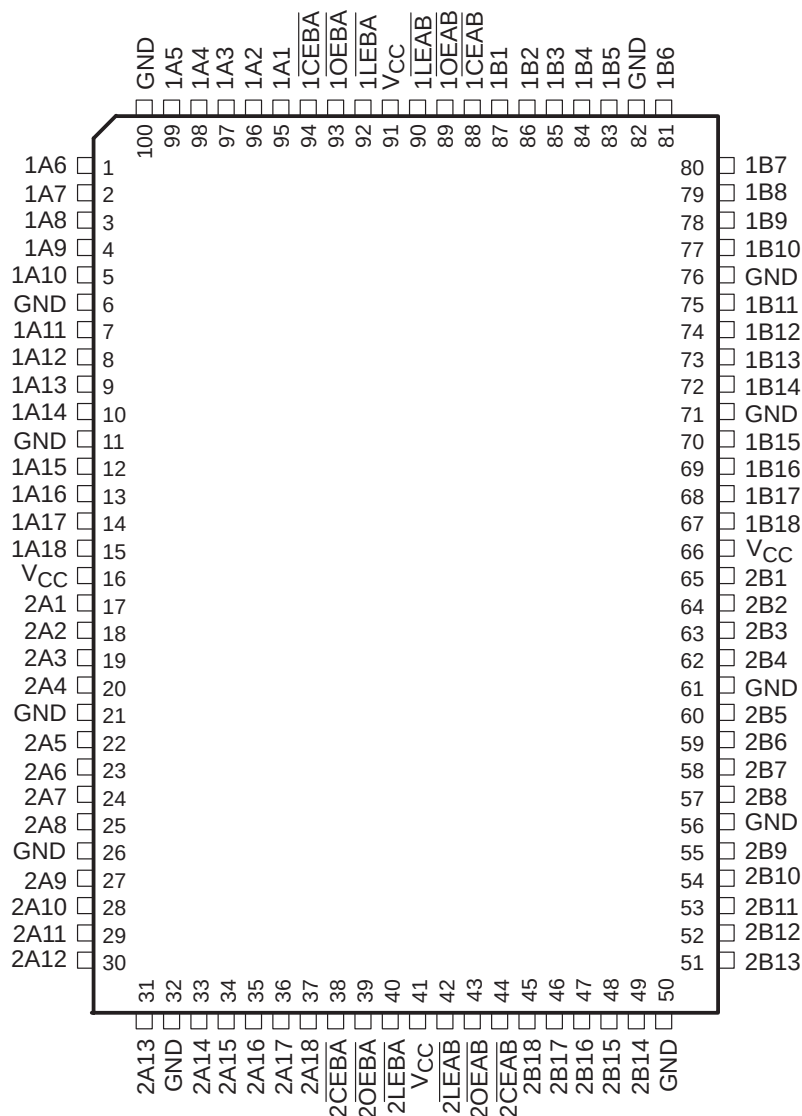
SN54ABTH32543, SN74ABTH32543

36-BIT REGISTERED BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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SN54ABTH32543 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The 'ABTH32543 are 36-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. These devices can be used as two 18-bit transceivers or one 36-bit transceiver. Separate latch-enable ($\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$) and output-enable ($\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{\text{CEAB}}$) input must be low to enter data from A or to output data from B. If $\overline{\text{CEAB}}$ is low and $\overline{\text{LEAB}}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{\text{LEAB}}$ puts the A latches in the storage mode. With $\overline{\text{CEAB}}$ and $\overline{\text{OEAB}}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$ inputs.



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SN54ABTH32543, SN74ABTH32543
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description (continued)

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH32543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH32543 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE[†]
(each 18-bit section)

INPUTS				OUTPUT B
$\overline{\text{CEAB}}$	$\overline{\text{LEAB}}$	$\overline{\text{OEAB}}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	$B_0^{\ddagger}$
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

[‡] Output level before the indicated steady-state input conditions were established

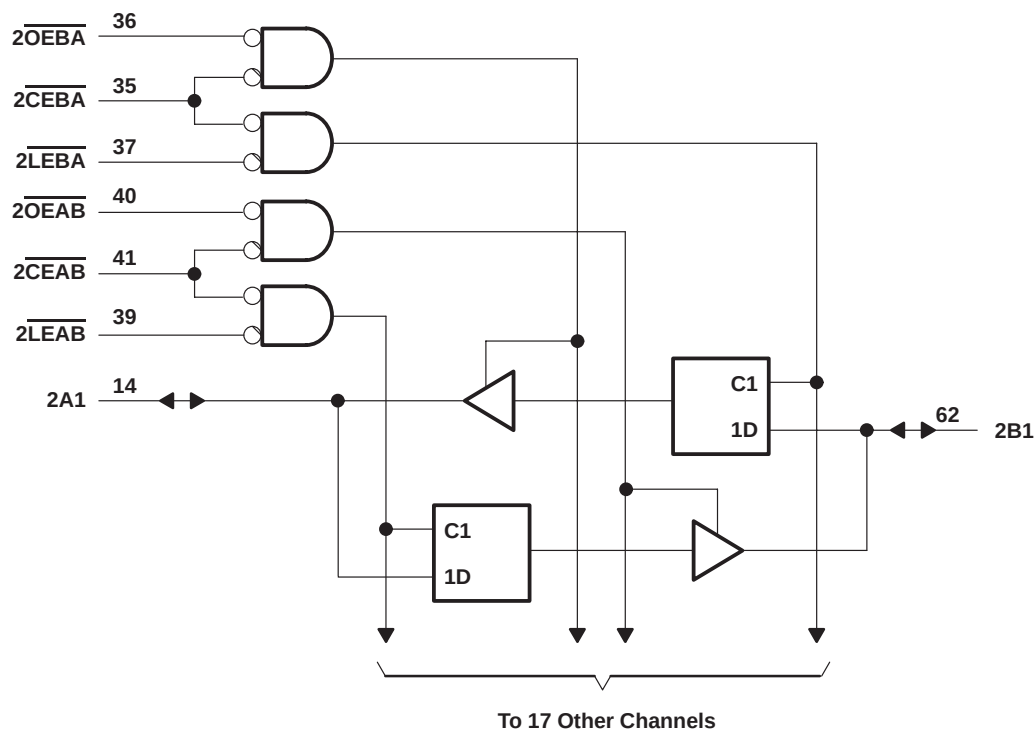
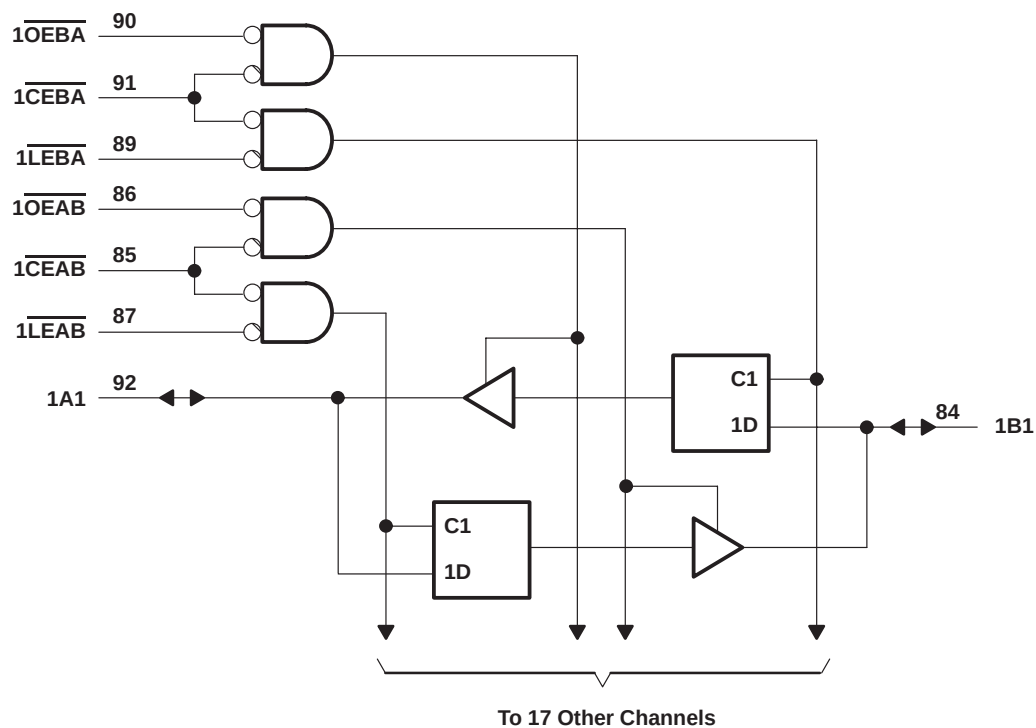
SN54ABTH32543, SN74ABTH32543

36-BIT REGISTERED BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the PZ package.

SN54ABTH32543, SN74ABTH32543

36-BIT REGISTERED BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32543	96 mA
SN74ABTH32543	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package	50°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH32543		SN74ABTH32543		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



SN54ABTH32543, SN74ABTH32543
36-BIT REGISTERED BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32543			SN74ABTH32543			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2			–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5			V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3			
		V _{CC} = 4.5 V	2			2			
V _{OL}		V _{CC} = 4.5 V			0.55			0.55	V
								0.55	
V _{hys}			100			100			mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND						±1	μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND						±20	
	Control inputs	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1				
	A or B ports				±20				
I _I (hold)	A or B ports	V _{CC} = 4.5 V						100	μA
								–100	
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50			±50	μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X			±50			±50	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V						±100	μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V			50			50	μA
I _O §		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–100	–180	mA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			3			3	mA
					20			20	
					2			2	
ΔI _{CC} ¶		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1			1	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V			3.5			3.5	pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V			9.5			9.5	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This parameter is specified by characterization.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, T _A = 25°C#		SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		3.3		3.3		3.3		ns
t _{su}	Setup time	Data before $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	2.1		2.6		2.1		ns
		Data before $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	1.7		2		1.7		
t _h	Hold time	Data after $\overline{LEAB}\uparrow$ or $\overline{LEBA}\uparrow$	0.6		1.1		0.6		ns
		Data after $\overline{CEAB}\uparrow$ or $\overline{CEBA}\uparrow$	0.9		1.2		0.9		

These limits apply only to the SN74ABTH32543.



SN54ABTH32543, SN74ABTH32543
36-BIT REGISTERED BUS TRANSCEIVERS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}^\dagger$			SN54ABTH32543		SN74ABTH32543		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1	3.5	5.2	0.5	6.3	1	5.9	ns
t_{PHL}			1	3.5	5.1	0.5	5.9	1	5.7	
t_{PLH}	$\overline{LE}$	A or B	1.9	4.6	6.3	0.8	7.9	1.9	7.5	ns
t_{PHL}			1.9	4.3	5.9	0.8	6.9	1.9	6.6	
t_{PZH}	$\overline{CE}$	A or B	1.7	4.3	6.7	0.8	8.3	1.7	8	ns
t_{PZL}			2.6	5.2	8	1	8.8	2.6	8.8	
t_{PHZ}	$\overline{CE}$	A or B	1.6	3.8	6.6	0.5	7.4	1.6	7.1	ns
t_{PLZ}			2.4	4.6	7	1	7.9	2.4	7.5	
t_{PZH}	$\overline{OE}$	A or B	1.4	3.8	6.1	0.5	7.6	1.4	7.3	ns
t_{PZL}			2.3	4.7	7.4	1	8.2	2.3	8.1	
t_{PHZ}	$\overline{OE}$	A or B	1.3	3.4	6.1	0.5	6.7	1.3	6.5	ns
t_{PLZ}			2	4.2	6.6	0.8	7.2	2	6.9	

[†] These limits apply only to the SN74ABTH32543.

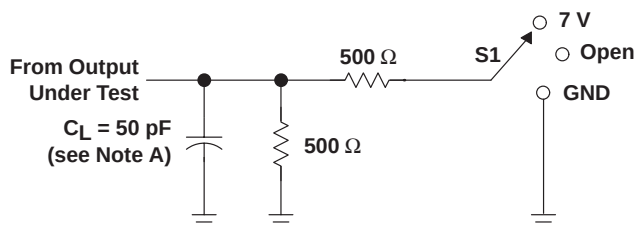
SN54ABTH32543, SN74ABTH32543

36-BIT REGISTERED BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

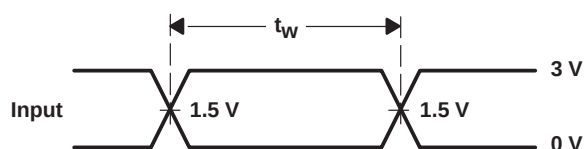
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PARAMETER MEASUREMENT INFORMATION

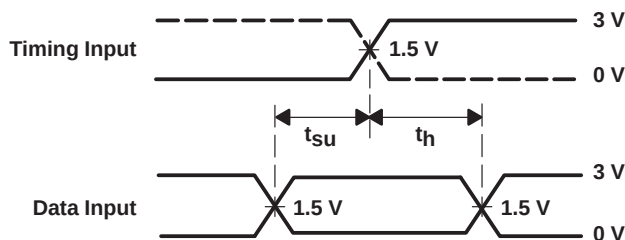


LOAD CIRCUIT

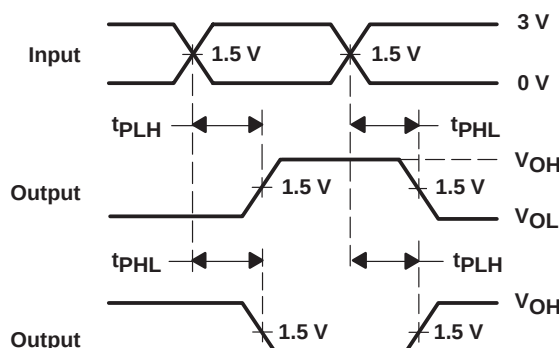
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



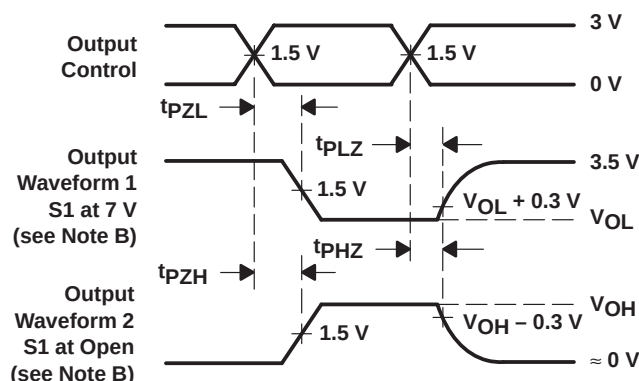
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9557801NXD	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	9557801NXD ABTH32543
SN74ABTH32543PZ	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32543
SN74ABTH32543PZ.B	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32543

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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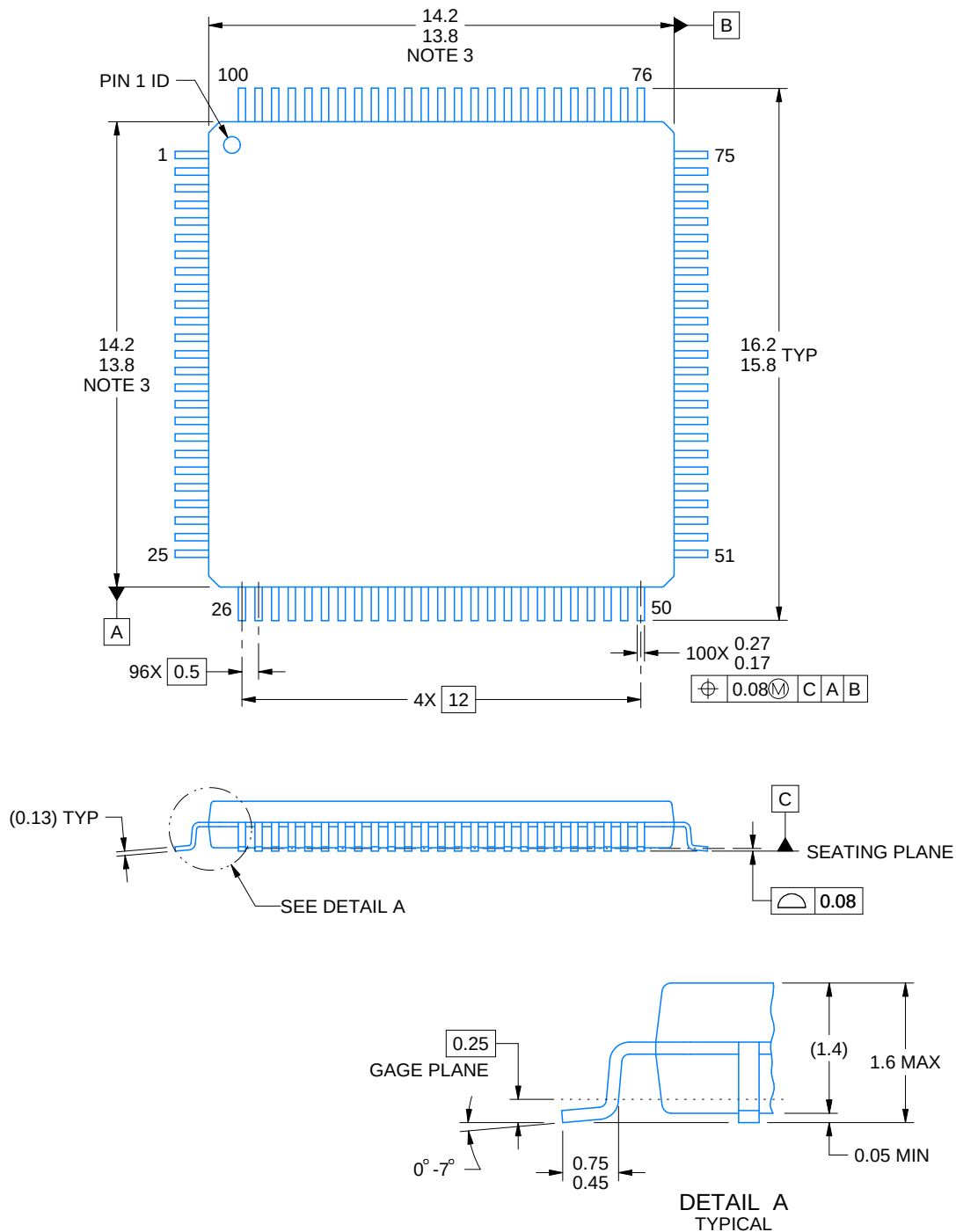
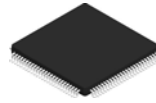
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ABTH32543, SN74ABTH32543 :

- Catalog : [SN74ABTH32543](#)
- Military : [SN54ABTH32543](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



4215169/A 03/2017

NOTES:

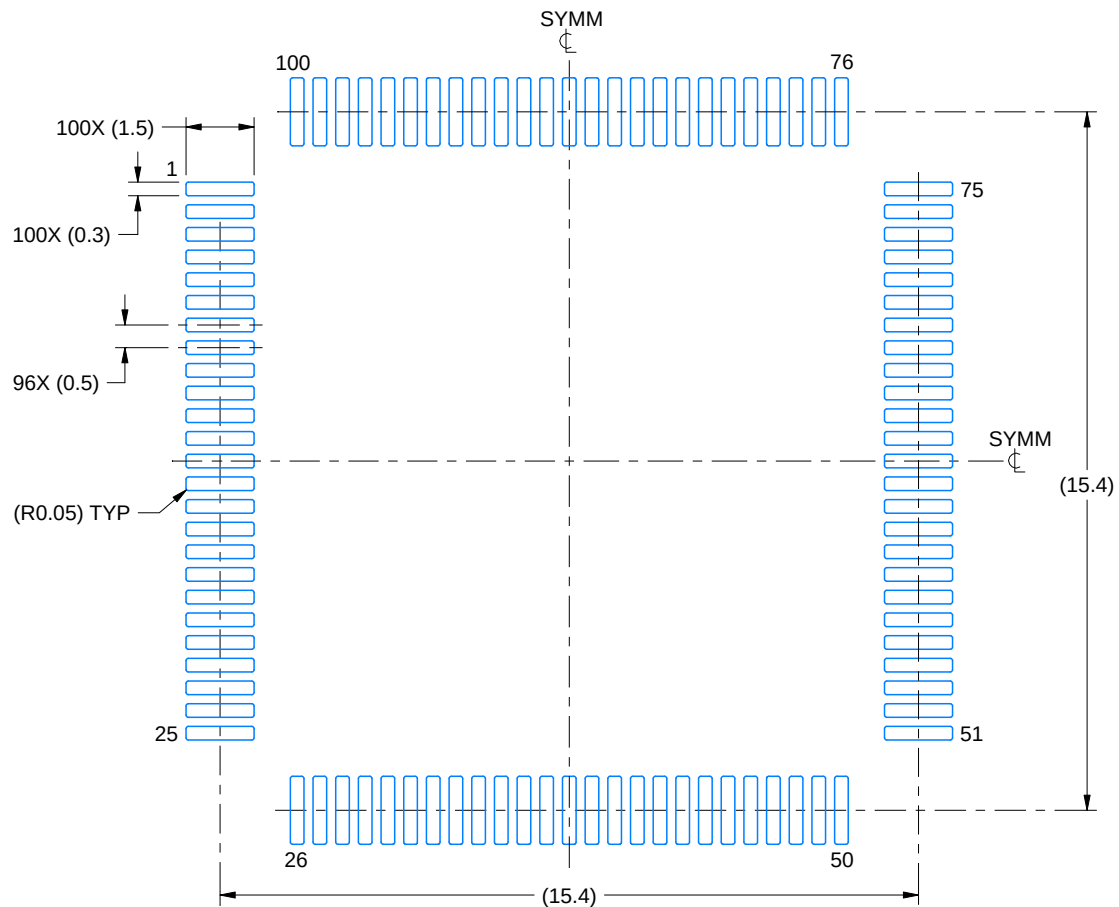
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

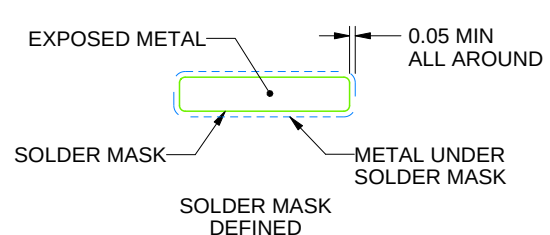
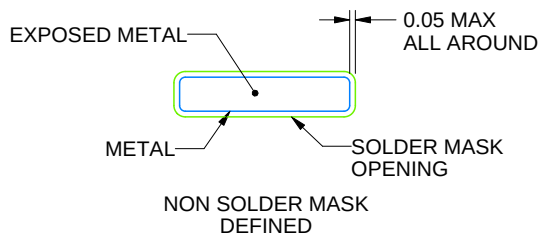
PZ0100A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

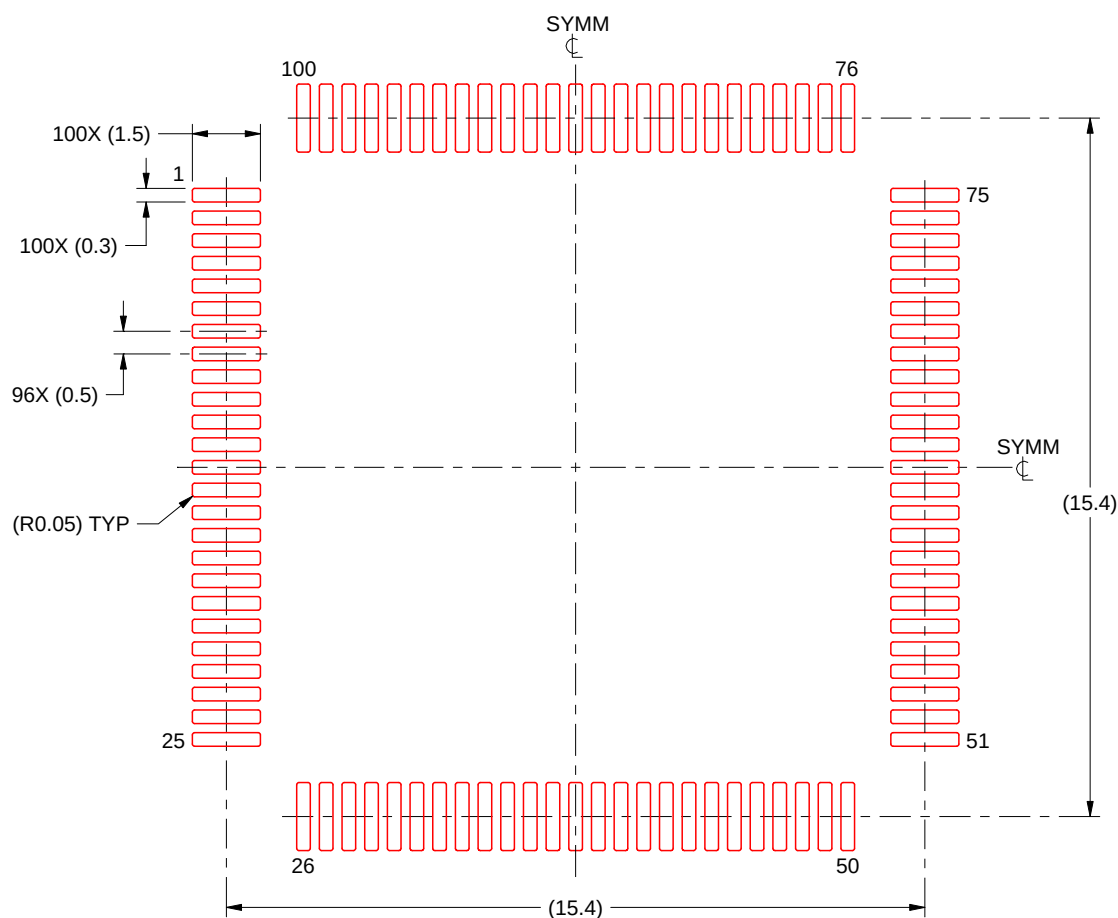
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PZ0100A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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