

- Members of the Texas Instruments *Widebus™* Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Flow-Through Architecture Optimizes PCB Layout
- Distributed  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- *EPIC™* (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages, and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

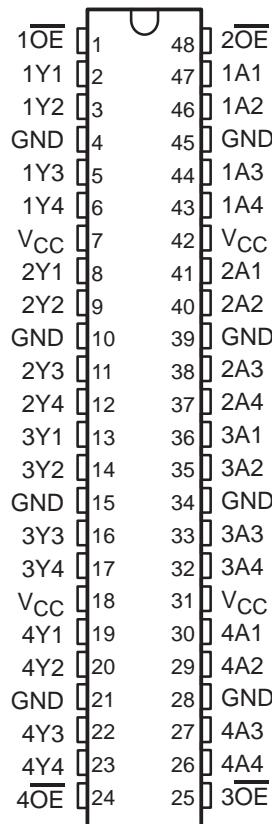
#### description

The SN54ACT16244 and 74ACT16244 are 16-bit buffers/line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. They can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. The devices provide true outputs and symmetrical  $\overline{OE}$  (active-low) output-enable inputs.

The 74ACT16244 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54ACT16244 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16244 is characterized for operation from –40°C to 85°C.

SN54ACT16244 . . . WD PACKAGE  
74ACT16244 . . . DGG OR DL PACKAGE  
(TOP VIEW)



FUNCTION TABLE  
(each driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
L	H	H
L	L	L
H	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

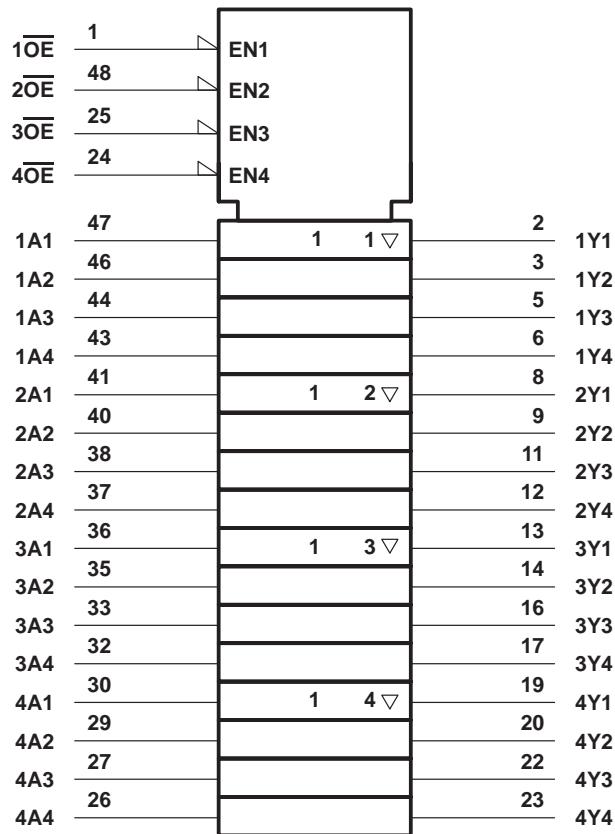
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**SN54ACT16244, 74ACT16244  
16-BIT BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

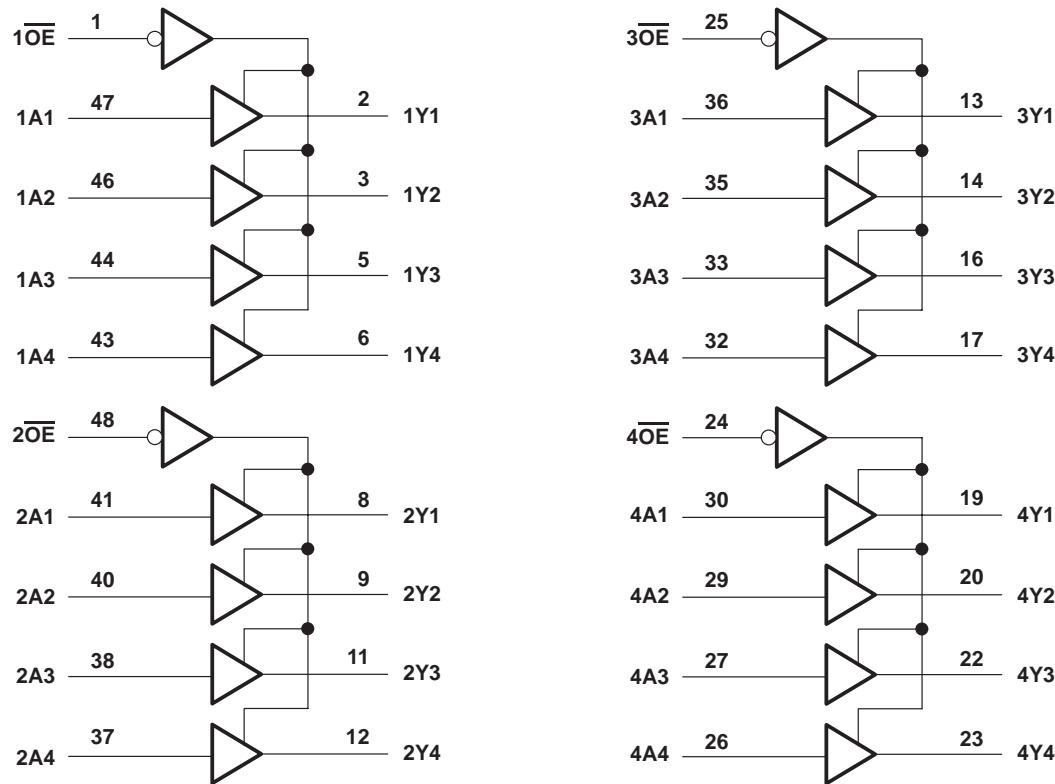
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**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±400 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package .....	0.85 W
	DL package .....
	1.2 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**SN54ACT16244, 74ACT16244  
16-BIT BUFFERS/LINE DRIVERS  
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**recommended operating conditions (see Note 3)**

		SN54ACT16244		74ACT16244		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage (see Note 4)	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-24		-24	mA
I <sub>OL</sub>	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTES: 3. Unused inputs should be tied to V<sub>CC</sub> through a pullup resistor of approximately 5 kΩ or greater to prevent them from floating.  
4. All V<sub>CC</sub> and GND pins must be connected to the proper voltage supply.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54ACT16244	74ACT16244	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4		4.4		4.4	V
		5.5 V	5.4		5.4		5.4	
	I <sub>OH</sub> = -24 mA	4.5 V	3.94		3.7		3.8	
		5.5 V	4.94		4.7		4.8	
	I <sub>OH</sub> = -50 mA <sup>†</sup>	5.5 V			3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V		0.1		0.1	0.1	V
		5.5 V		0.1		0.1	0.1	
	I <sub>OL</sub> = 24 mA	4.5 V		0.36		0.5	0.44	
		5.5 V		0.36		0.5	0.44	
	I <sub>OL</sub> = 50 mA <sup>†</sup>	5.5 V			1.65			
	I <sub>OL</sub> = 75 mA <sup>†</sup>	5.5 V					1.65	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V		±0.1		±1	±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V		±0.5		±10	±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		8		160	80	μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.9		1	1	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5				pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		13.5				pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

<sup>‡</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ACT16244			UNIT	
			TA = 25°C				
			MIN	TYP	MAX		
t <sub>PLH</sub>	A	Y	4	6.5	8.5	3	10.3
t <sub>PHL</sub>			3.4	6.3	8.7	3.4	10.1
t <sub>PZH</sub>	OE	Y	3	5.8	8.1	3	10.5
t <sub>PZL</sub>			3.7	6.7	9.3	3.7	11
t <sub>PHZ</sub>	OE	Y	5.4	8.1	11.5	5.4	13
t <sub>PLZ</sub>			5	7.5	9.5	5	10.9

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	74ACT16244			UNIT	
			TA = 25°C				
			MIN	TYP	MAX		
t <sub>PLH</sub>	A	Y	4	6.5	8.5	4	9.4
t <sub>PHL</sub>			3.4	6.3	8.7	3.4	9.5
t <sub>PZH</sub>	OE	Y	3	5.8	8.1	3	8.9
t <sub>PZL</sub>			3.7	6.7	9.3	3.7	10.3
t <sub>PHZ</sub>	OE	Y	5.4	8.1	10.3	5.4	11.3
t <sub>PLZ</sub>			5	7.5	9.5	5	10.3

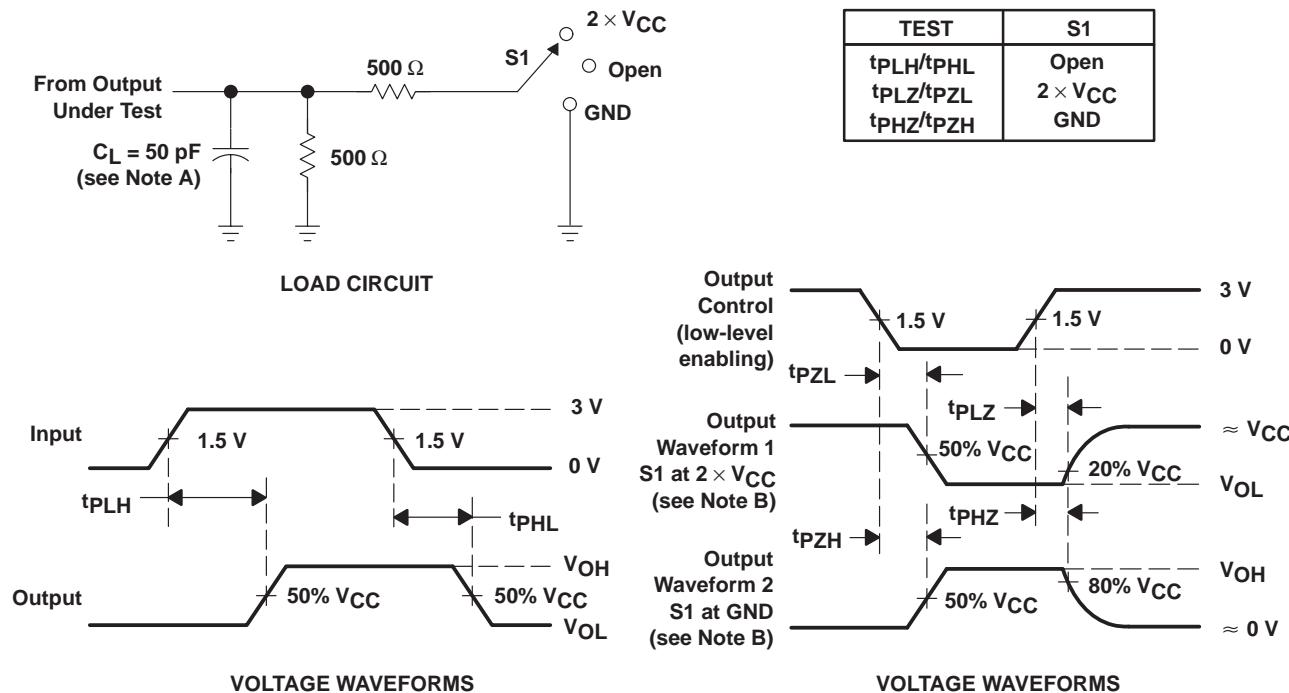
operating characteristics, V<sub>CC</sub> = 5 V, TA = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	C <sub>L</sub> = 50 pF, f = 1 MHz	39	pF
		Outputs disabled		11	

**SN54ACT16244, 74ACT16244  
16-BIT BUFFERS/LINE DRIVERS  
WITH 3-STATE OUTPUTS**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 3$  ns,  $t_f = 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9202201Mxa	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9202201MX A SNJ54ACT16244WD
74ACT16244DGG	Obsolete	Production	TSSOP (DGG)   48	-	-	Call TI	Call TI	-	ACT16244
74ACT16244DGGR	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
74ACT16244DGGR.A	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
74ACT16244DGGRG4	Active	Production	TSSOP (DGG)   48	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
74ACT16244DL	Obsolete	Production	SSOP (DL)   48	-	-	Call TI	Call TI	-40 to 85	ACT16244
74ACT16244DLR	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
74ACT16244DLR.A	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
74ACT16244DLRG4	Active	Production	SSOP (DL)   48	1000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT16244
SNJ54ACT16244WD	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-	5962-9202201MX A SNJ54ACT16244WD
SNJ54ACT16244WD.A	Active	Production	CFP (WD)   48	15   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9202201MX A SNJ54ACT16244WD

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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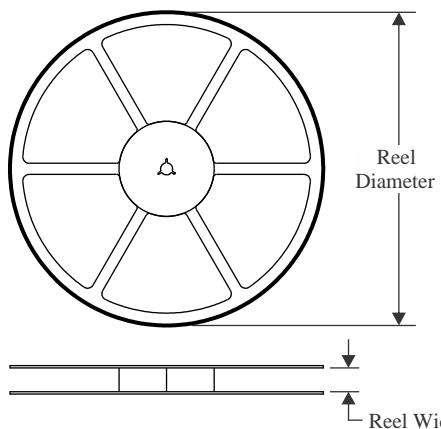
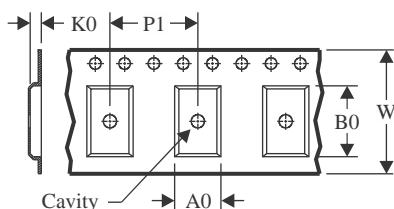
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

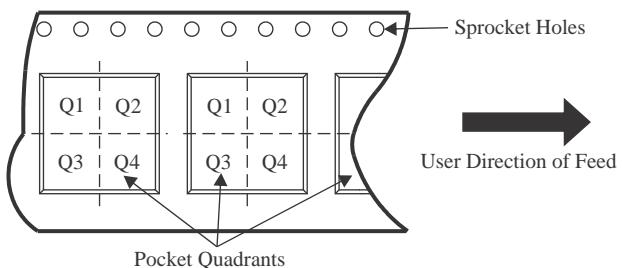
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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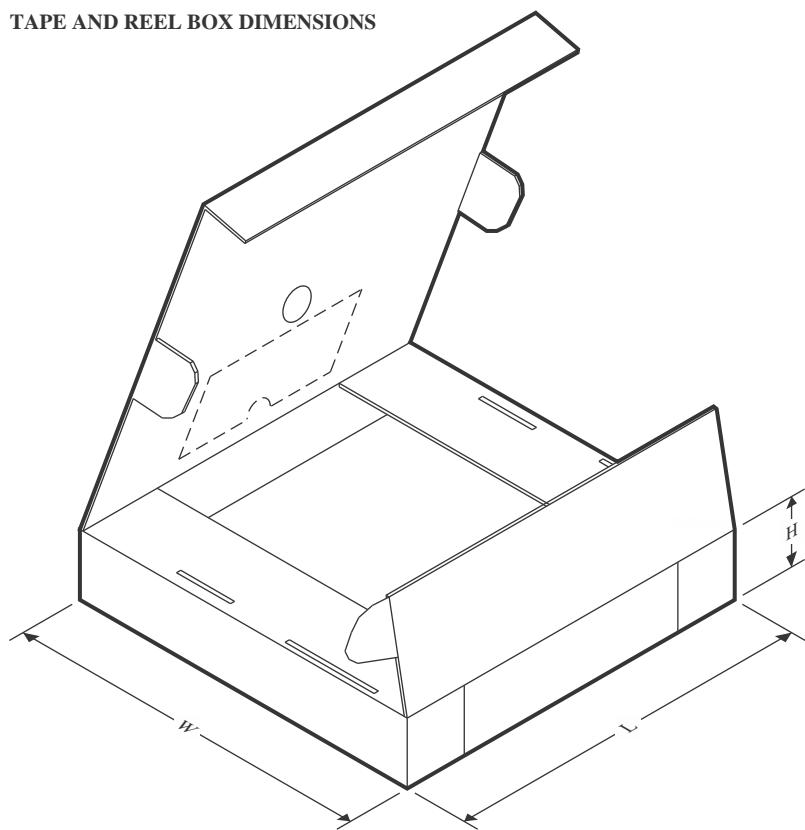
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74ACT16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


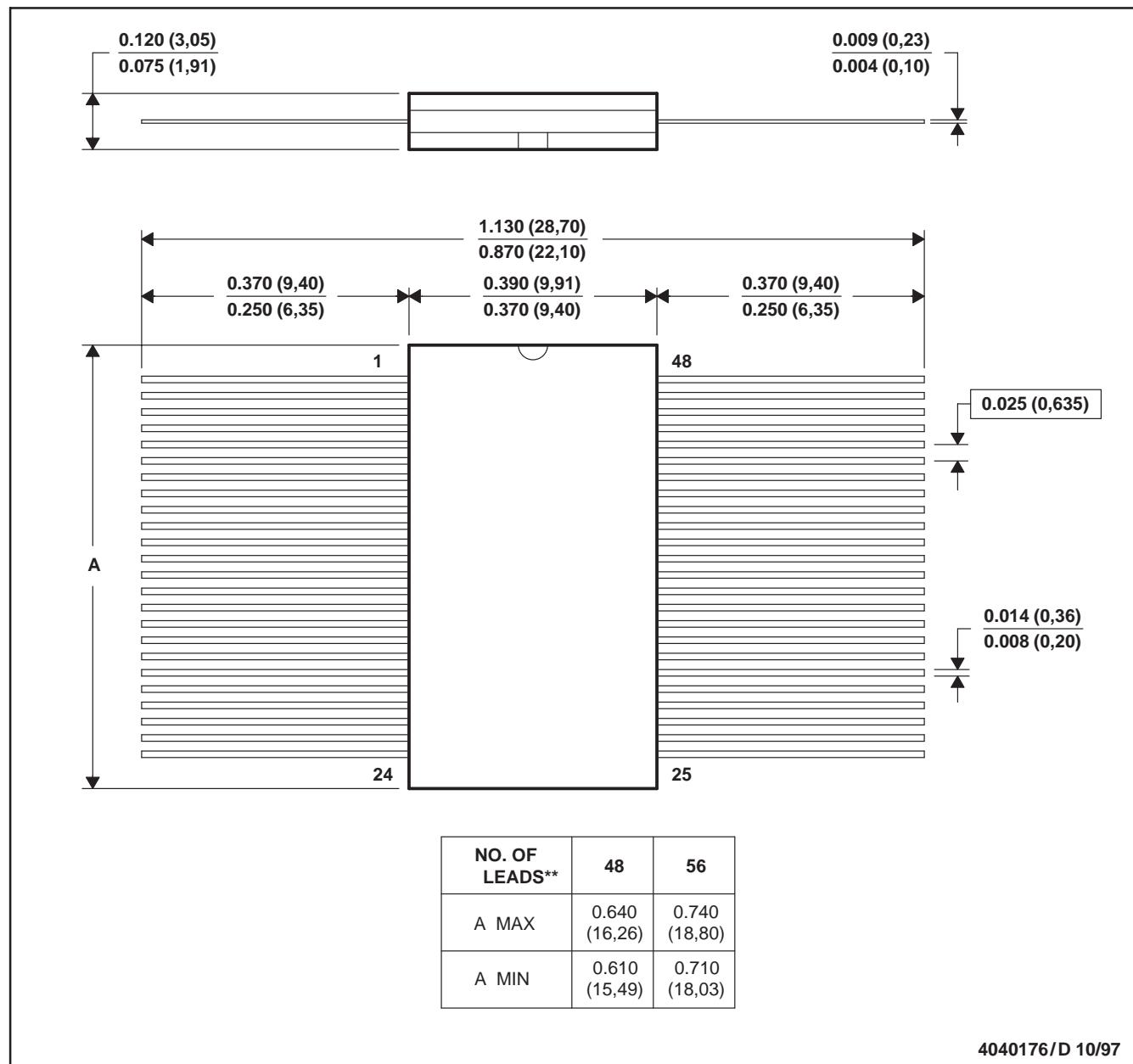
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16244DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
74ACT16244DLR	SSOP	DL	48	1000	356.0	356.0	53.0

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

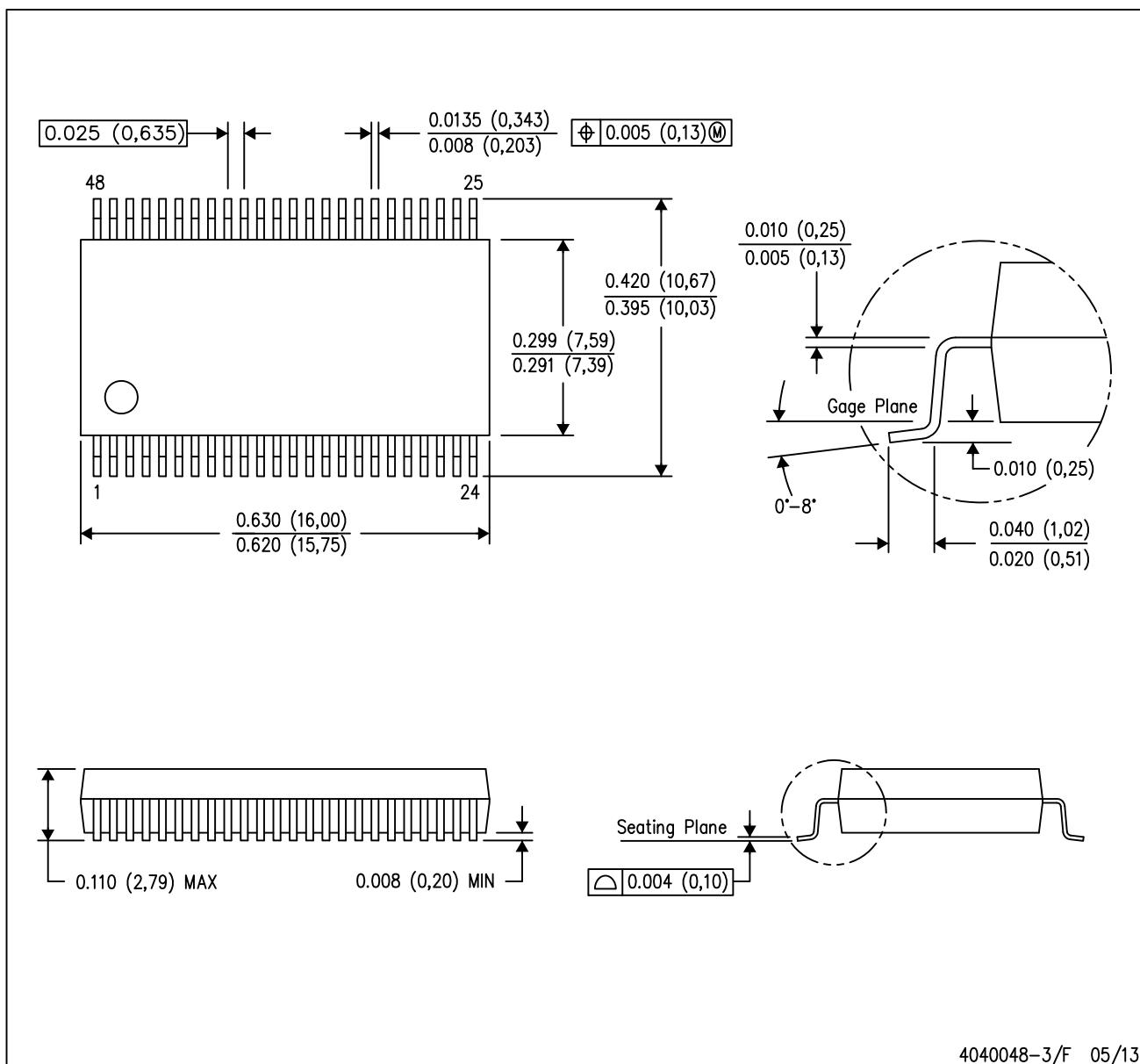
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only.  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



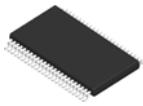
4040048-3/F 05/13

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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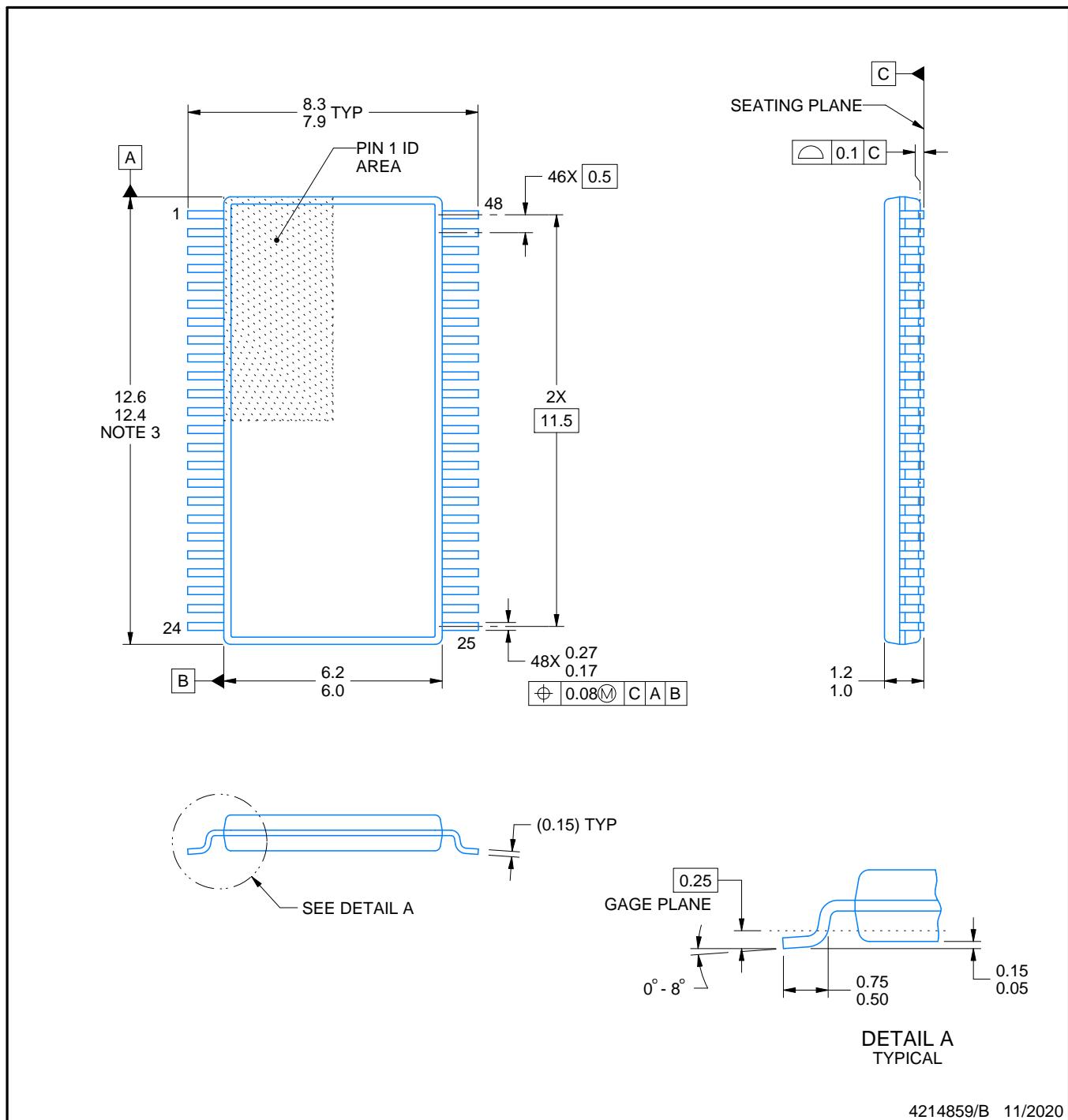
## PACKAGE OUTLINE

**DGG0048A**



## **TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



## NOTES:

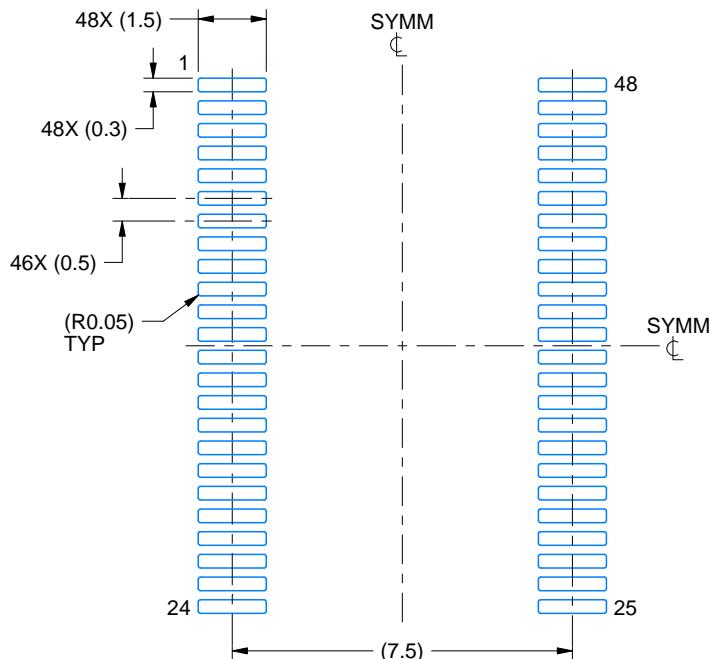
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
  4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

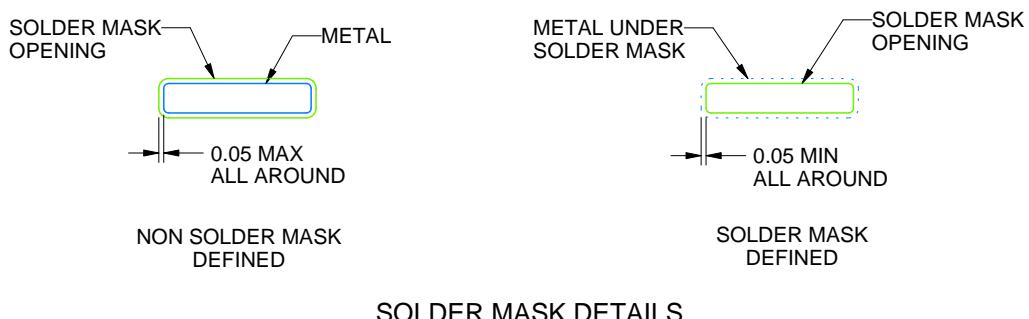
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

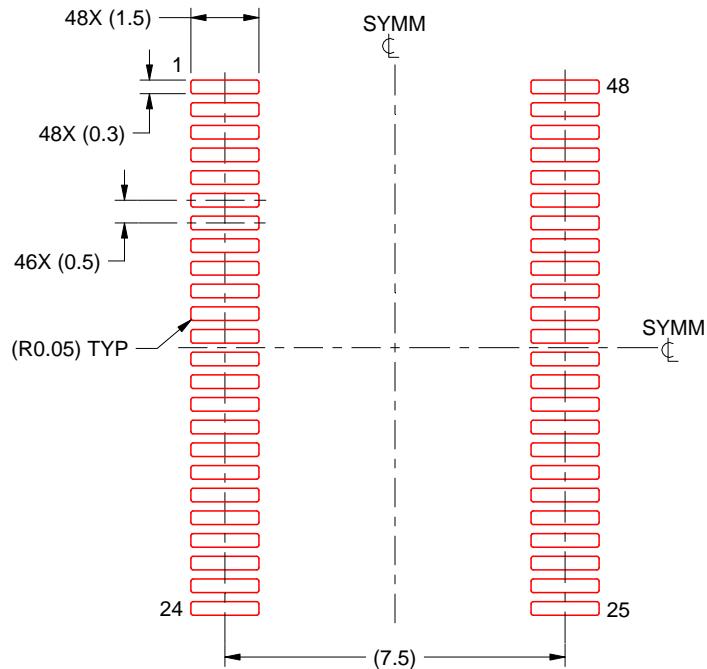
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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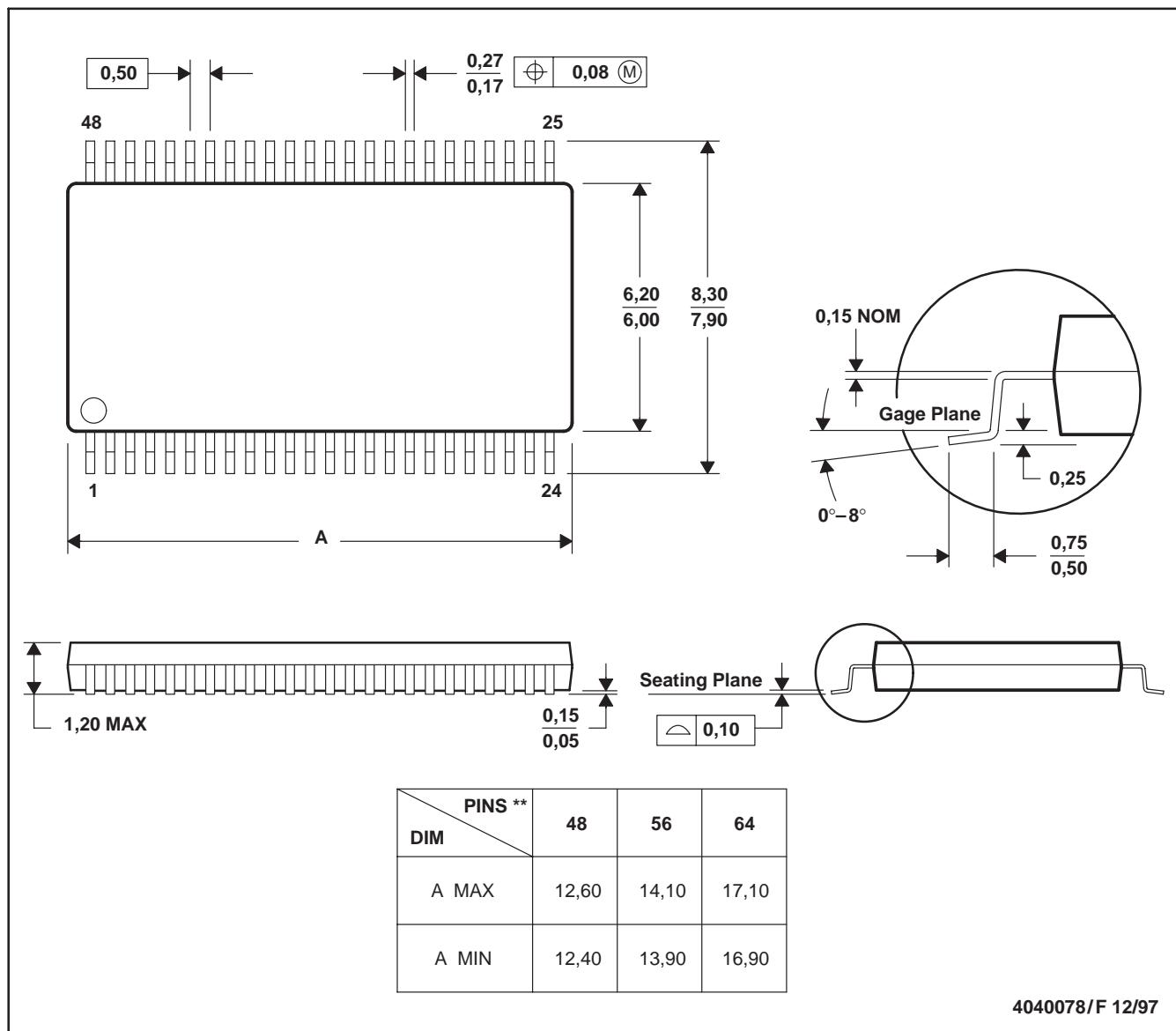
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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