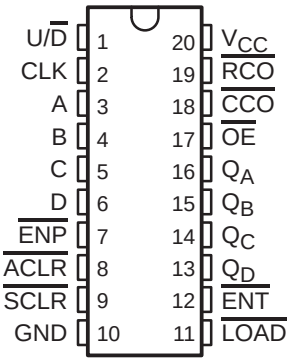
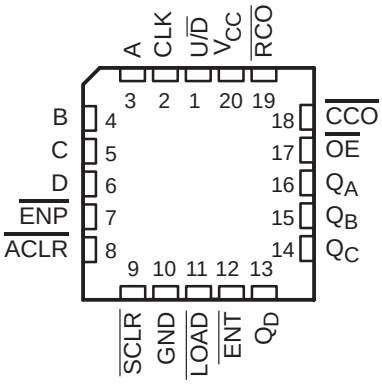
- **3-State Q Outputs Drive Bus Lines Directly**
- **Counter Operation Independent of 3-State Output**
- **Fully Synchronous Clear, Count, and Load**
- **Asynchronous Clear Is Also Provided**
- **Fully Cascadable**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

**SN54ALS569A . . . J PACKAGE**
**SN74ALS568A, SN74ALS569A . . . DW OR N PACKAGE**
**(TOP VIEW)**




**SN54ALS569A . . . FK PACKAGE**
**(TOP VIEW)**




## description

The SN74ALS568A decade counter and ′ALS569A binary counters are programmable, count up or down, and offer both synchronous and asynchronous clearing. All synchronous functions are executed on the positive-going edge of the clock (CLK) input.

The clear function is initiated by applying a low level to either asynchronous clear ($\overline{\text{ACLR}}$) or synchronous clear ($\overline{\text{SCLR}}$). Asynchronous (direct) clearing overrides all other functions of the device, while synchronous clearing overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by holding load ($\overline{\text{LOAD}}$) low during a positive-going clock transition. The counting function is enabled only when enable P ($\overline{\text{ENP}}$) and enable T ($\overline{\text{ENT}}$) are low and $\overline{\text{ACLR}}$, $\overline{\text{SCLR}}$, and $\overline{\text{LOAD}}$ are high. The up/down (U/$\overline{\text{D}}$) input controls the direction of the count. These counters count up when U/$\overline{\text{D}}$ is high and count down when U/$\overline{\text{D}}$ is low.

A high level at the output-enable ($\overline{\text{OE}}$) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{\text{OE}}$. $\overline{\text{ENT}}$ is fed forward to enable the ripple-carry output ($\overline{\text{RCO}}$) to produce a low-level pulse while the count is zero (all Q outputs low) when counting down or maximum (9 or 15) when counting up. The clocked carry output ($\overline{\text{CCO}}$) produces a low-level pulse for a duration equal to that of the low level of the clock when $\overline{\text{RCO}}$ is low and the counter is enabled (both $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ are low); otherwise, $\overline{\text{CCO}}$ is high. $\overline{\text{CCO}}$ does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting $\overline{\text{RCO}}$ or $\overline{\text{CCO}}$ of the first counter to $\overline{\text{ENT}}$ of the next counter. However, for very high-speed counting, $\overline{\text{RCO}}$ should be used for cascading since $\overline{\text{CCO}}$ does not become active until the clock returns to the low level.

The SN54ALS569A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS568A and SN74ALS569A are characterized for operation from 0°C to 70°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

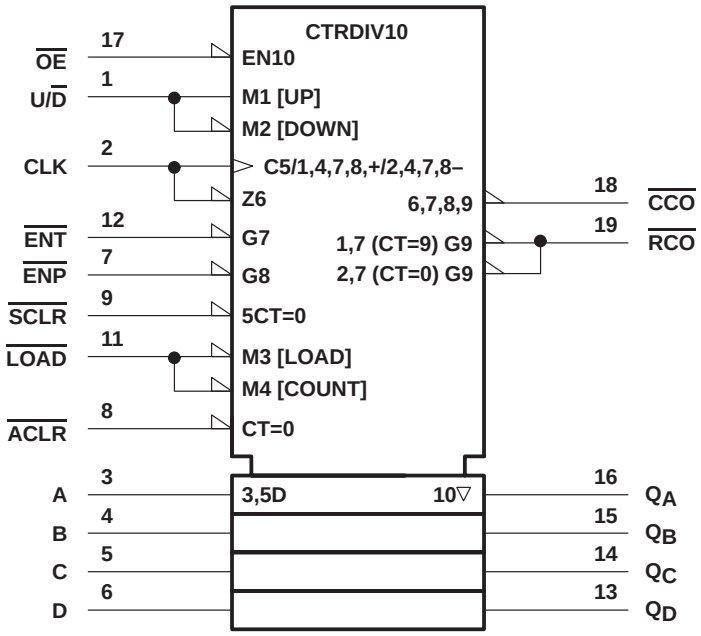
Copyright © 1995, Texas Instruments Incorporated

**FUNCTION TABLE**

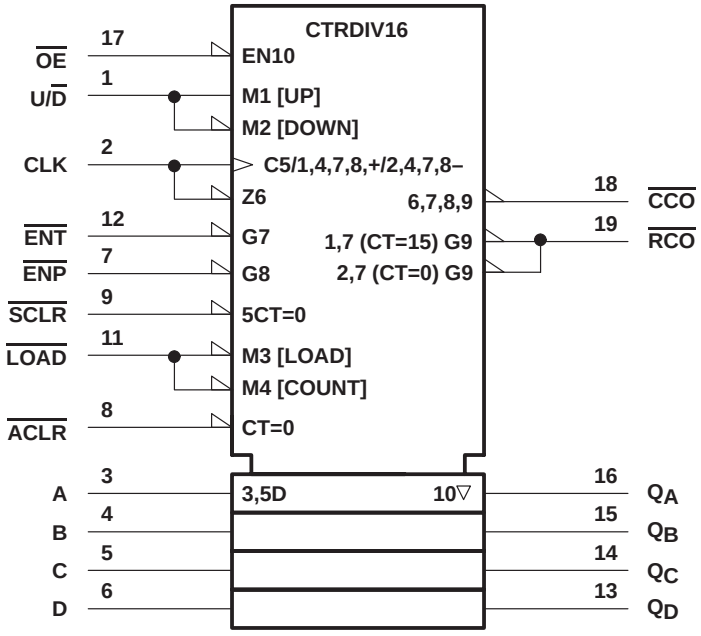
| INPUTS | | | | | | | | OPERATION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{ACLR}$ | $\overline{SCLR}$ | $\overline{LOAD}$ | $\overline{ENT}$ | $\overline{ENP}$ | U/$\overline{D}$ | CLK | |
| H | X | X | X | X | X | X | X | Q outputs disabled |
| L | L | X | X | X | X | X | X | Asynchronous clear |
| L | H | L | X | X | X | X | ↑ | Synchronous clear |
| L | H | H | L | X | X | X | ↑ | Load |
| L | H | H | H | L | L | H | ↑ | Count up |
| L | H | H | H | L | L | L | ↑ | Count down |
| L | H | H | H | H | X | X | X | Inhibit count |
| L | H | H | H | X | H | X | X | Inhibit count |

## logic symbols†

SN74ALS568A



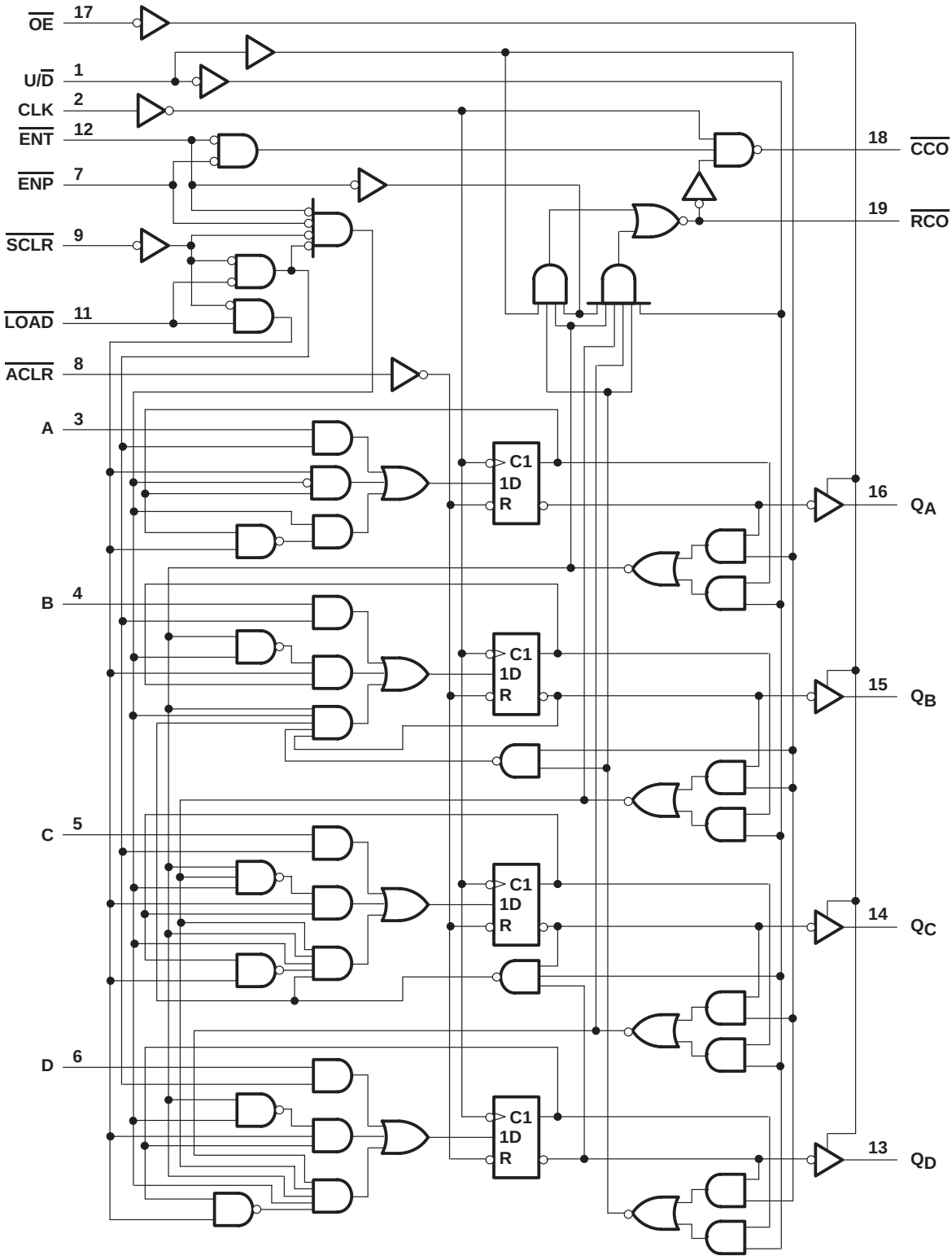

′ALS569A



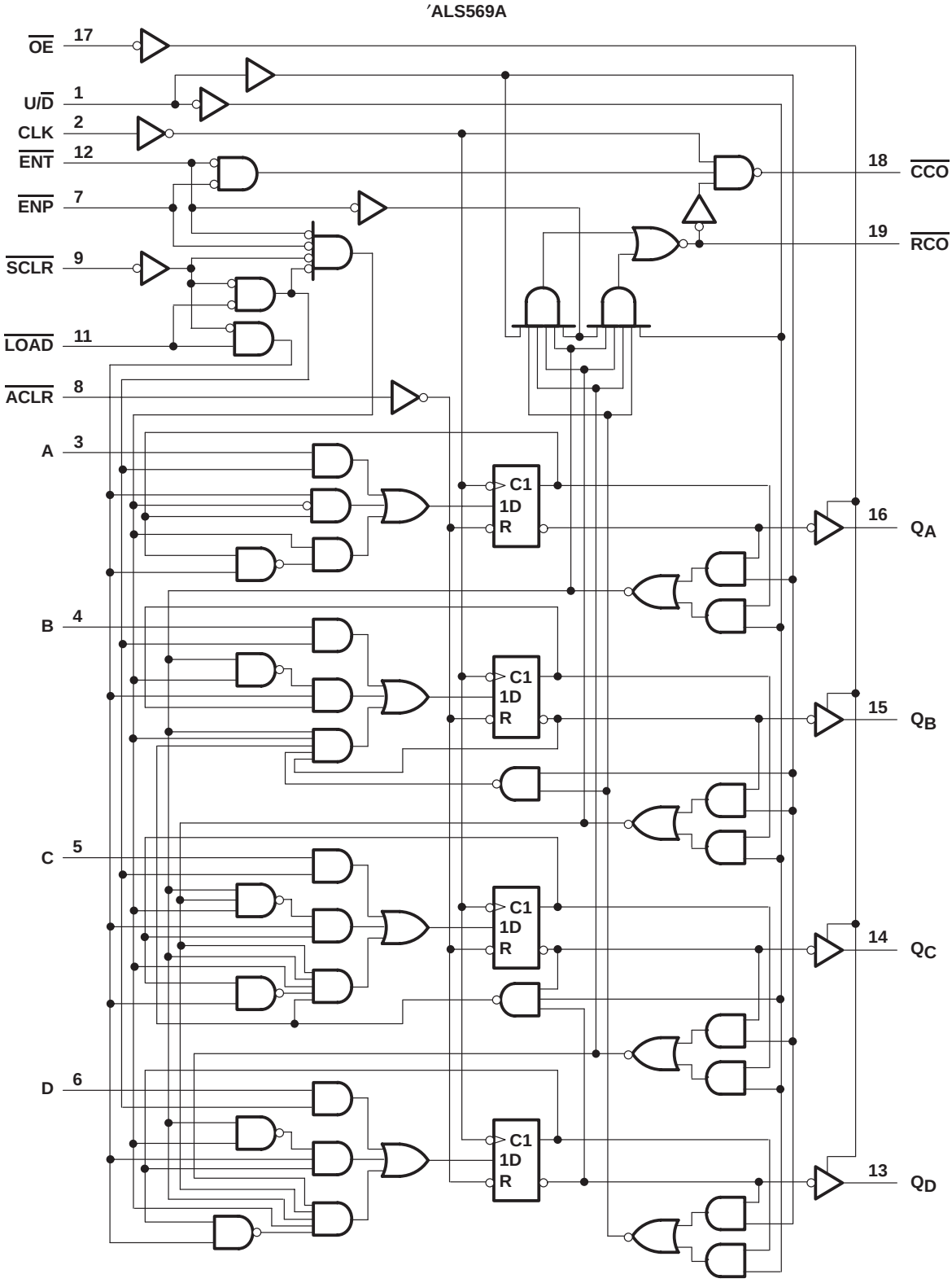

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagrams (positive logic)

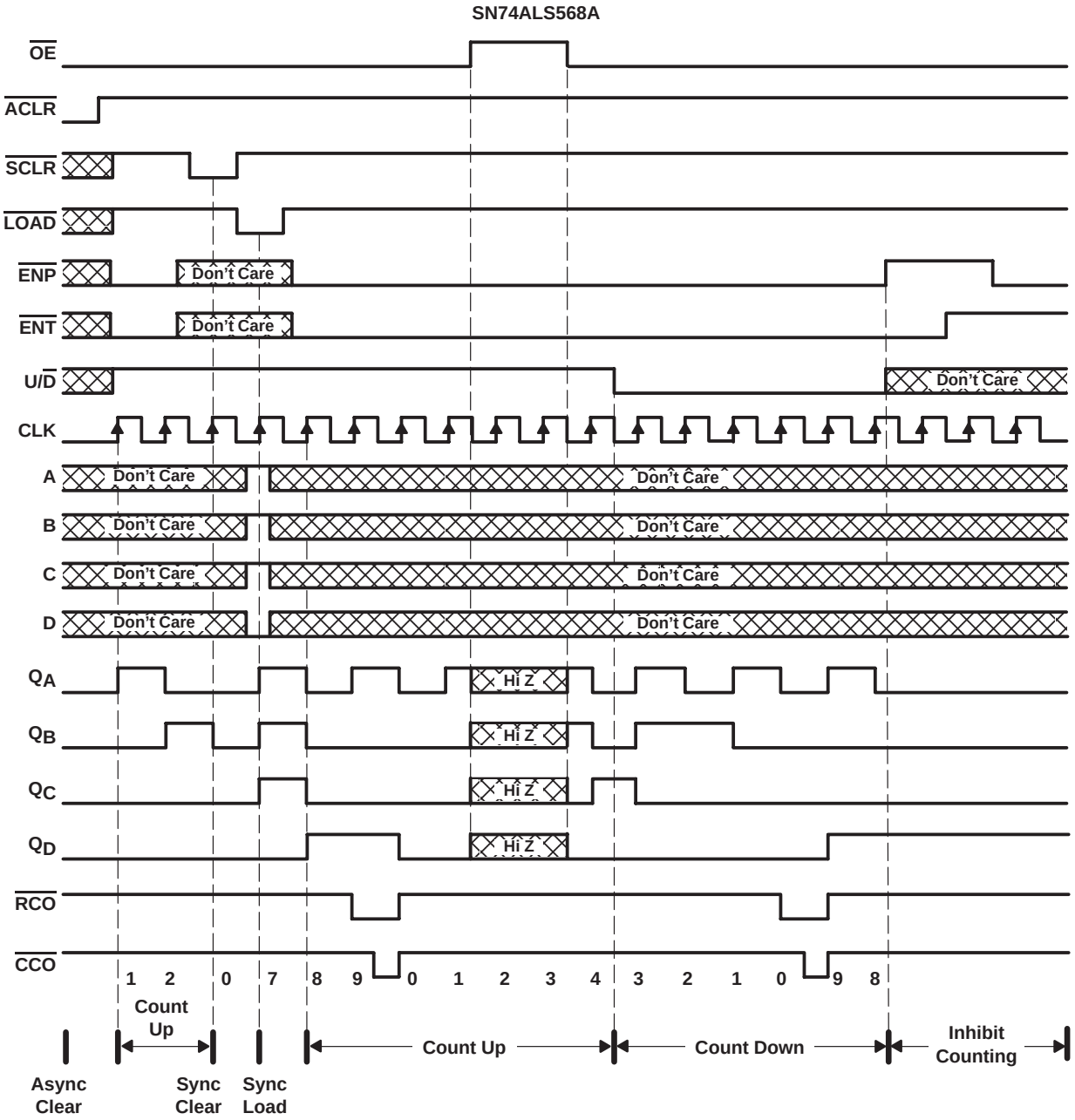
**SN74ALS568A**



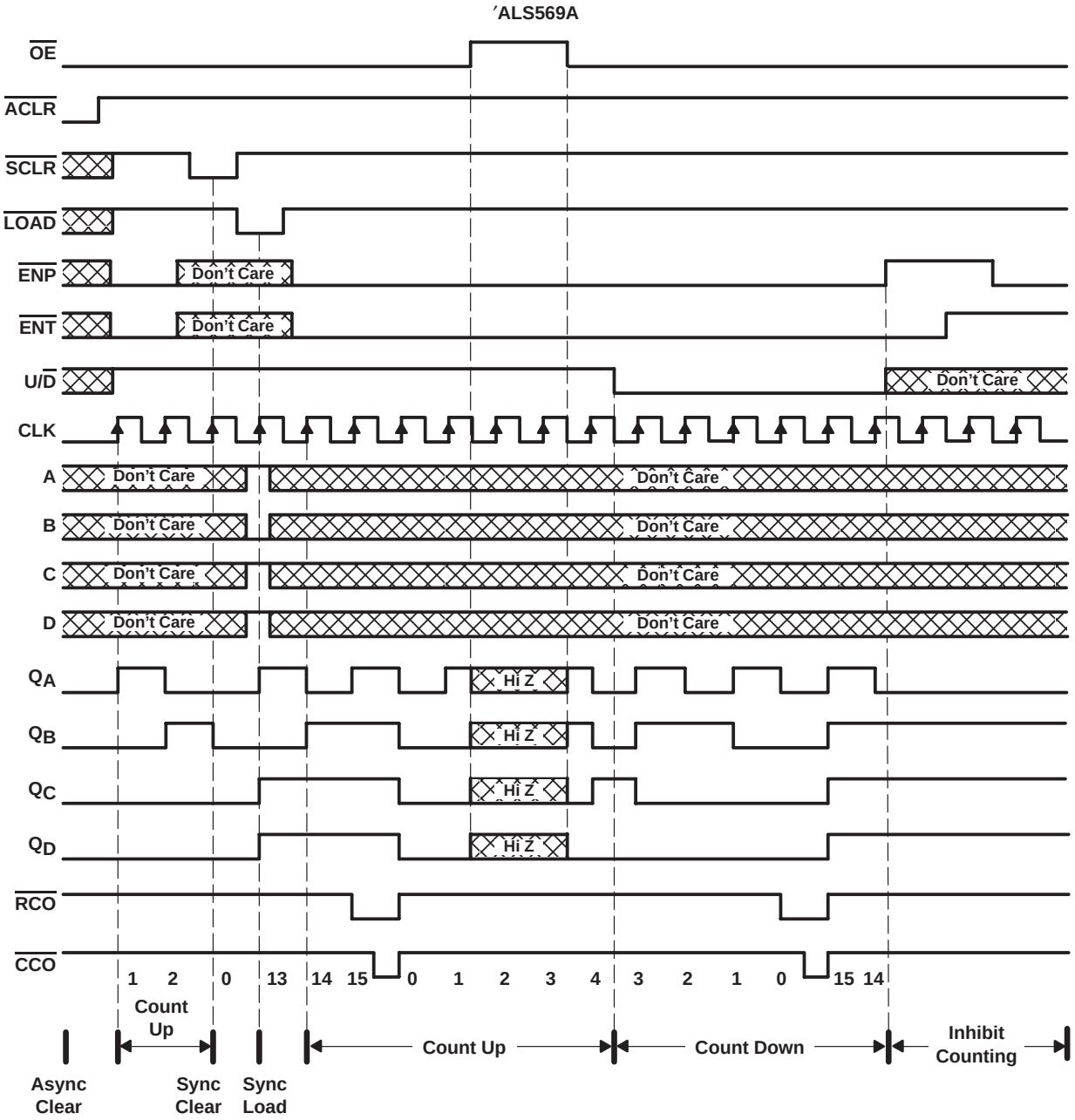
## logic diagrams (positive logic) (continued)



## typical load, count, and inhibit sequences



**typical load, count, and inhibit sequences (continued)**



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, $T_A$: SN54ALS569A . . . . . –55°C to 125°C
SN74ALS568A, SN74ALS569A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | | SN54ALS569A | | | SN74ALS568A SN74ALS569A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | Q outputs | | | | –1 | | | –2.6 | mA |
| | | $\overline{CCO}$ and $\overline{RCO}$ | | | | –0.4 | | | –0.4 | |
| $I_{OL}$ | Low-level output current | Q outputs | | | | 12 | | | 24 | mA |
| | | $\overline{CCO}$ and $\overline{RCO}$ | | | | 4 | | | 8 | |
| $f_{clock}$ | Clock frequency | SN74ALS568A | | | | | 0 | | 20 | MHz |
| | | ′ALS569A | | 0 | | 22 | 0 | | 30 | |
| $t_w$ | Pulse duration | $\overline{ACLR}$ or $\overline{LOAD}$ low | | 20 | | | 15 | | | ns |
| | | SN74ALS568A | CLK high | | | | 25 | | | |
| | | | CLK low | | | | 25 | | | |
| | | ′ALS569A | CLK high | 20 | | | 16.5 | | | |
| | | | CLK low | 23 | | | 16.5 | | | |
| $t_{su}$ | Setup time before CLK↑ | Data at A, B, C, D | | 25 | | | 20 | | | ns |
| | | $\overline{ENP}$, $\overline{ENT}$ | High | 35 | | | 30 | | | |
| | | | Low | 25 | | | 20 | | | |
| | | $\overline{SCLR}$ | Low | 20 | | | 15 | | | |
| | | | High (inactive) | 35 | | | 30 | | | |
| | | $\overline{LOAD}$ | Low | 20 | | | 15 | | | |
| | | | High (inactive) | 35 | | | 30 | | | |
| | | U/$\overline{D}$ | | 35 | | | 30 | | | |
| | | $\overline{ACLR}$ inactive | | 10 | | | 10 | | | |
| $t_h$ | Hold time after CLK↑ for any input | | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS569A | | | SN74ALS568A SN74ALS569A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | All outputs | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| | Q outputs | $V_{CC}$ = 4.5 V | $I_{OH}$ = –1 mA | 2.4 | 3.3 | | | | | |
| | | | $I_{OH}$ = –2.6 mA | | | | 2.4 | 3.2 | | |
| $V_{OL}$ | Q outputs | $V_{CC}$ = 4.5 V | $I_{OL}$ = 12 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | 0.35 | 0.5 | |
| | $\overline{CCO}$ and $\overline{RCO}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_{OZH}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0.4 V | | | –20 | | | –20 | µA |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.2 | | | –0.2 | mA |
| $I_O$‡ | $\overline{CCO}$ and $\overline{RCO}$ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –15 | | –70 | –15 | | –70 | mA |
| | Q outputs | | | –20 | | –112 | –30 | | –112 | |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | Outputs high | | 16 | 26 | | 16 | 26 | mA |
| | | | Outputs low | | 20 | 32 | | 20 | 32 | |
| | | | Outputs disabled | | 20 | 32 | | 20 | 32 | |

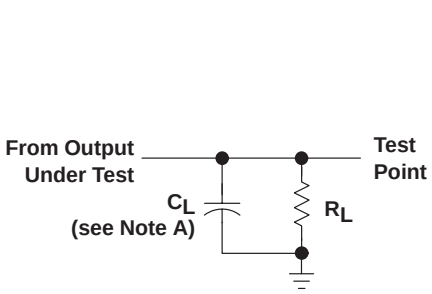
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

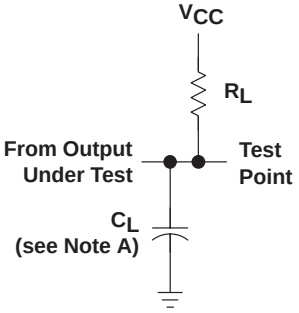
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, R1 = 500 Ω, R2 = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS569A | | SN74ALS568A SN74ALS569A | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | SN74ALS568A | | | | 20 | | MHz |
| | ′ALS569A | | 22 | | 30 | | |
| $t_{PLH}$ | CLK | Any Q | 4 | 21 | 4 | 13 | ns |
| $t_{PHL}$ | | | 7 | 19 | 7 | 16 | |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 12 | 37 | 12 | 28 | ns |
| $t_{PHL}$ | | | 10 | 28 | 10 | 19 | |
| $t_{PLH}$ | CLK | $\overline{CCO}$ | 5 | 17 | 5 | 13 | ns |
| $t_{PHL}$ | | | 6 | 30 | 6 | 25 | |
| $t_{PLH}$ | U/$\overline{D}$ | $\overline{RCO}$ | 9 | 31 | 9 | 23 | ns |
| $t_{PHL}$ | | | 9 | 33 | 9 | 19 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 6 | 21 | 6 | 15 | ns |
| $t_{PHL}$ | | | 4 | 20 | 4 | 13 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{CCO}$ | 5 | 18 | 5 | 13 | ns |
| $t_{PHL}$ | | | 9 | 32 | 9 | 23 | |
| $t_{PLH}$ | $\overline{ENP}$ | $\overline{CCO}$ | 4 | 18 | 4 | 12 | ns |
| $t_{PHL}$ | | | 5 | 18 | 5 | 14 | |
| $t_{PHL}$ | $\overline{ACLR}$ | Any Q | 9 | 25 | 9 | 20 | ns |
| $t_{PZH}$ | $\overline{OE}$ | Any Q | 6 | 23 | 6 | 18 | ns |
| $t_{PZL}$ | | | 6 | 29 | 6 | 24 | |
| $t_{PHZ}$ | $\overline{OE}$ | Any Q | 1 | 12 | 1 | 10 | ns |
| $t_{PLZ}$ | | | 3 | 29 | 3 | 13 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

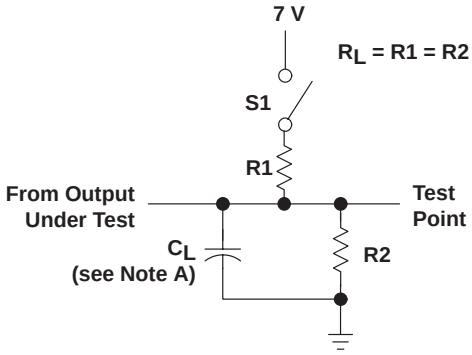
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



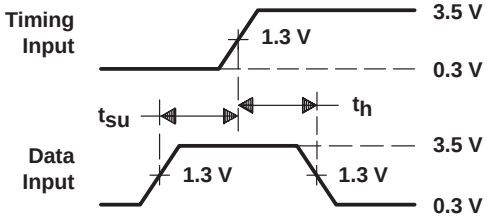

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



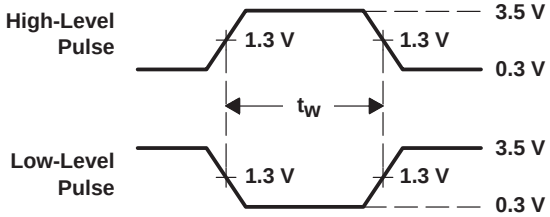

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



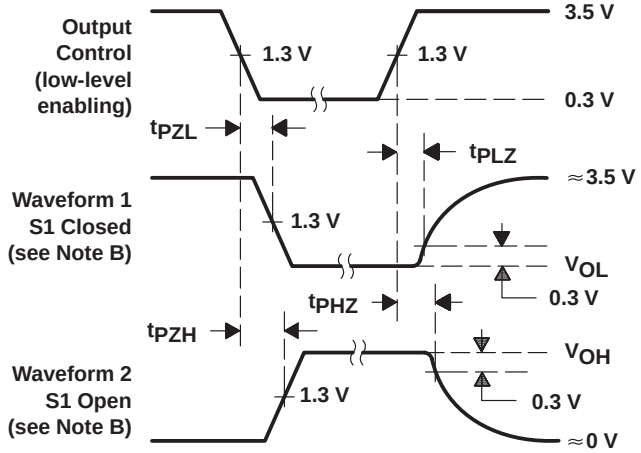

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



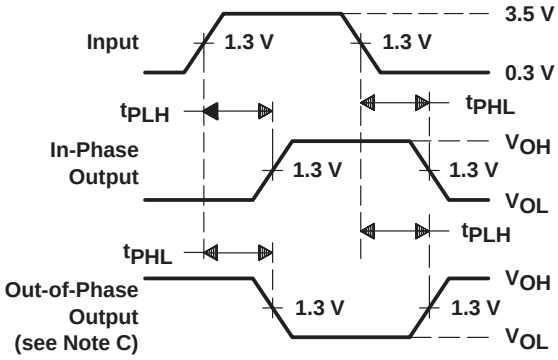

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 83025022A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83025022A SNJ54ALS 569AFK |
| 8302502RA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8302502RA SNJ54ALS569AJ |
| SN54ALS569AJ | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS569AJ |
| SN54ALS569AJ.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS569AJ |
| SN74ALS569ADWR | Last Time Buy | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS569A |
| SN74ALS569ADWR.A | Last Time Buy | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS569A |
| SN74ALS569AN | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS569AN |
| SN74ALS569AN.A | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS569AN |
| SNJ54ALS569AFK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83025022A SNJ54ALS 569AFK |
| SNJ54ALS569AFK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83025022A SNJ54ALS 569AFK |
| SNJ54ALS569AJ | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8302502RA SNJ54ALS569AJ |
| SNJ54ALS569AJ.A | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8302502RA SNJ54ALS569AJ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF SN54ALS569A, SN74ALS569A :**

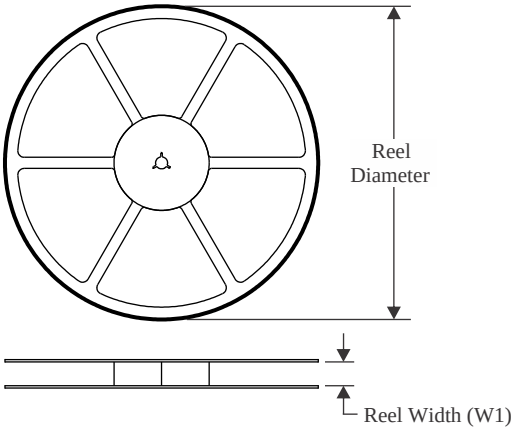
- Catalog : SN74ALS569A
- Military : SN54ALS569A

NOTE: Qualified Version Definitions:

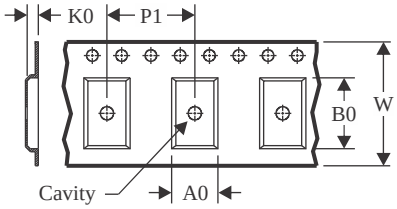
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

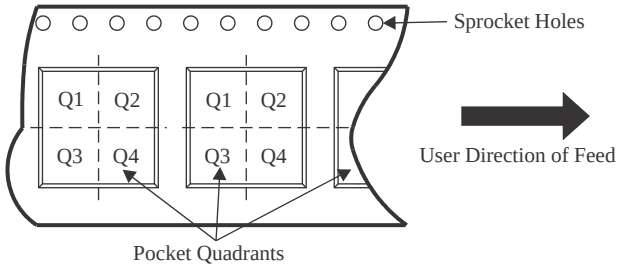



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

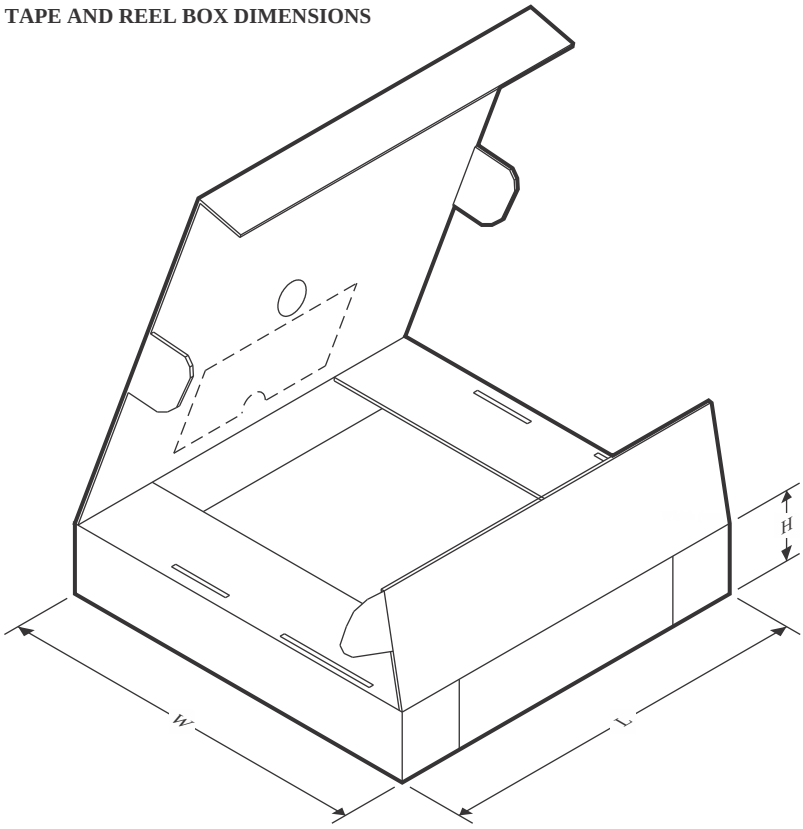
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS569ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

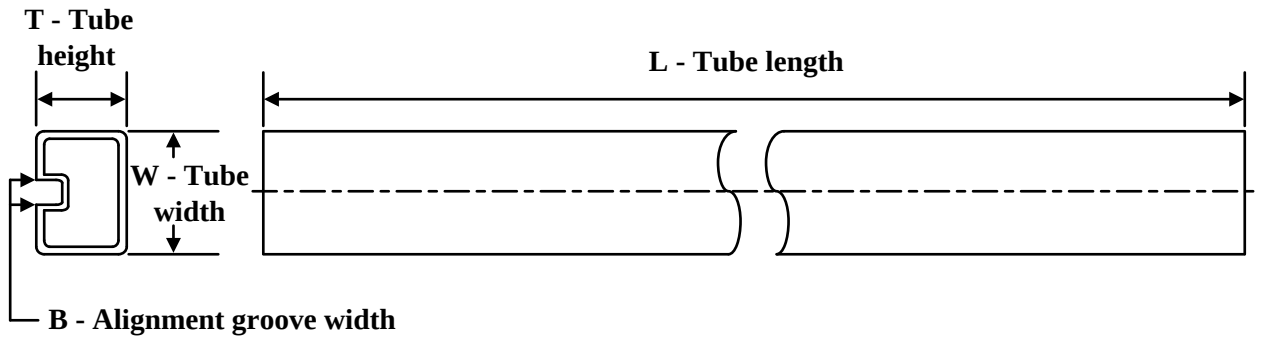
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALS569ADWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |

## TUBE



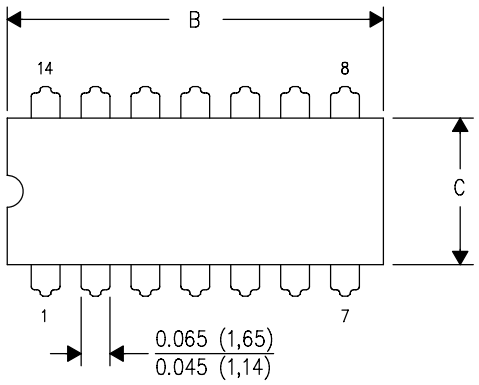

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 83025022A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74ALS569AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS569AN.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS569AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS569AFK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

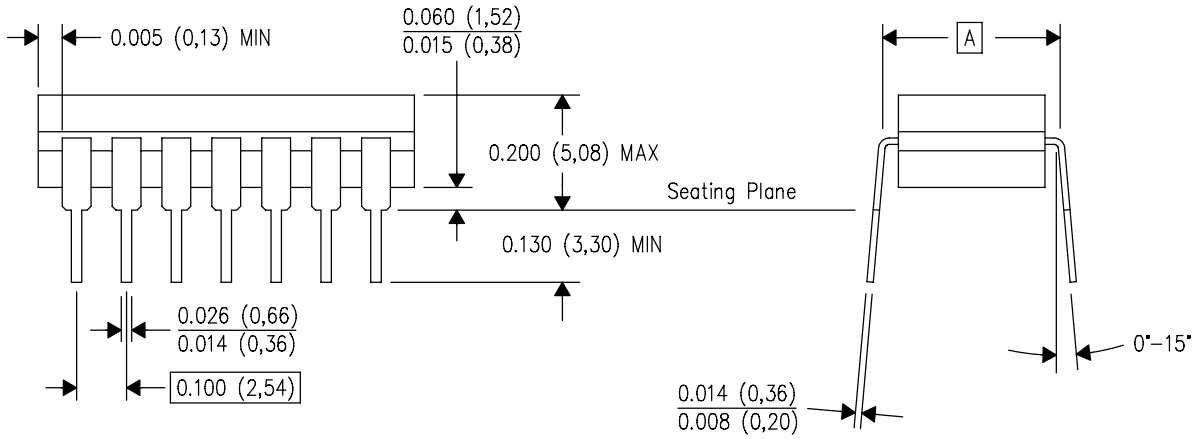
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

# GENERIC PACKAGE VIEW

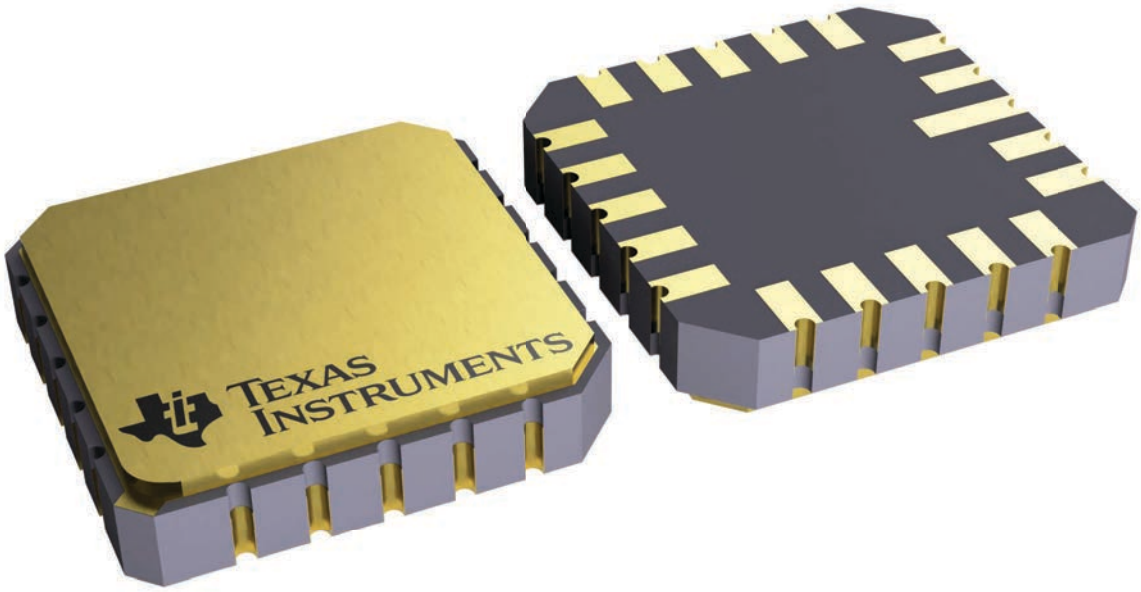
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

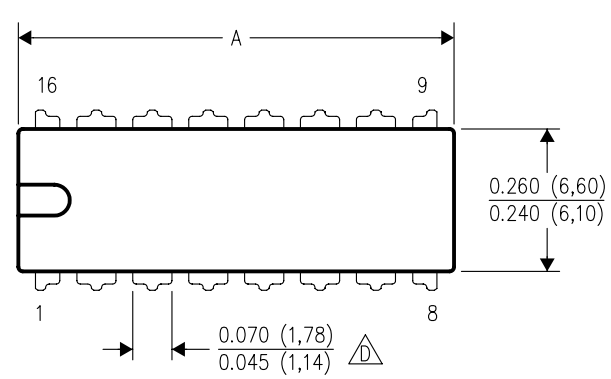



4229370VA\

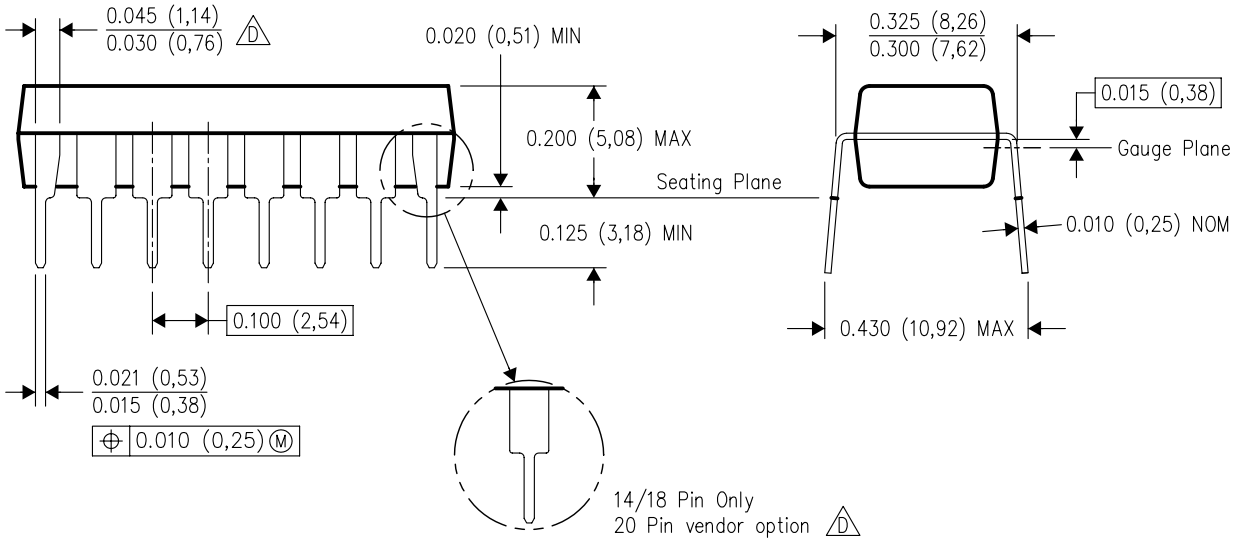
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

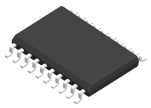



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

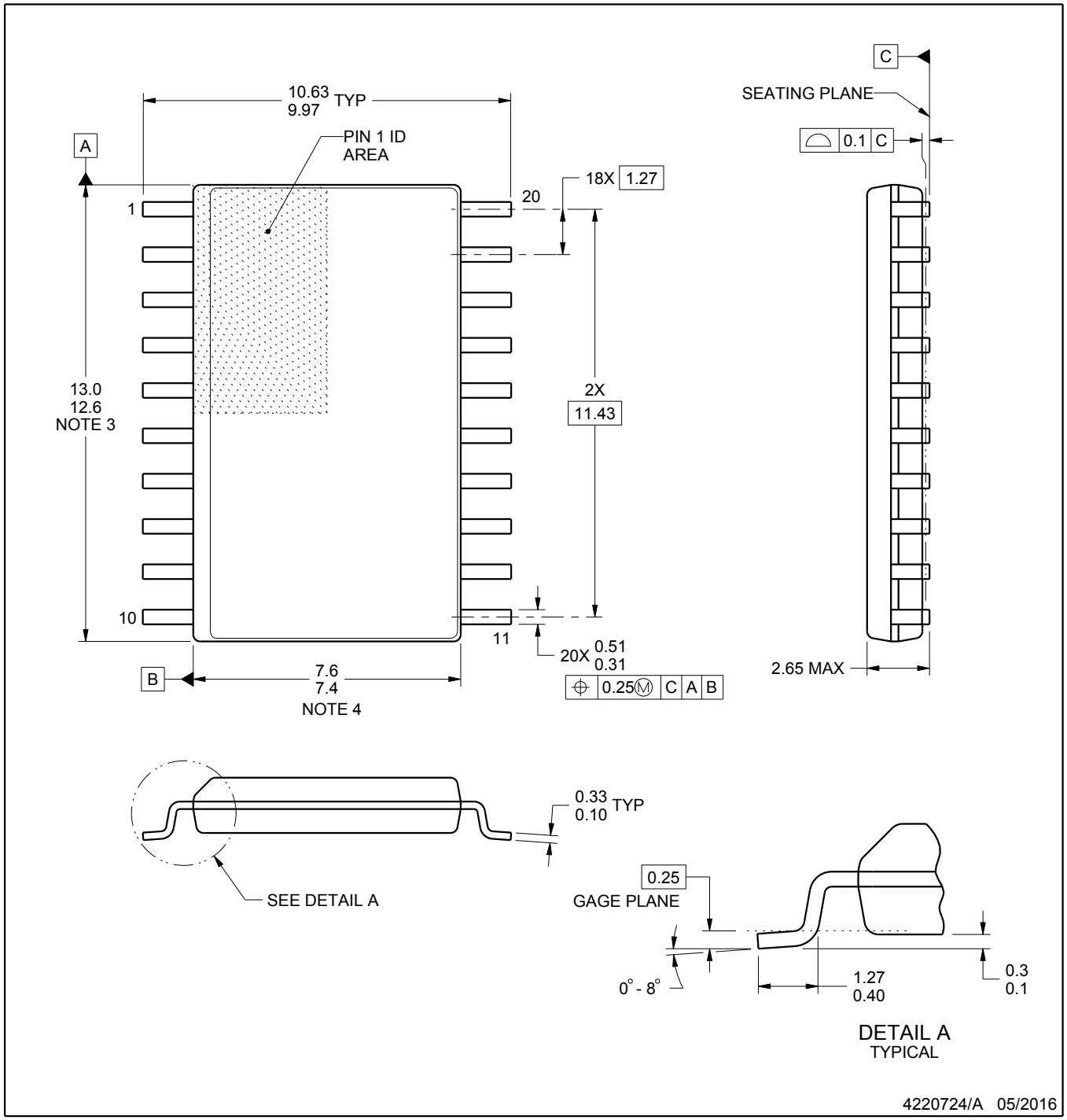


# PACKAGE OUTLINE

## DW0020A

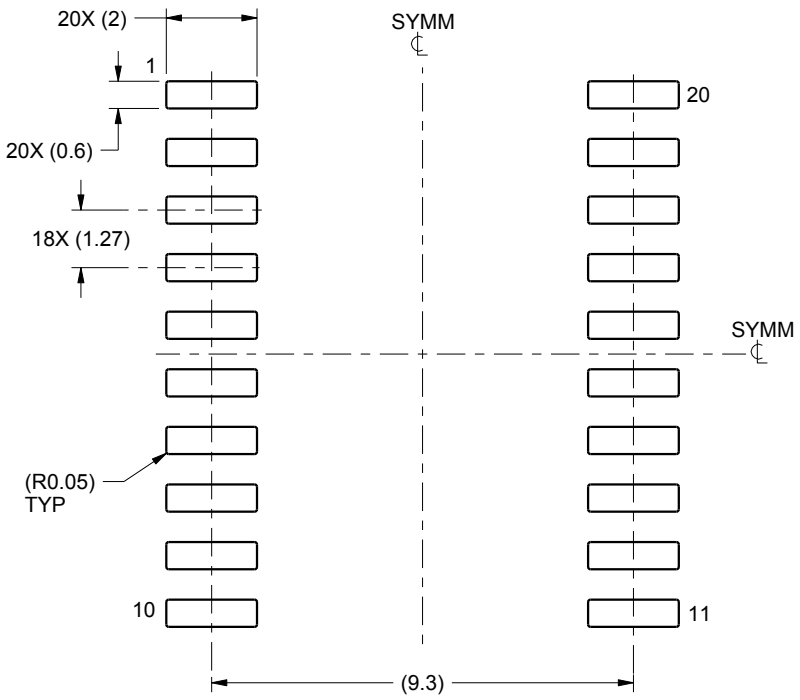
## SOIC - 2.65 mm max height

SOIC

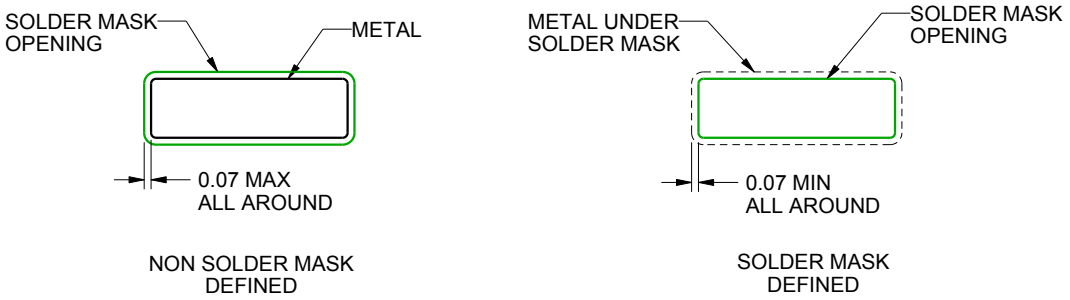



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

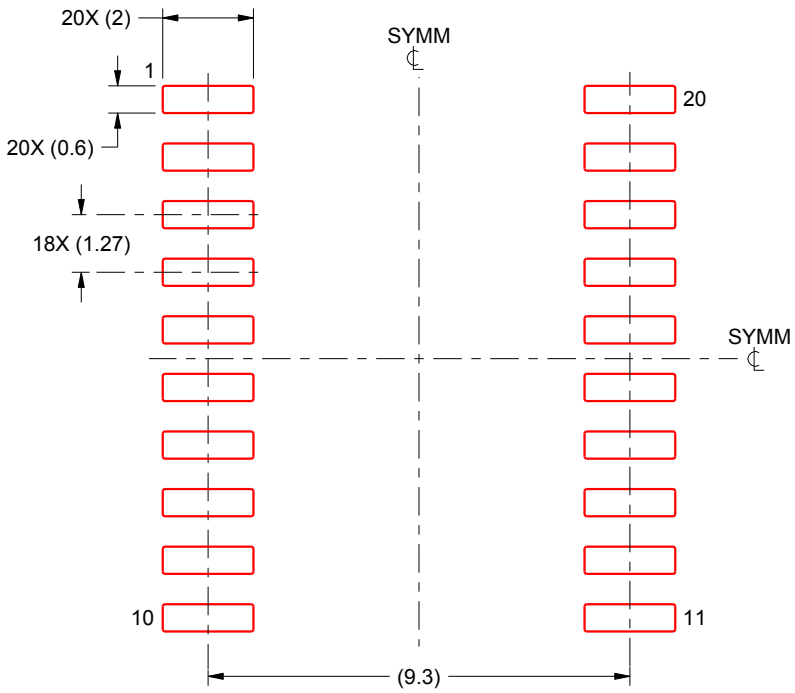



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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