

8-INPUT POSITIVE-NAND GATES

Check for Samples: [SN54ALS30A](#), [SN54AS30](#), [SN74ALS30A](#), [SN74AS30](#)

FEATURES

- 8-Input Positive-NAND Gates
- Available in J, DW, N, and FK Packages

DESCRIPTION

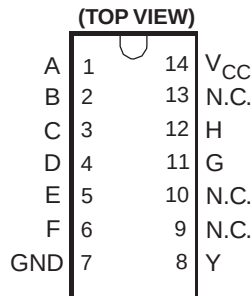
These devices contain an 8-input positive-NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$$

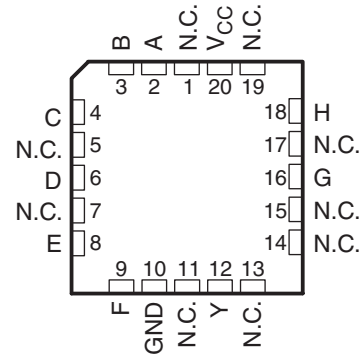
or

$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . DW OR N PACKAGE
SN74AS30 . . . DB PACKAGE



SN54ALS30A, SN54AS30 . . . FK PACKAGE
(TOP VIEW)



N.C. – No internal connection

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾ (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS30AN	SN74ALS30AN
			SN74AS30N	SN74AS30N
	SOIC – D	Tube	SN74AS30AD	ALS30A
		Tape and reel	SN74ALS30ADR	
		Tube	SN74AS30D	AS30
		Tape and reel	SN74AS30DR	
–55°C to 125°C	SSOP – DB	Tape and reel	SN74AS30DBR	AS30
	CDIP – J	Tube	SNJ54ALS30AJ	SNJ54ALS30AJ
			SNJ54AS30J	SNJ54AS30J
	LCCC –FK	Tube	SNJ54ALS30AFK	SNJ54ALS30AFK
			SNJ54AS30FK	SNJ54AS30FK

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

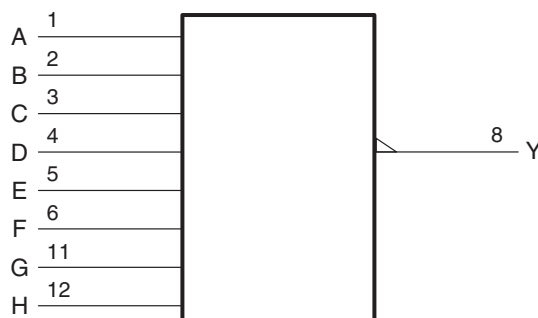
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



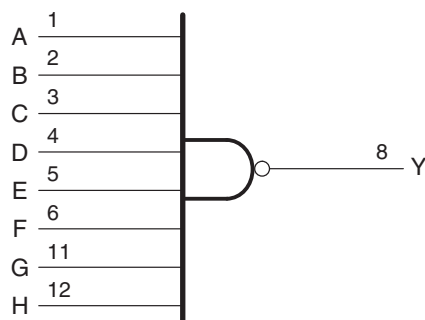
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 1. FUNCTION TABLE

INPUTS A–H	OUTPUT Y
All inputs H	L
One or more inputs L	H

LOGIC SYMBOL

- A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin number shown are for the D, DB, J, and N packages.

LOGIC DIAGRAM (POSITIVE LOGIC)

Pin number shown are for the D, DB, J, and N packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range	–0.5	7	V
θ_{JA}	Package thermal impedance ⁽²⁾	D package		86
		DB package		96
		N package		80
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8 ⁽¹⁾	V
				0.7 ⁽²⁾	
I_{OH}	High-level output current	'ALS30A		–0.4	mA
		'AS30		–2	
I_{OL}	Low-level output current	SN54ALS30A		4	mA
		SN74ALS30A		8	
		'AS30		20	
T_A	Operating free-air temperature	SN54ALS30A, SN54AS30		–55	°C
		SN74ALS30A, SN74AS30		0	

- (1) Applies to the 'AS30 and SN74ALS30A across the full operating temperature range, and SN54ALS30A over the temperature range of –55°C to 7°C.
- (2) Applies to the SN54ALS30A over the temperature range of 70°C to 125°C.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$	'ALS30A 'AS30		–1.5	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$,	$I_{OH} = -0.4\text{ mA}$	'ALS30A	$V_{CC} - 2$		V
		$I_{OH} = -2\text{ mA}$	'AS30	$V_{CC} - 2$		
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 4\text{ mA}$	'ALS30A	0.25	0.4	V
		$I_{OL} = 8\text{ mA}$	SN74ALS30A	0.35	0.5	
		$I_{OL} = 20\text{ mA}$	'AS30	0.35	0.5	
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	'ALS30A		–0.1	mA
			'AS30		–0.5	
$I_O^{(2)}$	$V_{CC} = 5.5\text{ V}$,	$V_O = 2.25\text{ V}$	SN54ALS30A	–20	–112	mA
			SN74ALS30A	–30	–112	
			'AS30	–30	–112	
I_{CCH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0\text{ V}$	'ALS30A	0.22	0.36	mA
			'AS30	0.9	1.5	
I_{CCL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 4.5\text{ V}$	'ALS30A	0.54	0.9	mA
			'AS30	3	4.9	

- (1) All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
- (2) The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SWITCHING CHARACTERISTICS

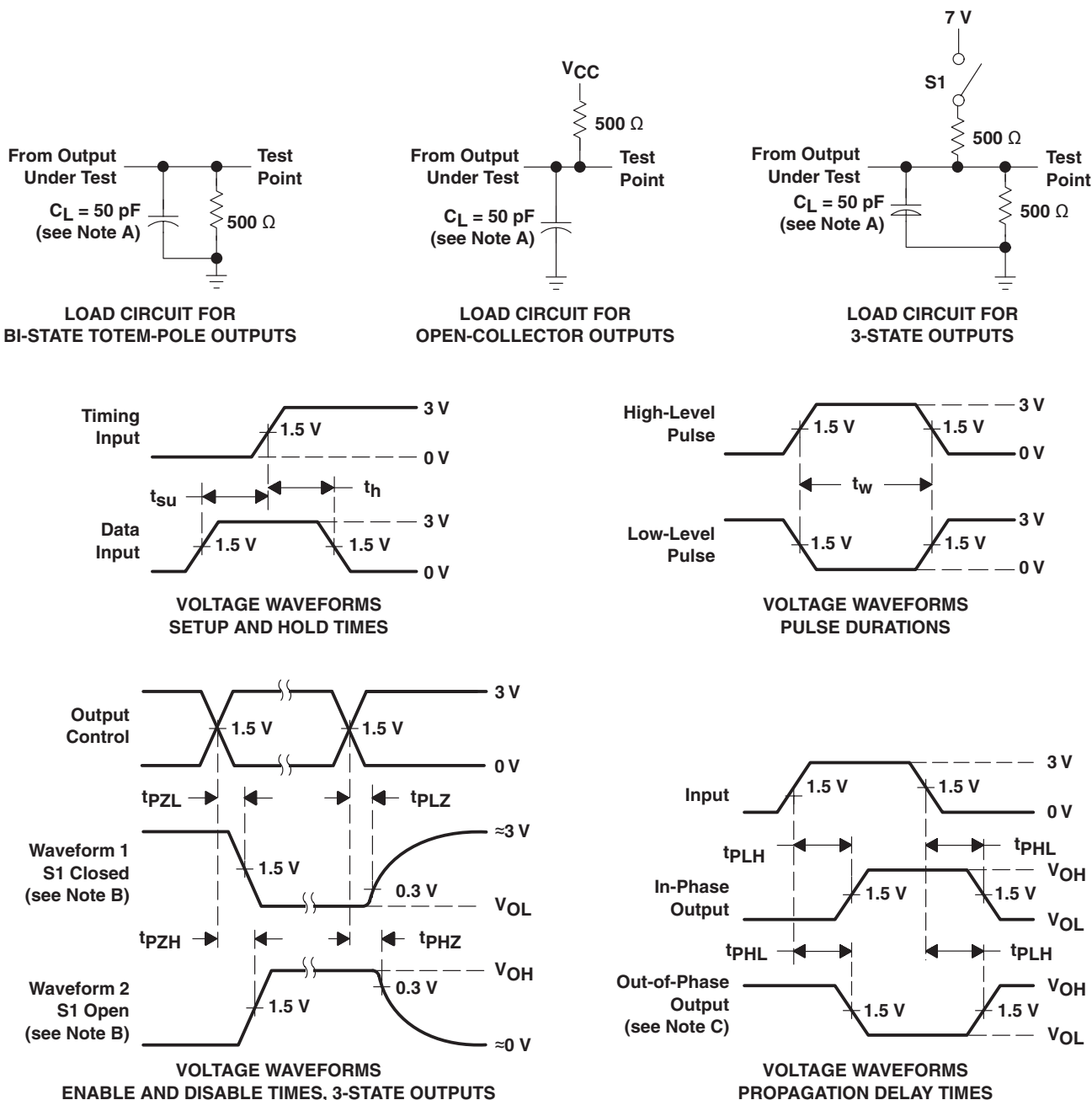
over recommended operating conditions (unless otherwise noted (see [Figure 1](#)))

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t_{PLH}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	10	
			SN54AS30	1	5.5	
			SN74AS30	1	5	

SWITCHING CHARACTERISTICS (continued)over recommended operating conditions (unless otherwise noted (see [Figure 1](#)))

PARAMETER	FROM (INPUT)	TO (OUTPUT)		MIN	MAX	UNIT
t_{PHL}	A, B, C, D, E, F, G, or H	Y	SN54ALS30A	3	15	ns
			SN74ALS30A	3	12	
			SN54AS30	1	5	
			SN74AS30	1	4.5	

PARAMETER MEASUREMENT INFORMATION



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

REVISION HISTORY

Changes from Original (April 2009) to Revision E	Page
• Updated ORDERING INFORMATION table.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-86837012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 86837012A SNJ54ALS 30AFK	Samples
5962-8683701DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8683701DA SNJ54ALS30AW	Samples
5962-9755801QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9755801QC A SNJ54AS30J	Samples
JM38510/37004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Non-Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37004B2A	Samples
JM38510/37004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37004BCA	Samples
M38510/37004B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37004B2A	Samples
M38510/37004BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 37004BCA	Samples
SN54ALS30AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54ALS30AJ	Samples
SN74ALS30ADB	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		G30A	Samples
SN74ALS30ADBE4	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		G30A	Samples
SN74ALS30ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS30A	Samples
SN74ALS30AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS30AN	Samples
SN74AS30DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS30	Samples
SN74AS30N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74AS30N	Samples
SNJ54ALS30AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 86837012A SNJ54ALS 30AFK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54ALS30AJ	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54ALS30AJ	Samples
SNJ54ALS30AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8683701DA SNJ54ALS30AW	Samples
SNJ54AS30J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9755801QC A SNJ54AS30J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

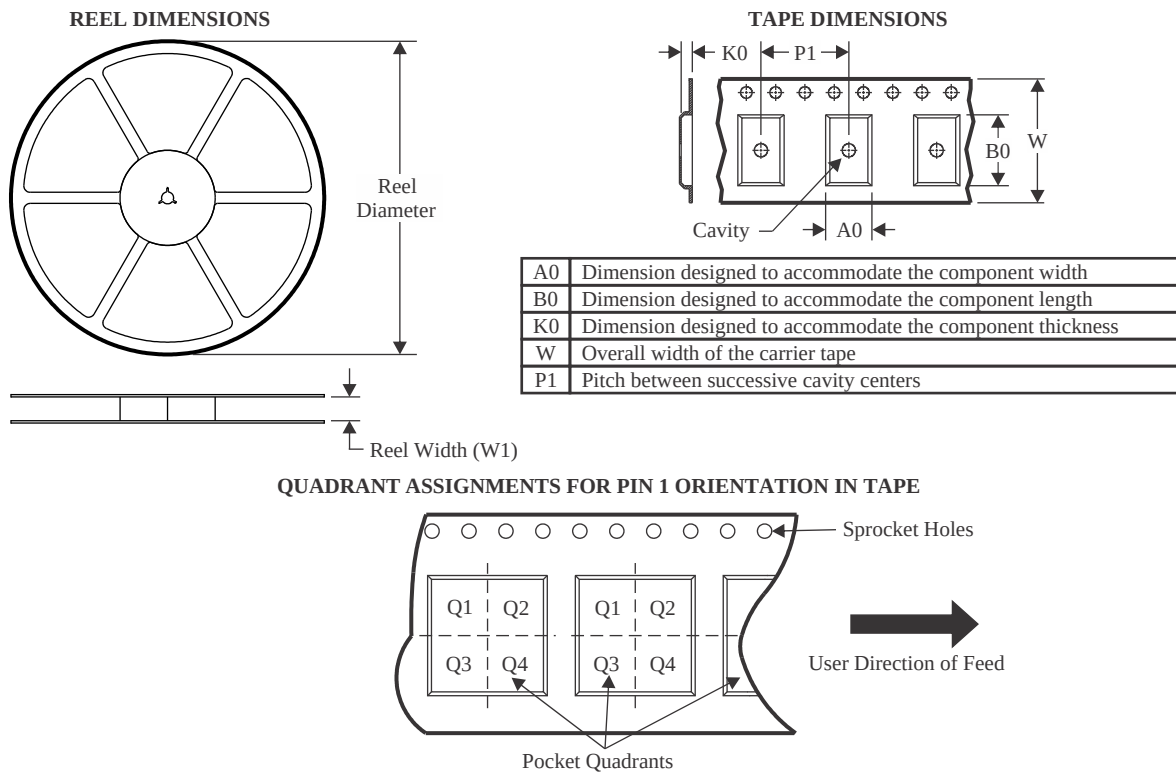
OTHER QUALIFIED VERSIONS OF SN54ALS30A, SN54AS30, SN74ALS30A, SN74AS30 :

- Catalog : [SN74ALS30A](#), [SN74AS30](#)
- Military : [SN54ALS30A](#), [SN54AS30](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

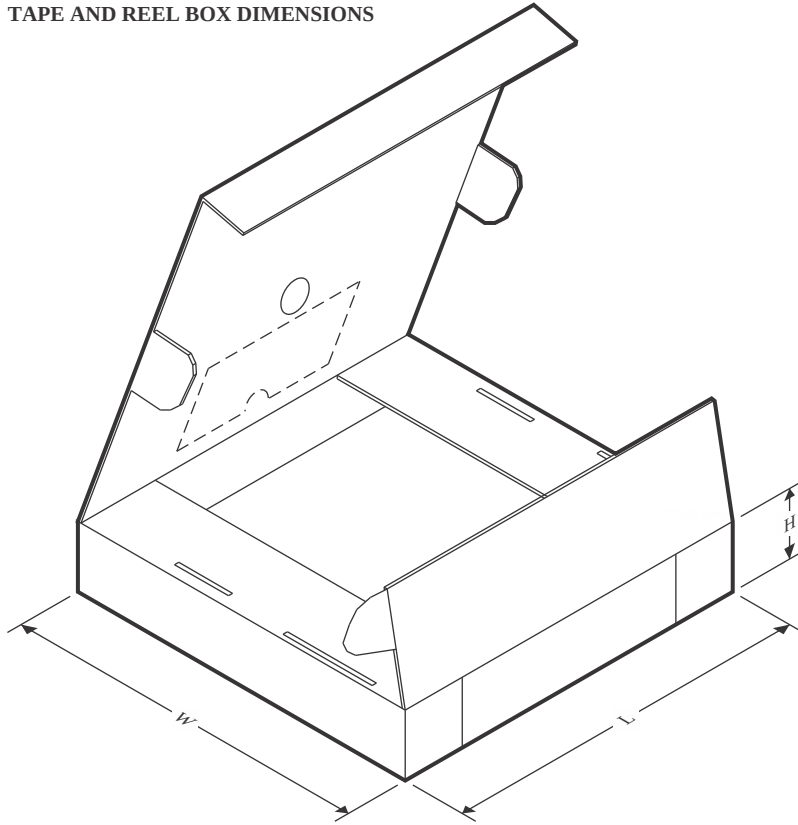
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS30ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AS30DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

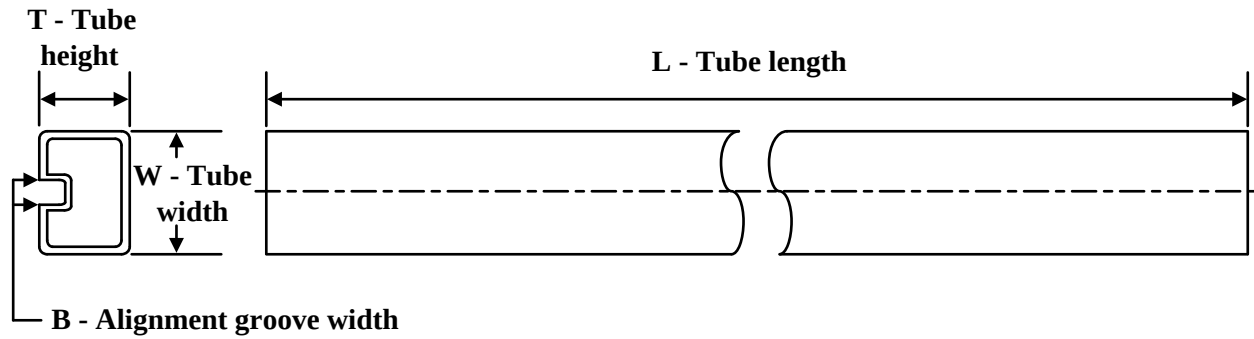
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS30ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AS30DR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE

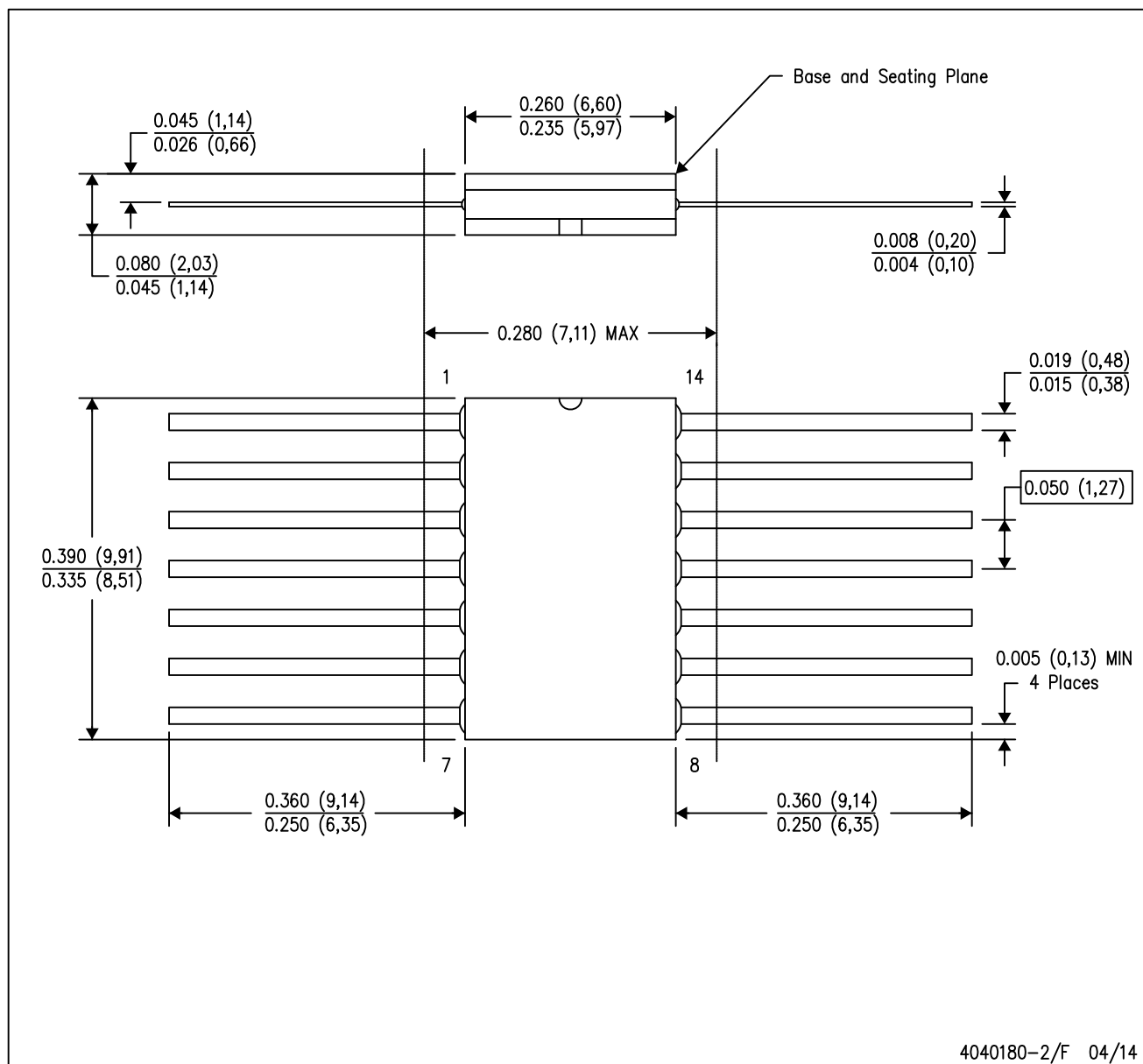


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-86837012A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8683701DA	W	CFP	14	25	506.98	26.16	6220	NA
JM38510/37004B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37004B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS30ADB	DB	SSOP	14	80	530	10.5	4000	4.1
SN74ALS30ADBE4	DB	SSOP	14	80	530	10.5	4000	4.1
SN74ALS30AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS30AN	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS30N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AS30N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ALS30AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS30AW	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

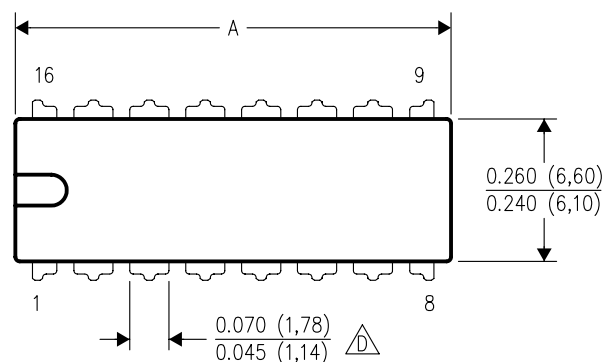
CERAMIC DUAL FLATPACK



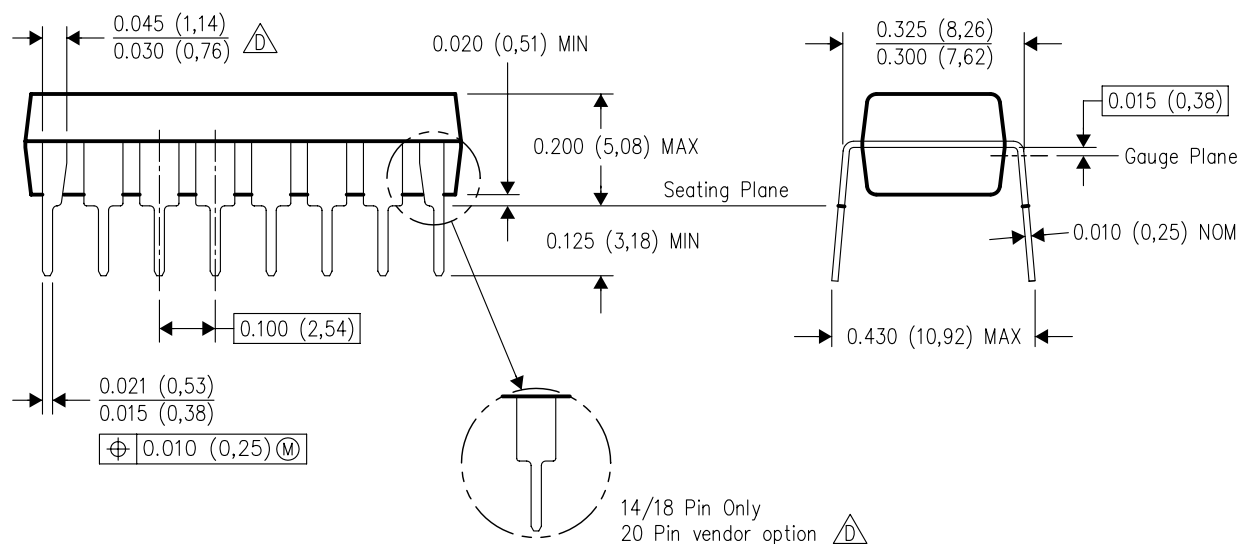
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



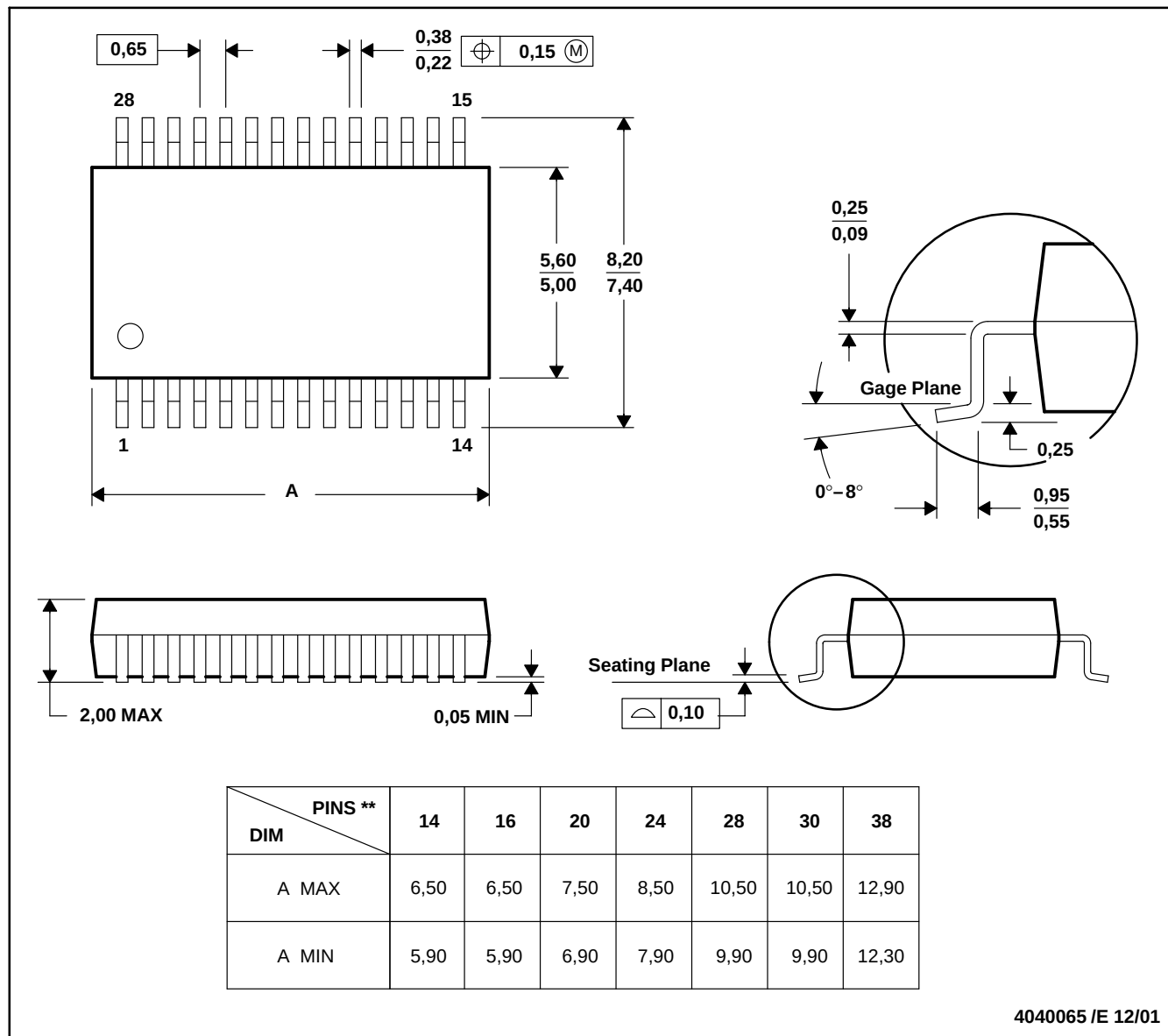
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

GENERIC PACKAGE VIEW

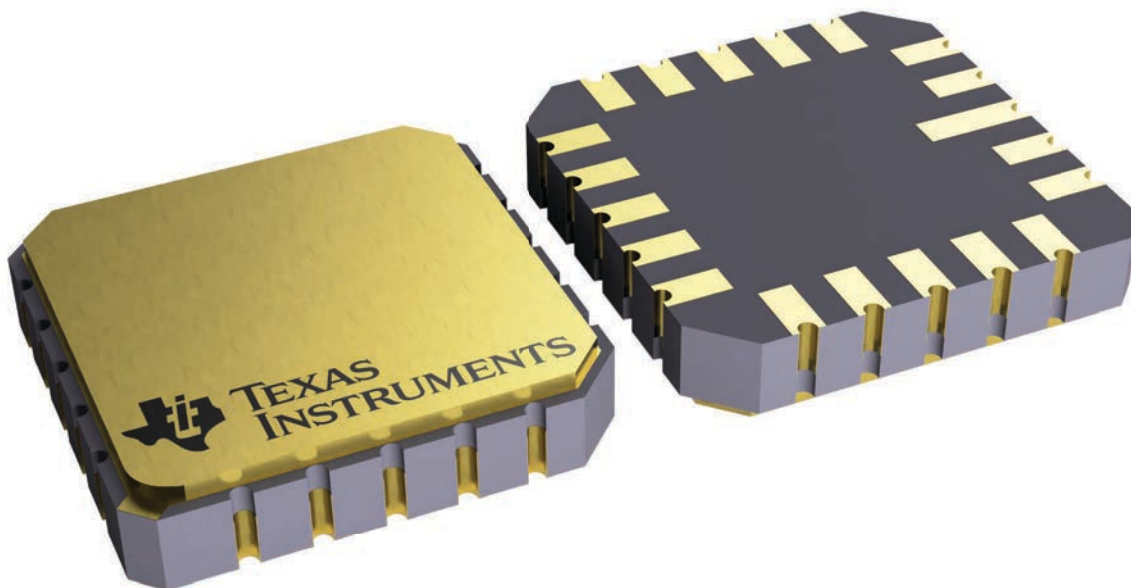
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



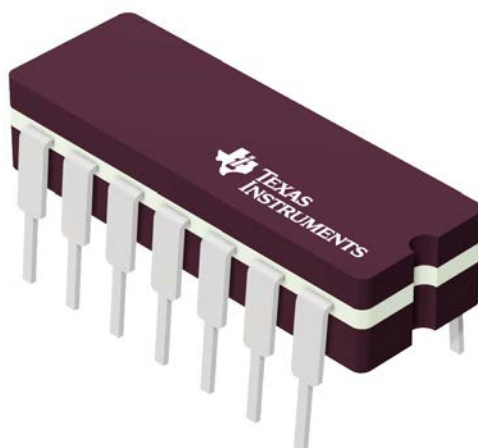
4229370VA\

J 14

GENERIC PACKAGE VIEW

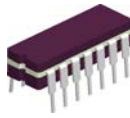
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

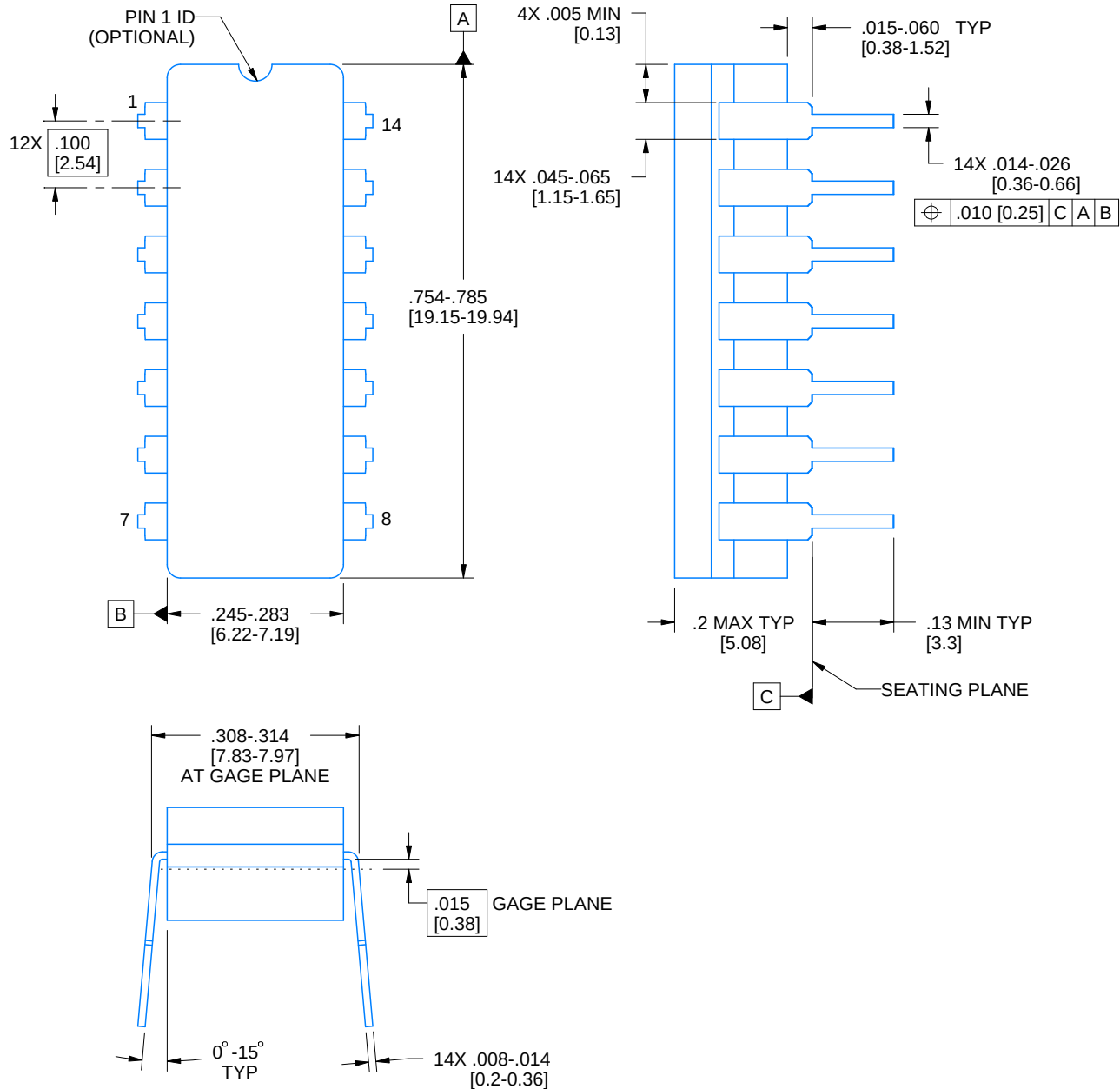


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



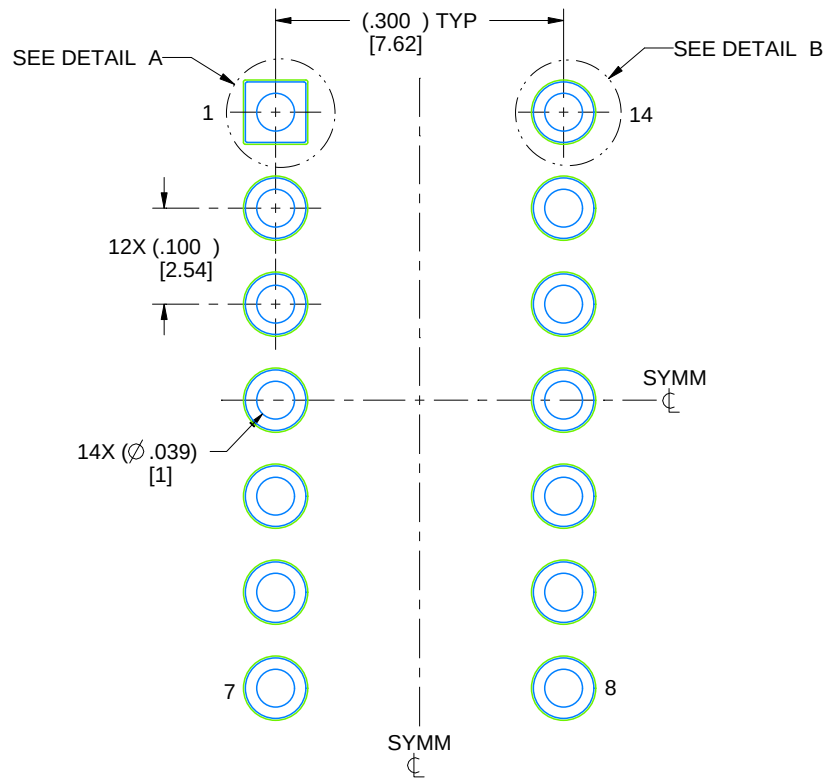
**TEXAS
INSTRUMENTS**
www.ti.com

EXAMPLE BOARD LAYOUT

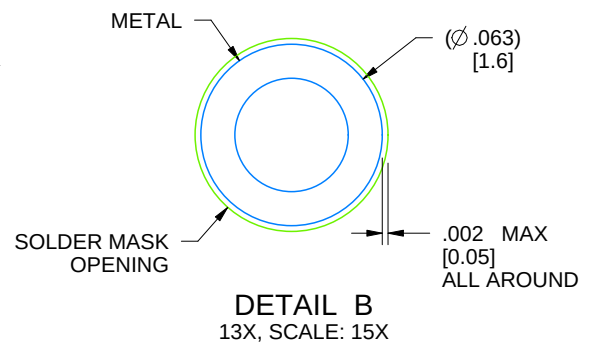
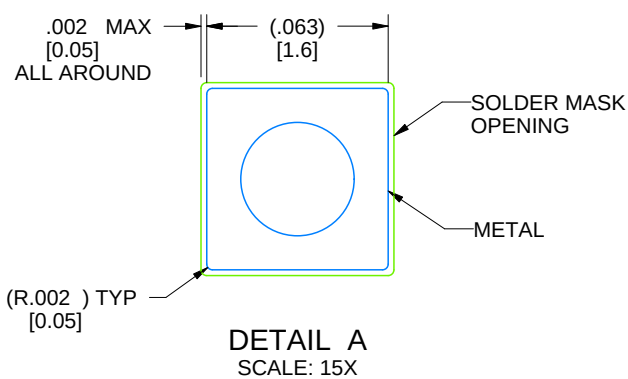
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



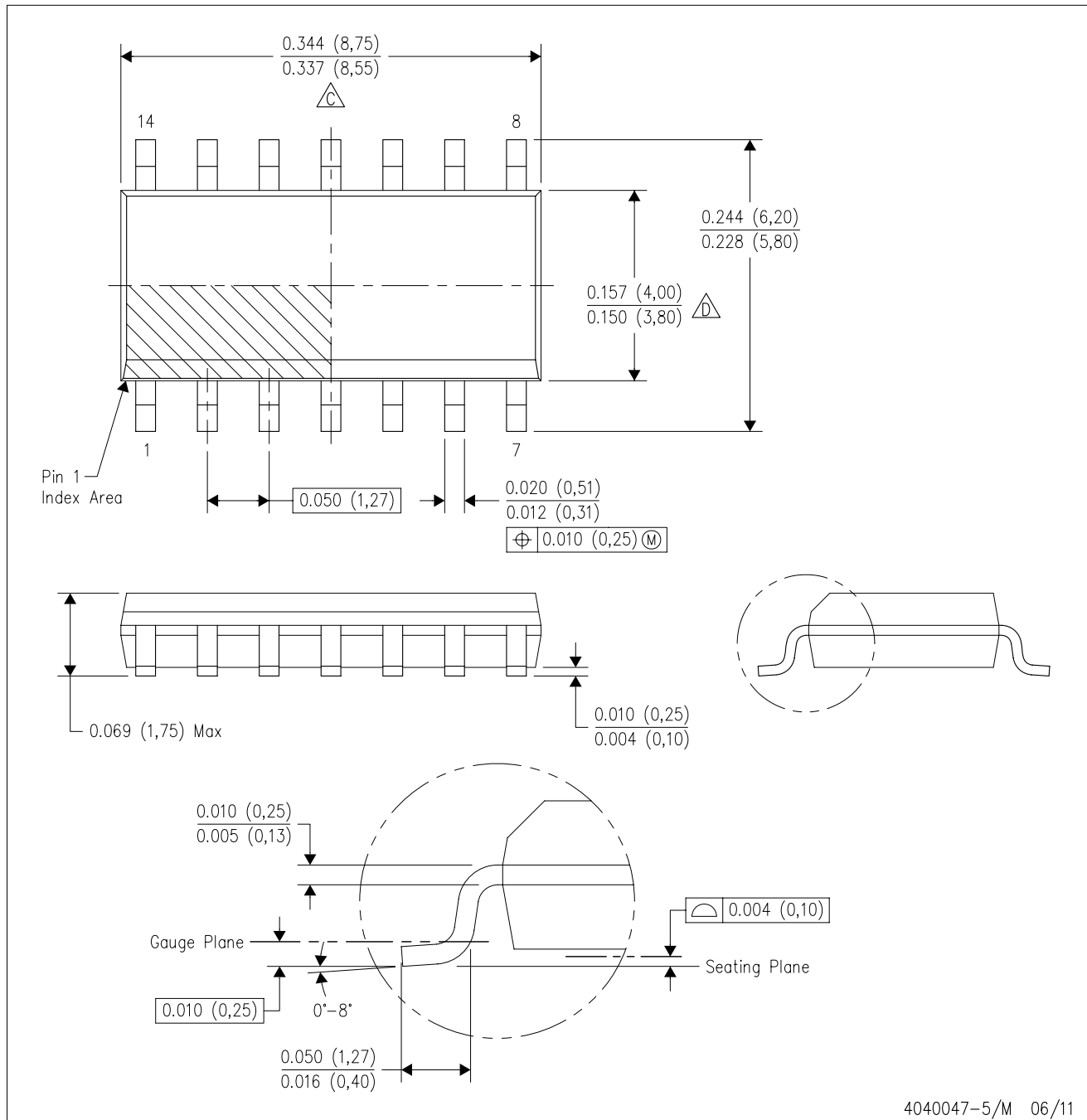
LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

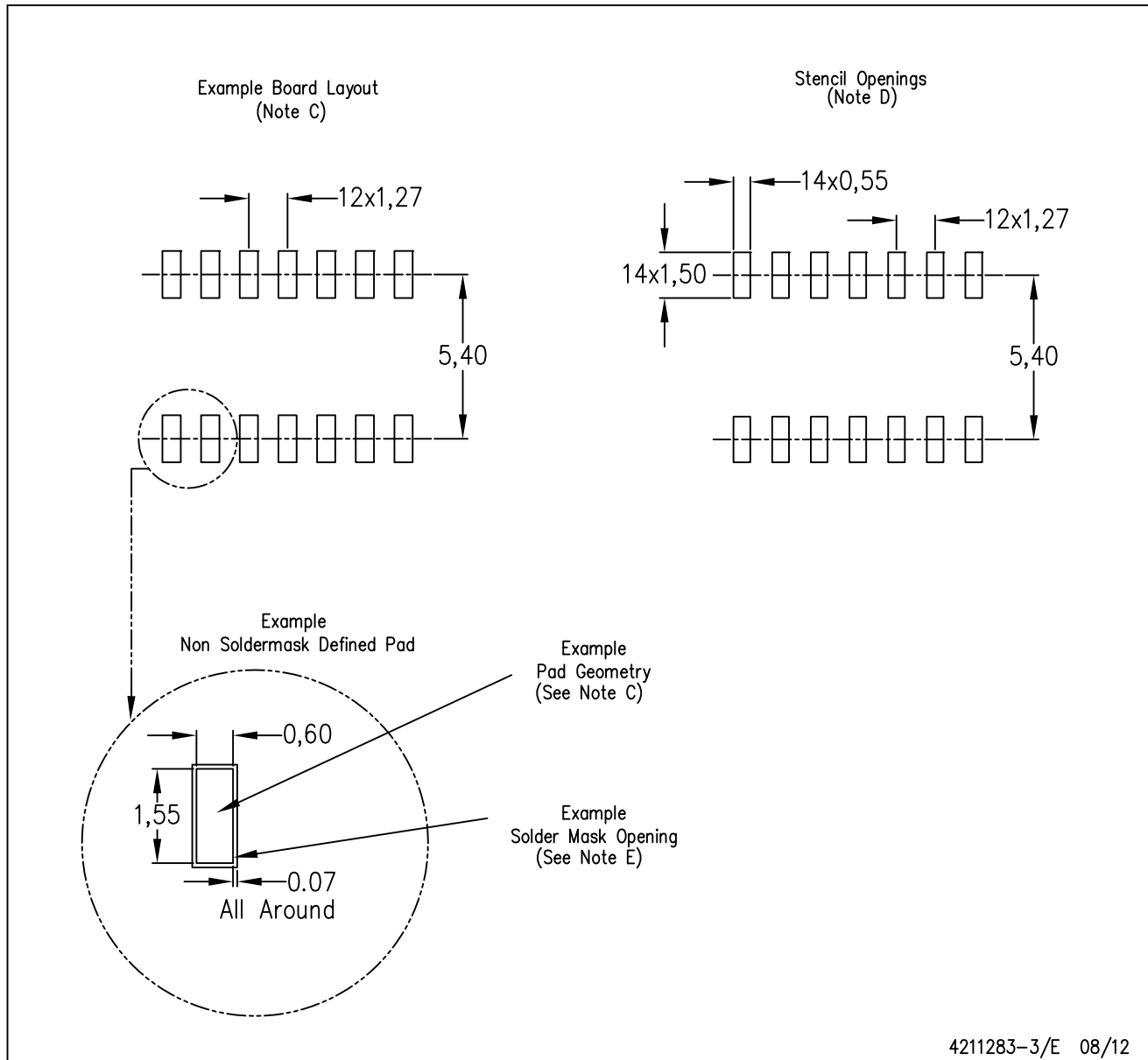
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated