

SNx4HC109 Dual J- \bar{K} Positive-Edge-Triggered Flip-Flops With Clear and Preset

1 Features

- Wide operating voltage range of 2 V to 6 V
- Low input current of 1 μ A max
- High-current outputs drive up to 10 LSTTL loads
- Low power consumption, 40- μ A max I_{CC}
- Typical $t_{pd} = 12$ ns
- ± 4 -mA output drive at 5 V

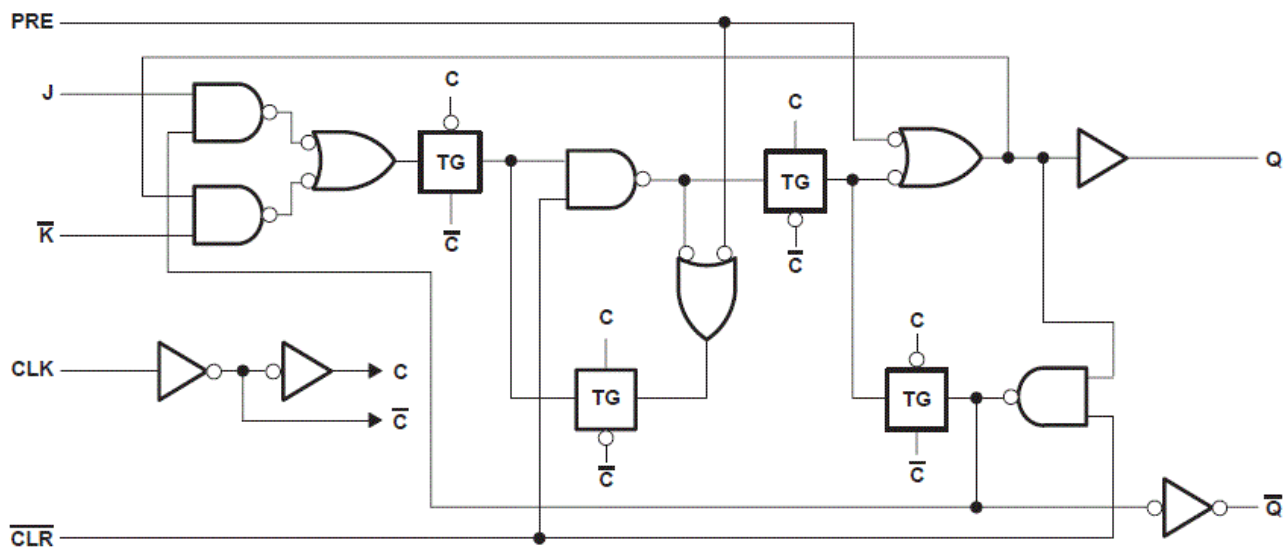
2 Description

These devices contain two independent J- \bar{K} positive-edge-triggered flip-flops. A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the J and \bar{K} inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the J and \bar{K} inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding \bar{K} and tying J high. They also can perform as D-type flip-flops if J and \bar{K} are tied together.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|--------------|------------------------|---------------------------|
| SN54HC109J | CDIP (16) | 24.38 mm \times 6.92 mm |
| SN74HC109D | SOIC (16) | 9.90 mm \times 3.90 mm |
| SN74HC109N | PDIP (16) | 19.31 mm \times 6.35 mm |
| SN74HC109NS | SO (16) | 6.20 mm \times 5.30 mm |
| SNJ54HC109FK | LCCC (20) | 8.89 mm \times 8.45 mm |
| SNJ54HC109W | CFP (16) | 10.16 mm \times 6.73 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



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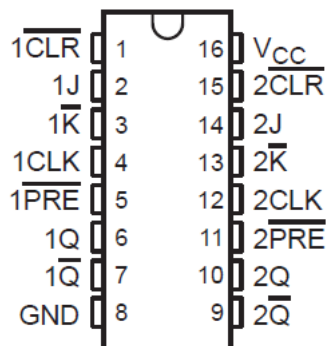
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3 Revision History

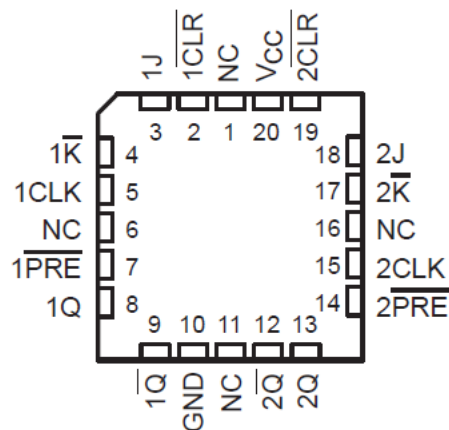
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (February 2022) to Revision C (June 2022) | Page |
|--|-------------|
| <ul style="list-style-type: none"> Junction-to-ambient thermal resistance values increased. D was 73 is now 117.2, N was 67 is now 60.5, NS was 64 is now 88.3..... | 4 |
| Changes from Revision A (October 2003) to Revision B (February 2022) | Page |
| <ul style="list-style-type: none"> Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | 1 |

4 Pin Configuration and Functions



J, W, D, N, or NS Package
16-Pin CDIP, CFP, SOIC, PDIP, or SO
Top View



NC - No internal connection

FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------|--|-----------------------------|------|-----|------|
| V_{CC} | Supply voltage range | | –0.5 | 7 | V |
| I_{IK} | Input clamp current | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ±35 | mA |
| | Continuous current through V_{CC} or GND | | | ±70 | mA |
| | Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds | FK package | | 300 | °C |
| | | J package | | | |
| | | W package | | | |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | D package | | 260 | °C |
| | | N package | | | |
| | | NS package | | | |
| T_J | Junction temperature | | | 150 | °C |
| T_{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions⁽¹⁾

| | | | SN54HC109 | | | SN74HC109 | | | UNIT |
|---------------------|---------------------------------|------------------|-----------|-----|----------|-----------|-----|----------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | 1.5 | | | 1.5 | | | V |
| | | $V_{CC} = 4.5$ V | 3.15 | | | 3.15 | | | |
| | | $V_{CC} = 6$ V | 4.2 | | | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | | 0.3 | | | 0.5 | V |
| | | $V_{CC} = 4.5$ V | | | 0.9 | | | 1.35 | |
| | | $V_{CC} = 6$ V | | | 1.2 | | | 1.8 | |
| V_I | Input voltage | | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise/fall time | $V_{CC} = 2$ V | | | 1000 | | | 1000 | ns |
| | | $V_{CC} = 4.5$ V | | | 500 | | | 500 | |
| | | $V_{CC} = 6$ V | | | 400 | | | 400 | |
| T_A | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

| THERMAL METRIC | | D (SOIC) | N (PDIP) | NS (SO) | UNIT |
|----------------------|---|----------|----------|---------|------|
| | | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽¹⁾ | 117.2 | 60.5 | 88.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.2 | 47.9 | 45.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 75.6 | 40.4 | 50.9 | °C/W |

5.3 Thermal Information (continued)

| THERMAL METRIC | | D (SOIC) | N (PDIP) | NS (SO) | UNIT |
|----------------------|--|----------|----------|---------|------|
| | | 16 PINS | 16 PINS | 16 PINS | |
| Ψ_{JT} | Junction-to-top characterization parameter | 38.1 | 27.3 | 12.9 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 75.3 | 40.2 | 50.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC109 | | SN74HC109 | | UNIT |
|-----------|---------------------------------------|----------------------------|------------|--------------------------|-----------|-----------|-----------|------------|-----------|------------|---------------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V_{OH} | $V_I = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -20 \mu\text{A}$ | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | $I_{OH} = -4 \text{ mA}$ | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | $I_{OH} = -5.2 \text{ mA}$ | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V_{OL} | $V_I = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 20 \mu\text{A}$ | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL} = 4 \text{ mA}$ | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | $I_{OL} = 5.2 \text{ mA}$ | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I_I | $V_I = V_{CC} \text{ or } 0$ | | 6 V | | ± 0.1 | ± 100 | | ± 1000 | | ± 1000 | nA |
| I_{CC} | $V_I = V_{CC} \text{ or } 0, I_O = 0$ | | 6 V | | | 4 | | 80 | | 40 | μA |
| C_i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | | V_{CC} | $T_A = 25^\circ\text{C}$ | | SN54HC109 | | SN74HC109 | | UNIT |
|--------------------|-----------------|------------------------------------|----------|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | | 2 V | | 6 | | 4.2 | | 5 | MHz |
| | | | 4.5 V | | 31 | | 21 | | 25 | |
| | | | 6 V | | 36 | | 25 | | 29 | |
| t_w | Pulse duration | PRE or $\overline{\text{CLR}}$ low | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | CLK high or low | 2 V | 80 | | 120 | | 100 | | |
| | | | 4.5 V | 16 | | 24 | | 20 | | |
| | | | 6 V | 14 | | 20 | | 17 | | |

over recommended operating free-air temperature range (unless otherwise noted)

| | | | V _{CC} | T _A = 25°C | | SN54HC109 | | SN74HC109 | | UNIT |
|-----------------|-------------------------|---|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{su} | Setup time before CLK ↑ | Data (J, \overline{K}) | 2 V | 100 | | 150 | | 125 | | ns |
| | | | 4.5 V | 20 | | 30 | | 25 | | |
| | | | 6 V | 17 | | 25 | | 21 | | |
| | | \overline{PRE} or \overline{CLR} inactive | 2 V | 25 | | 40 | | 30 | | |
| | | | 4.5 V | 5 | | 8 | | 6 | | |
| | | | 6 V | 4 | | 7 | | 5 | | |
| t _h | Hold time | Data after CLK↑ | 2 V | 0 | | 0 | | 0 | | ns |
| | | | 4.5 V | 0 | | 0 | | 0 | | |
| | | | 6 V | 0 | | 0 | | 0 | | |

5.6 Switching Characteristics

 over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 6-1](#))

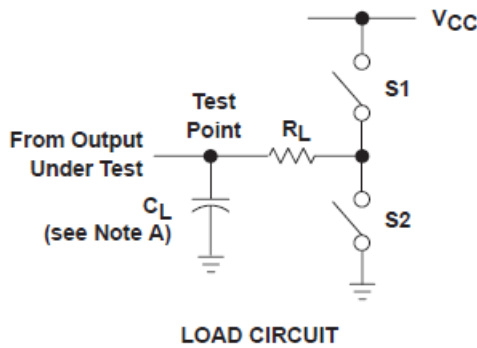
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC109 | | SN74HC109 | | UNIT |
|-----------|--------------------------------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 2 V | 6 | 10 | | 4.2 | | 5 | | ns |
| | | | 4.5 V | 31 | 50 | | 21 | | 25 | | |
| | | | 6 V | 36 | 60 | | 25 | | 29 | | |
| t_{pd} | \overline{PRE} or \overline{CLR} | Q or \bar{Q} | 2 V | | 60 | 230 | | 345 | | 290 | ns |
| | | | 4.5 V | | 15 | 46 | | 69 | | 58 | |
| | | | 6 V | | 12 | 39 | | 59 | | 49 | |
| | CLK | Q or \bar{Q} | 2 V | | 50 | 175 | | 250 | | 220 | |
| | | | 4.5 V | | 15 | 35 | | 50 | | 44 | |
| | | | 6 V | | 12 | 30 | | 42 | | 37 | |
| t_t | | Q or \bar{Q} | 2 V | | 28 | 75 | | 110 | | 95 | ns |
| | | | 4.5 V | | 8 | 15 | | 22 | | 19 | |
| | | | 6 V | | 6 | 13 | | 19 | | 16 | |

5.7 Operating Characteristics

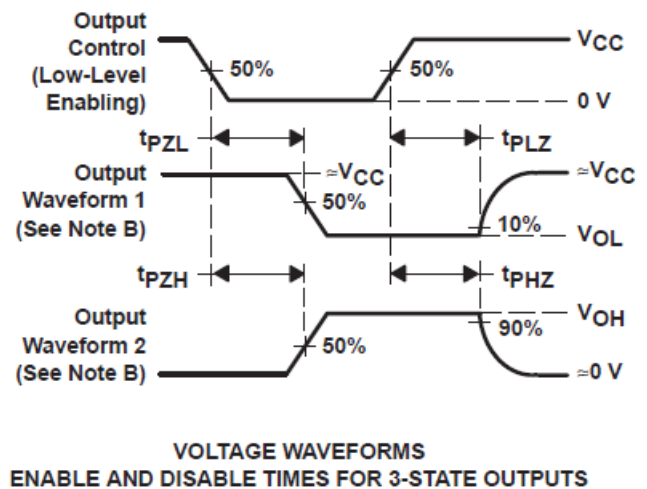
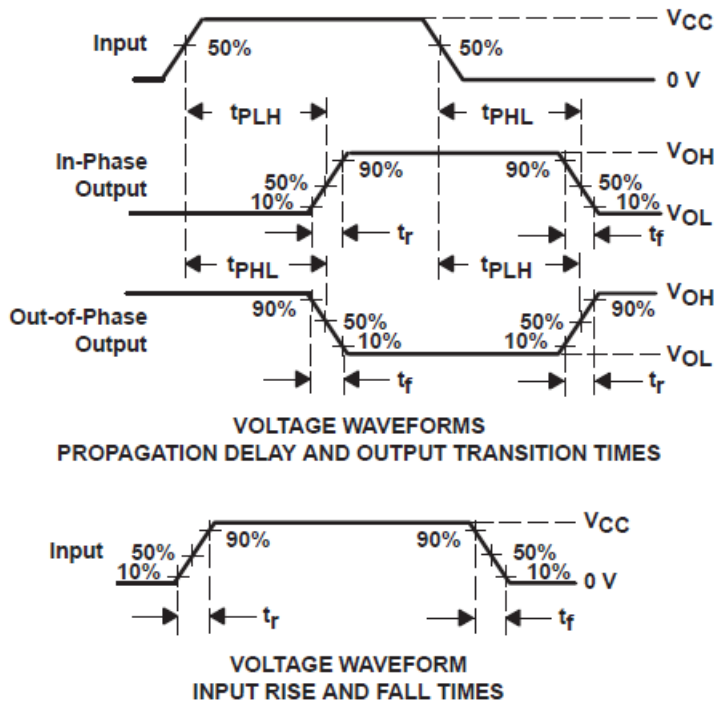
 $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|-----------------|-----|------|
| C_{pd} | Power dissipation capacitance per buffer/driver | No load | 35 | pF |

6 Parameter Measurement Information



| PARAMETER | | R_L | C_L | S1 | S2 |
|-------------------|-----------|--------------|-----------------|--------|--------|
| t_{en} | t_{PZH} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | t_{PZL} | | | Closed | Open |
| t_{dis} | t_{PHZ} | 1 k Ω | 50 pF | Open | Closed |
| | t_{PLZ} | | | Closed | Open |
| t_{pd} or t_t | | -- | 50 pF or 150 pF | Open | Open |



- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

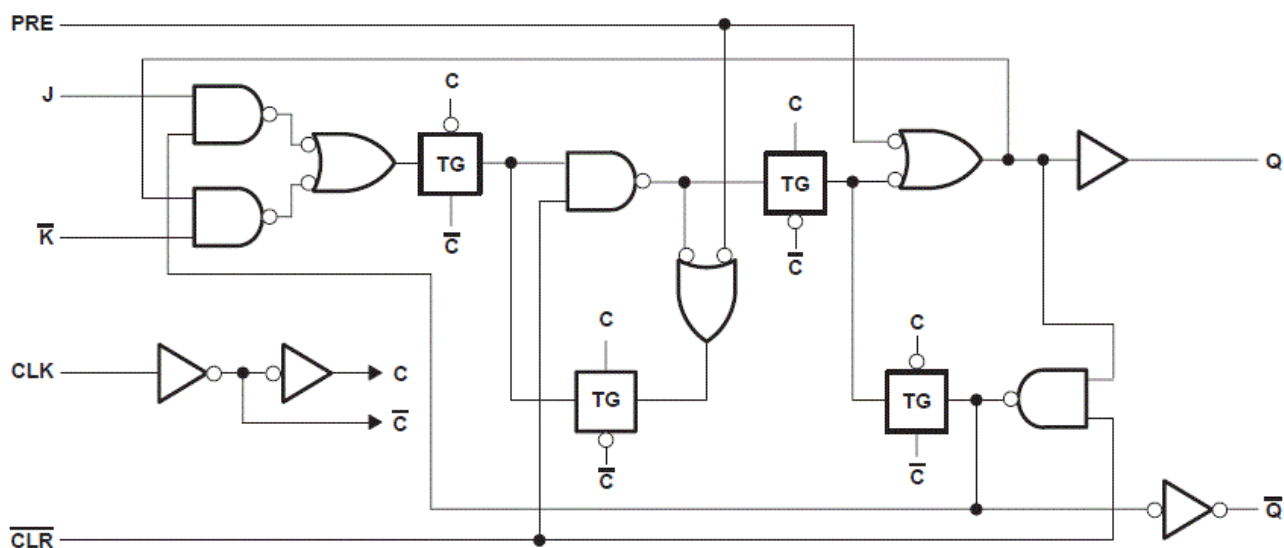
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and $\overline{\text{K}}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{\text{K}}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{\text{K}}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{\text{K}}$ are tied together.

7.2 Functional Block Diagram



7.3 Device Functional Modes

Table 7-1. Function Table

| INPUTS | | | | | OUTPUTS | |
|--------|-------------------------|-----|---|-----------------------|------------------|------------------------|
| PRE | $\overline{\text{CLR}}$ | CLK | J | $\overline{\text{K}}$ | Q | $\overline{\text{Q}}$ |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H ⁽¹⁾ | H ⁽¹⁾ |
| H | H | ↑ | L | L | L | H |
| H | H | ↑ | H | L | Toggle | |
| H | H | ↑ | L | H | Q0 | $\overline{\text{Q0}}$ |
| H | H | ↑ | H | H | H | L |
| H | H | L | X | X | Q0 | $\overline{\text{Q0}}$ |

(1) This configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------|
| 5962-8415001VFA | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8415001VF A SNV54HC109W |
| 5962-8415001VFA.A | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8415001VF A SNV54HC109W |
| 84150012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84150012A SNJ54HC 109FK |
| 8415001EA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001EA SNJ54HC109J |
| 8415001FA | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001FA SNJ54HC109W |
| JM38510/65304BEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65304BEA |
| JM38510/65304BEA.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65304BEA |
| M38510/65304BEA | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65304BEA |
| SN54HC109J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC109J |
| SN54HC109J.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC109J |
| SN74HC109D | Obsolete | Production | SOIC (D) 16 | - | - | Call TI | Call TI | -40 to 85 | HC109 |
| SN74HC109DR | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HC109 |
| SN74HC109DR.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC109 |
| SN74HC109DRG4 | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC109 |
| SN74HC109DRG4.A | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC109 |
| SN74HC109N | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC109N |
| SN74HC109N.A | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC109N |
| SN74HC109NE4 | Active | Production | PDIP (N) 16 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC109N |
| SN74HC109NSR | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC109 |
| SN74HC109NSR.A | Active | Production | SOP (NS) 16 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC109 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SNJ54HC109FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84150012A SNJ54HC 109FK |
| SNJ54HC109FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84150012A SNJ54HC 109FK |
| SNJ54HC109J | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001EA SNJ54HC109J |
| SNJ54HC109J.A | Active | Production | CDIP (J) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001EA SNJ54HC109J |
| SNJ54HC109W | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001FA SNJ54HC109W |
| SNJ54HC109W.A | Active | Production | CFP (W) 16 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8415001FA SNJ54HC109W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC109, SN54HC109-SP, SN74HC109 :

- Catalog : [SN74HC109](#), [SN54HC109](#)
- Military : [SN54HC109](#)
- Space : [SN54HC109-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

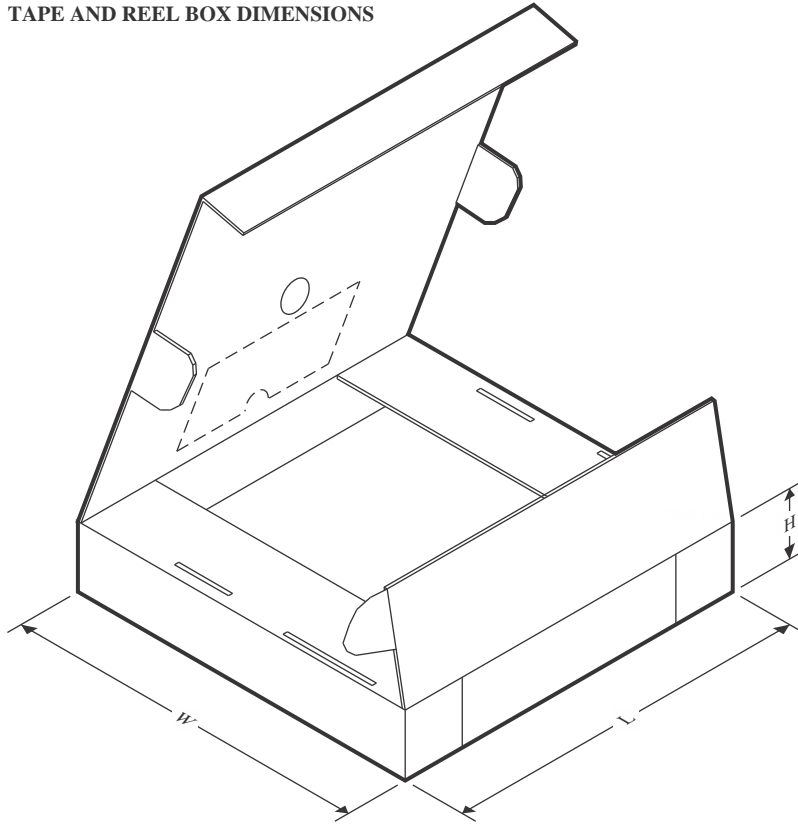
TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC109DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC109DRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC109NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

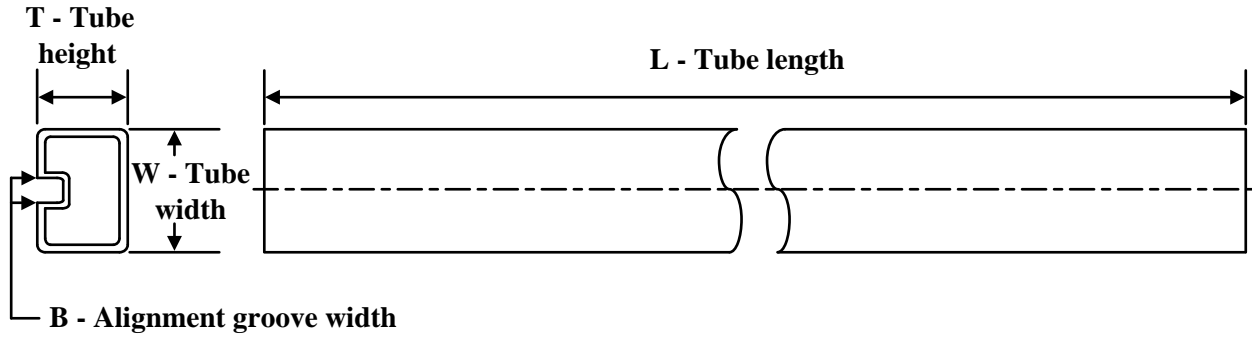
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

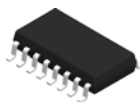
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC109DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC109DRG4 | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC109NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8415001VFA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-8415001VFA.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| 84150012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8415001FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HC109N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC109N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC109N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC109N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC109NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC109NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC109FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC109FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC109W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HC109W.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

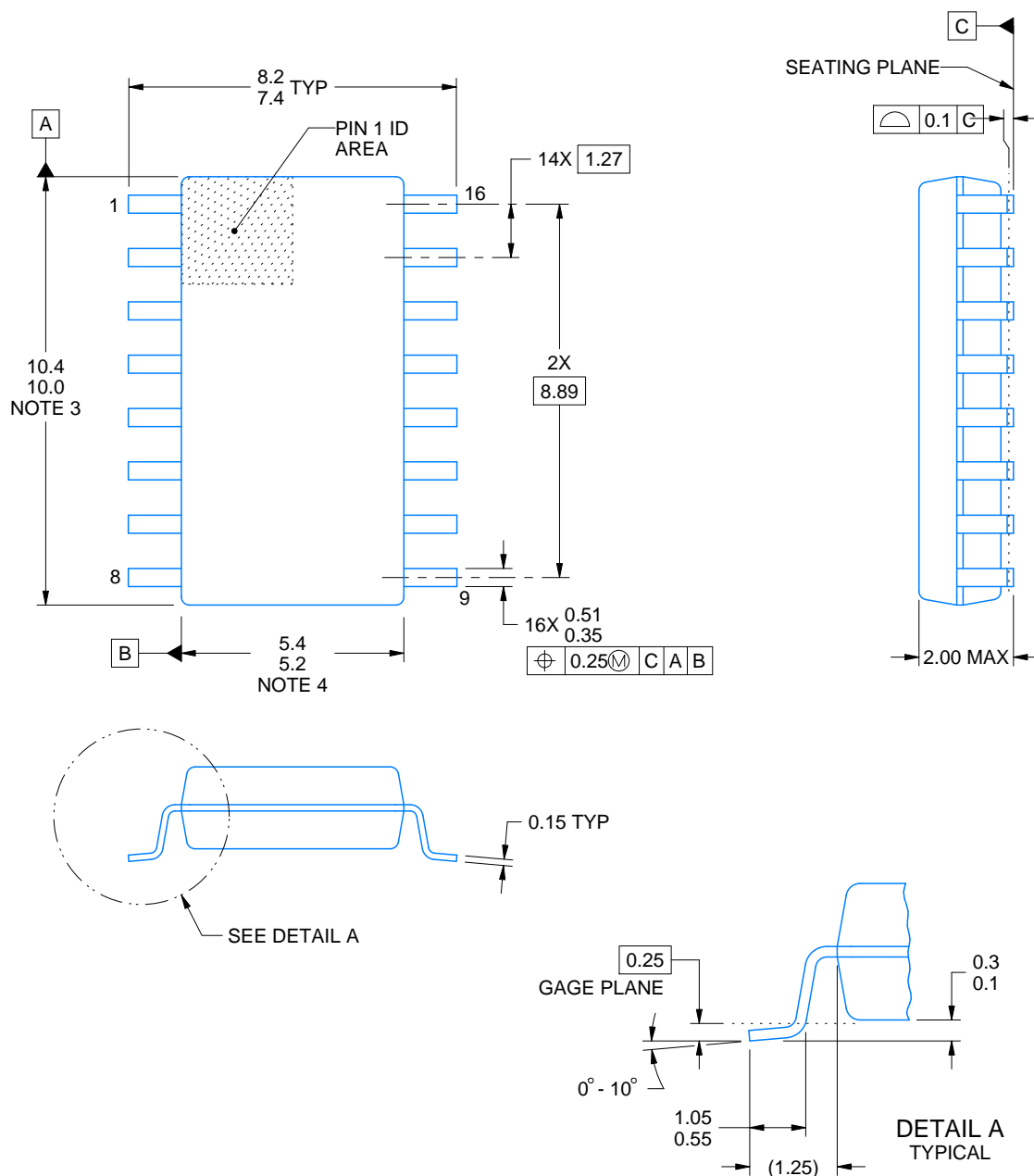


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

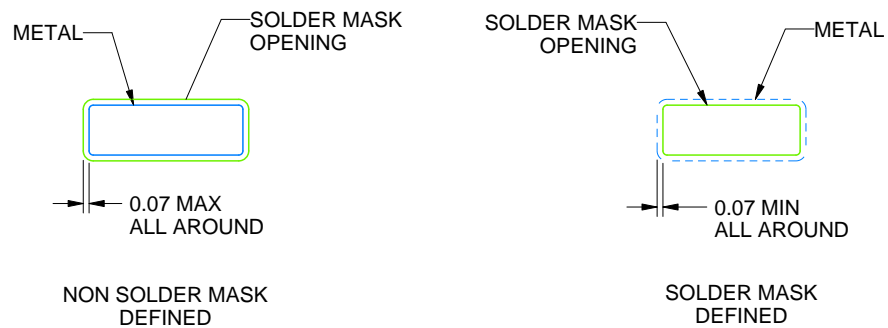
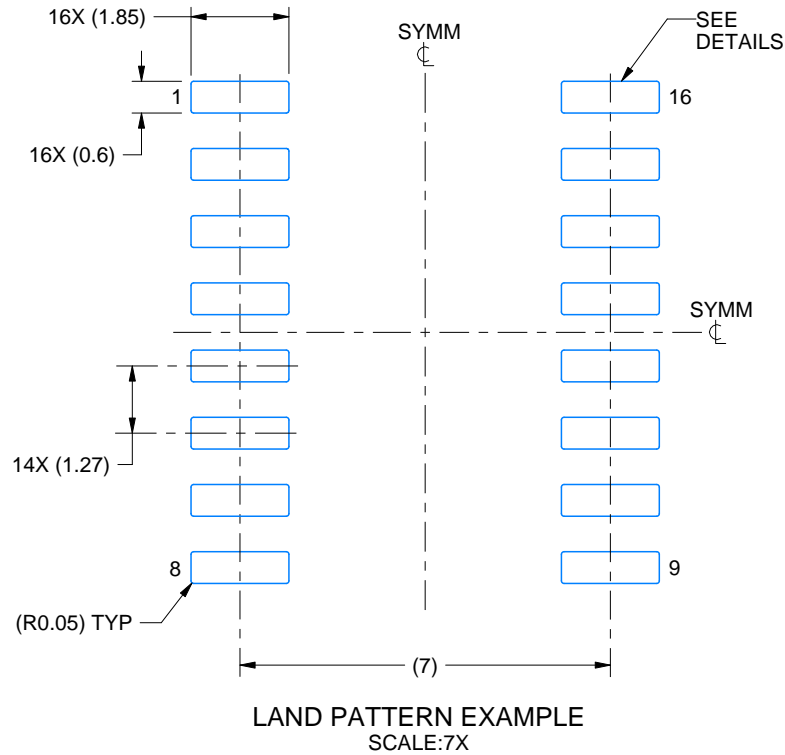
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

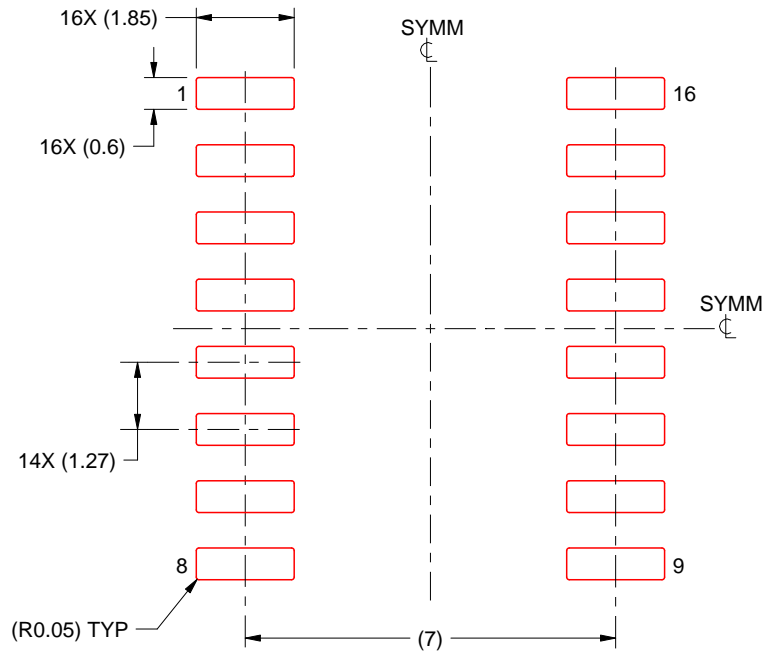
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

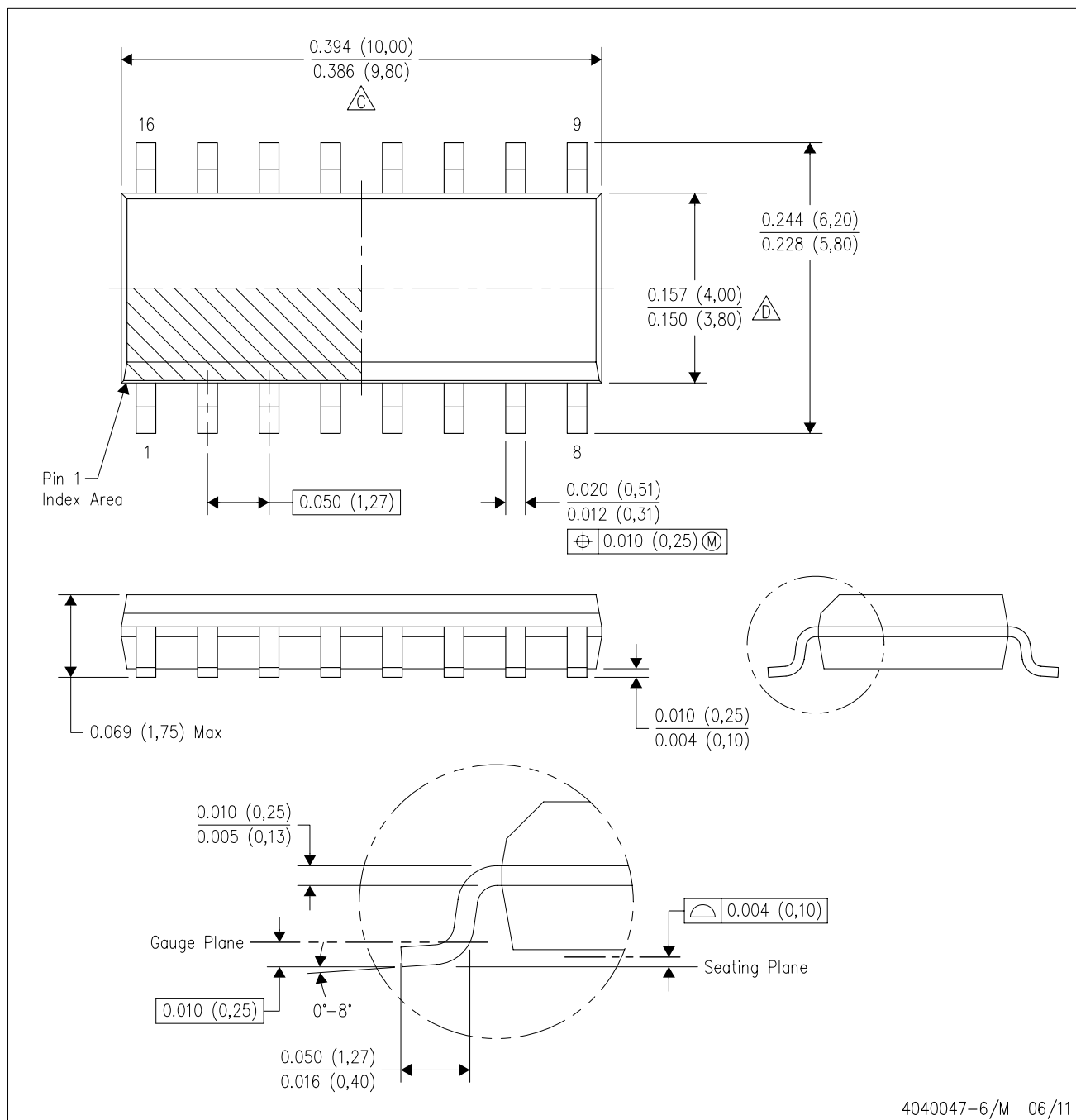
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

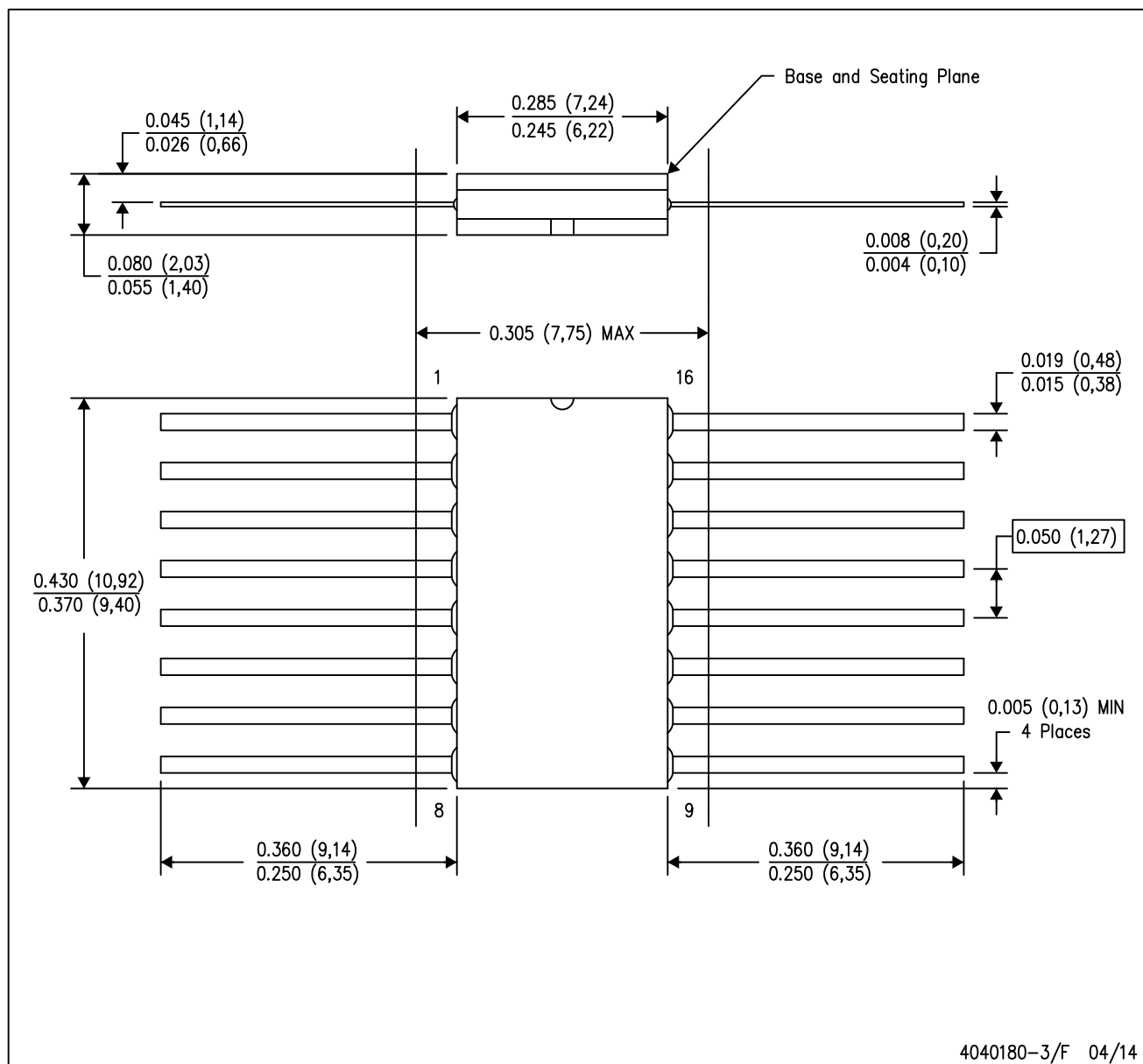
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

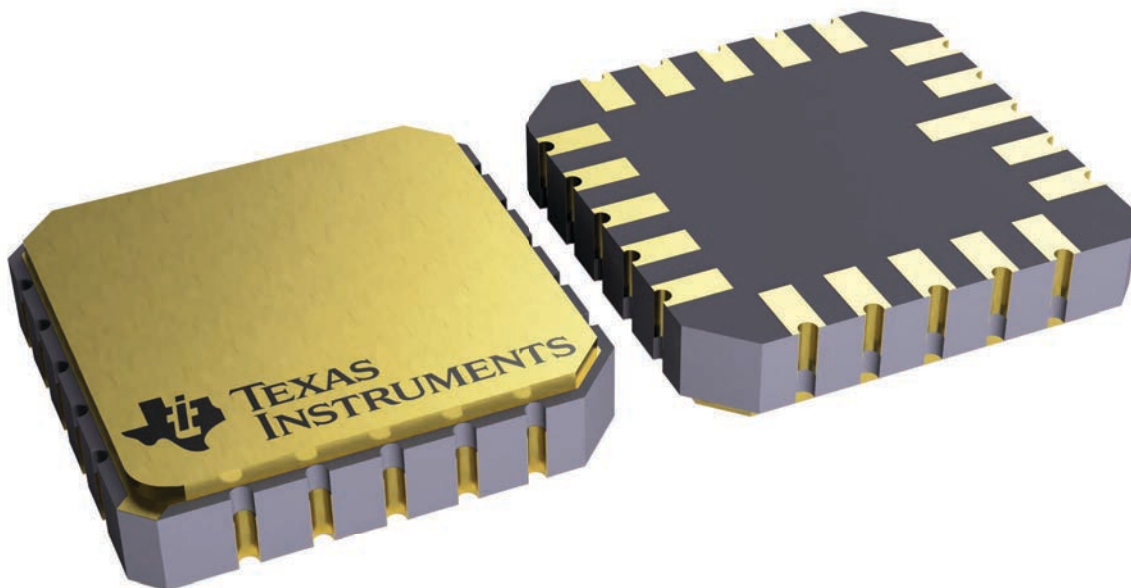
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

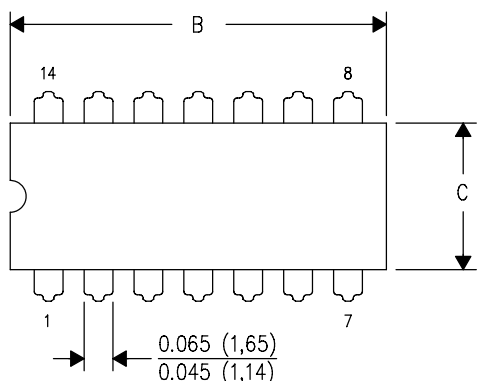


4229370VA\

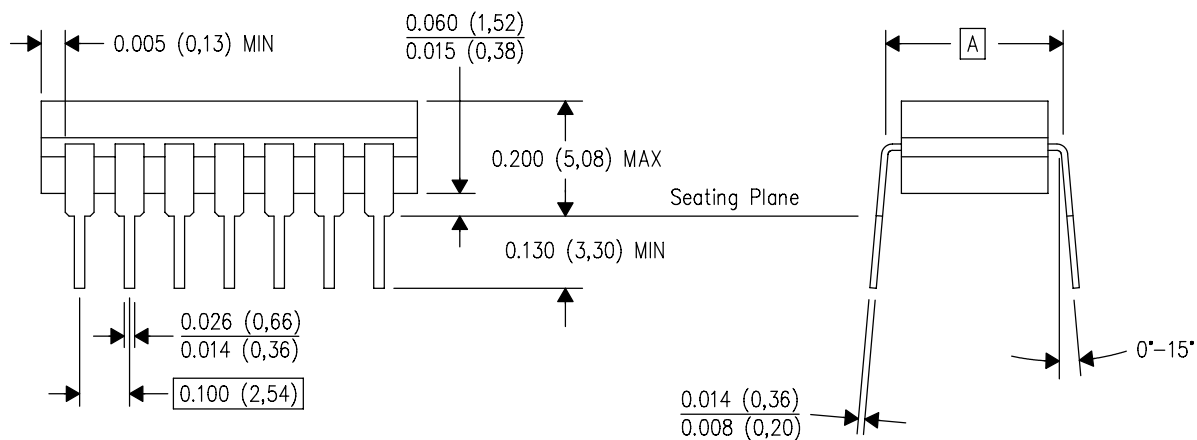
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



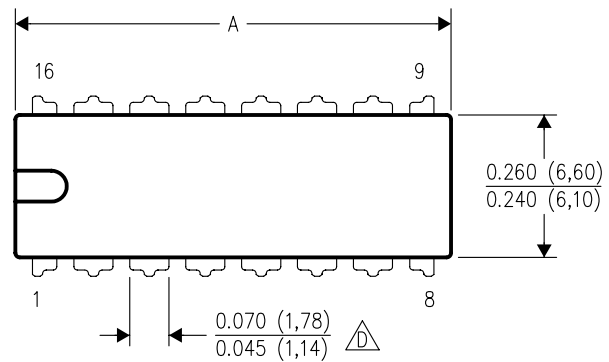
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

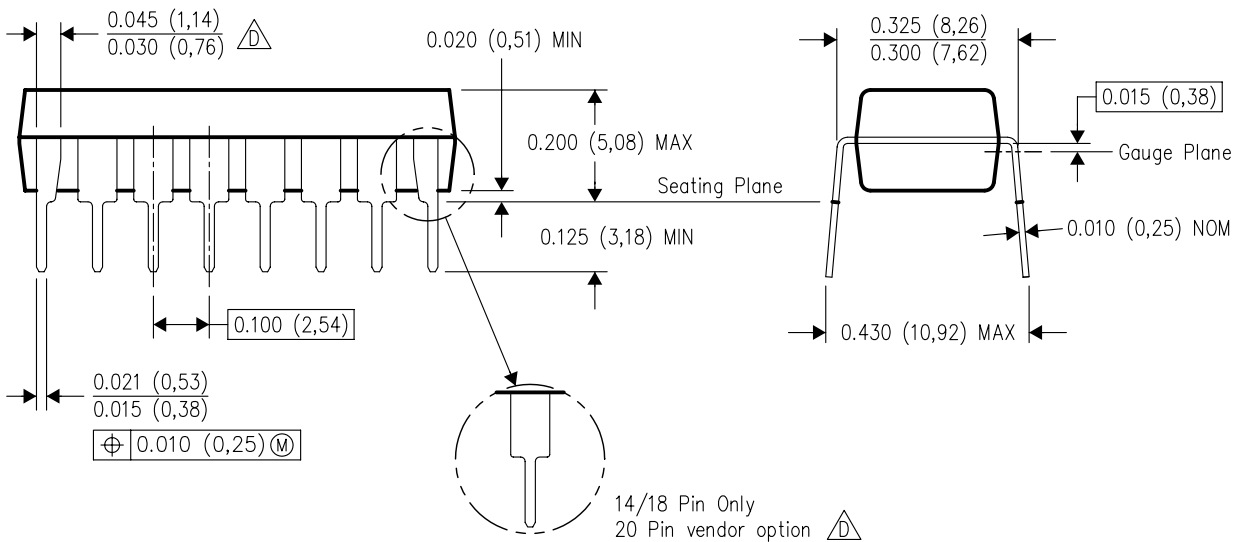
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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