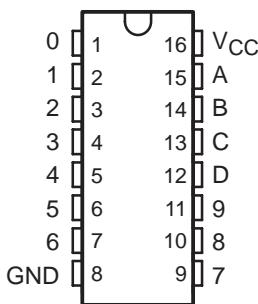
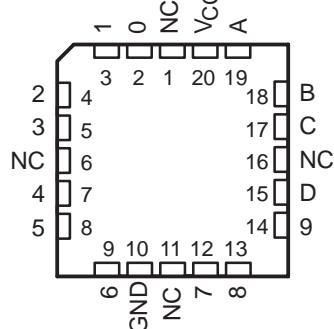


- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical $t_{pd} = 14$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Full Decoding of Input Logic
- All Outputs Are High for Invalid BCD Conditions
- Also for Applications as 3-Line to 8-Line Decoders

SN54HC42 . . . J OR W PACKAGE
SN74HC42 . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54HC42 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all inputs remain off for all invalid input conditions.

ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC42N	SN74HC42N
	SOIC – D	Tube of 40	SN74HC42D	HC42
		Reel of 2500	SN74HC42DR	
		Reel of 250	SN74HC42DT	
	SOP – NS	Reel of 2000	SN74HC42NSR	HC42
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC42J	SNJ54HC42J
	CFP – W	Tube of 150	SNJ54HC42W	SNJ54HC42W
	LCCC – FK	Tube of 55	SNJ54HC42FK	SNJ54HC42FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54HC42, SN74HC42
4-LINE TO 10-LINE DECODERS (1 of 10)**

SCLS091D – DECEMBER 1982 – REVISED SEPTEMBER 2003

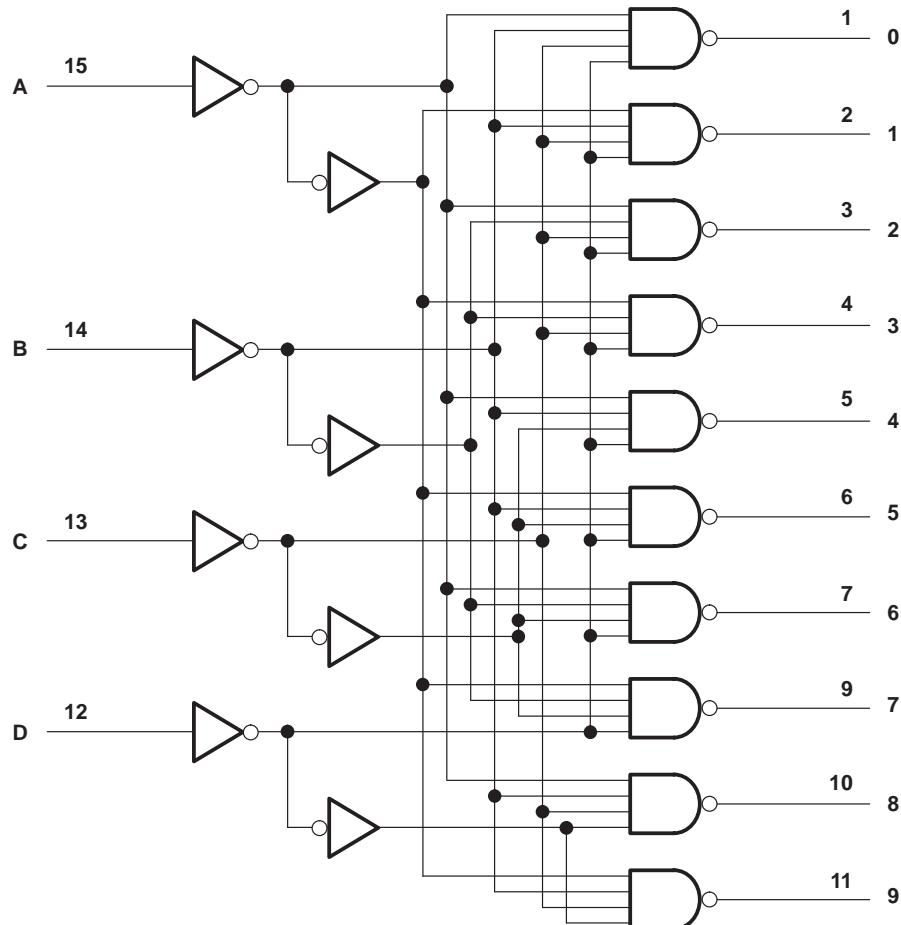
FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
Invalid	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H



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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC42, SN74HC42 4-LINE TO 10-LINE DECODERS (1 of 10)

SCLS091D – DECEMBER 1982 – REVISED SEPTEMBER 2003

recommended operating conditions (see Note 3)

			SN54HC42			SN74HC42			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5				V
		V _{CC} = 4.5 V	3.15		3.15				
		V _{CC} = 6 V	4.2		4.2				
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5			V
		V _{CC} = 4.5 V		1.35		1.35			
		V _{CC} = 6 V		1.8		1.8			
V _I	Input voltage		0	V _{CC}		0	V _{CC}		V
V _O	Output voltage		0	V _{CC}		0	V _{CC}		V
Δt/ΔV	Input transition rise/fall time	V _{CC} = 2 V		1000		1000			ns
		V _{CC} = 4.5 V		500		500			
		V _{CC} = 6 V		400		400			
T _A	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC42		SN74HC42		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998	1.9		1.9		V
			4.5 V	4.4	4.499	4.4		4.4		
			6 V	5.9	5.999	5.9		5.9		
		I _{OH} = -4 mA	4.5 V	3.98	4.3	3.7		3.84		V
			6 V	5.48	5.8	5.2		5.34		
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V	0.002	0.1	0.1		0.1		V
			4.5 V	0.001	0.1	0.1		0.1		
			6 V	0.001	0.1	0.1		0.1		
		I _{OL} = 4 mA	4.5 V		0.17	0.26	0.4		0.33	V
			6 V	0.15	0.26	0.4		0.33		
I _I	V _I = V _{CC} or 0	6 V		±0.1	±100		±1000		±1000	nA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V			8	160		80	μA	
C _i		2 V to 6 V		3	10	10		10	pF	

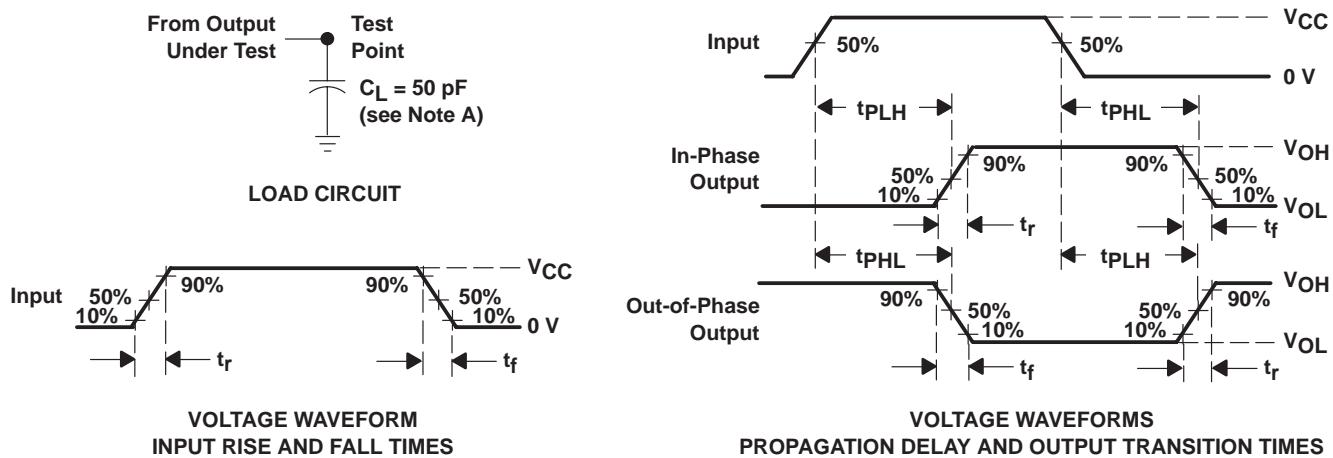
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC42		SN74HC42		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C, or D	0-9	2 V	65	150	225	190				ns
			4.5 V	18	30	45	38				
			6 V	14	26	38	32				
t _t		Any	2 V	28	75	110	95				ns
			4.5 V	8	15	22	19				
			6 V	7	13	19	16				

operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load	39	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
 B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 C. The outputs are measured one at a time with one input transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-86821012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86821012A SNJ54HC 42FK
5962-8682101EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682101EA SNJ54HC42J
SN54HC42J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC42J
SN54HC42J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC42J
SN74HC42D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC42
SN74HC42DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HC42
SN74HC42DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC42
SN74HC42DRG4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC42
SN74HC42DRG4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC42
SN74HC42DT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-40 to 85	HC42
SN74HC42N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC42N
SN74HC42N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC42N
SNJ54HC42FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86821012A SNJ54HC 42FK
SNJ54HC42FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962- 86821012A SNJ54HC 42FK
SNJ54HC42J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682101EA SNJ54HC42J
SNJ54HC42J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8682101EA SNJ54HC42J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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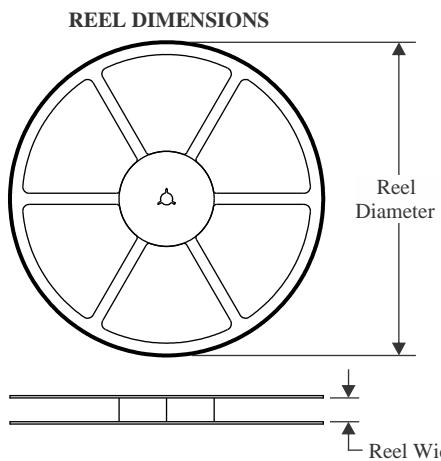
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OTHER QUALIFIED VERSIONS OF SN54HC42, SN74HC42 :

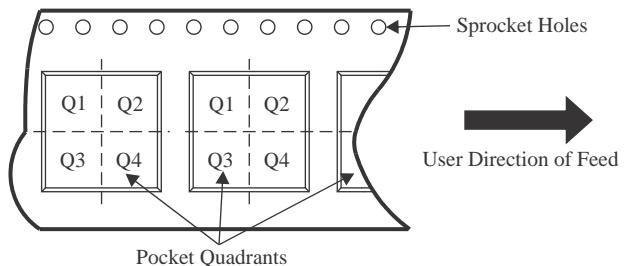
- Catalog : [SN74HC42](#)
- Military : [SN54HC42](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC42DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC42DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC42DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC42DRG4	SOIC	D	16	2500	353.0	353.0	32.0

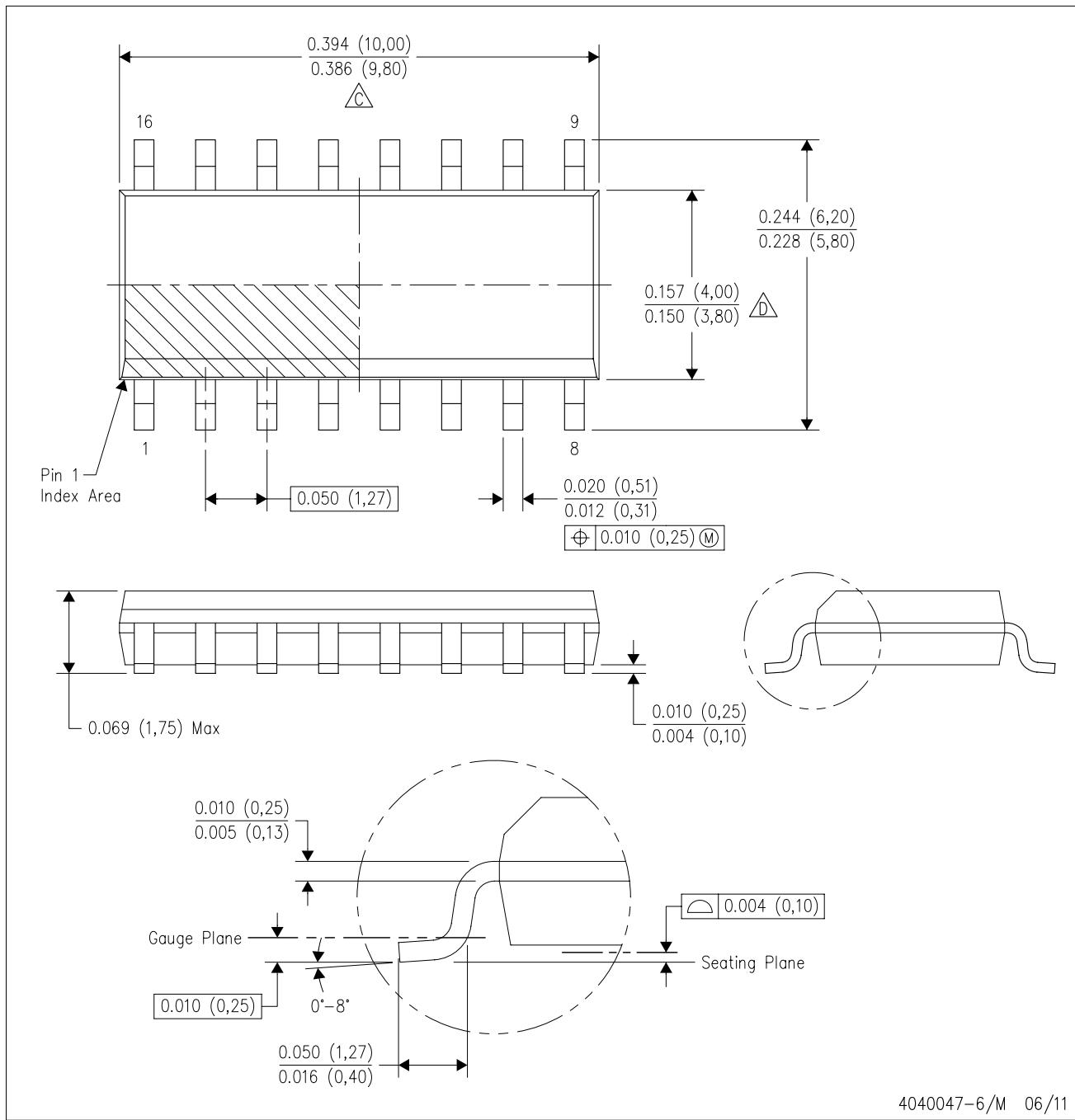
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
5962-86821012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74HC42N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC42N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC42N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC42N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54HC42FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC42FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

GENERIC PACKAGE VIEW

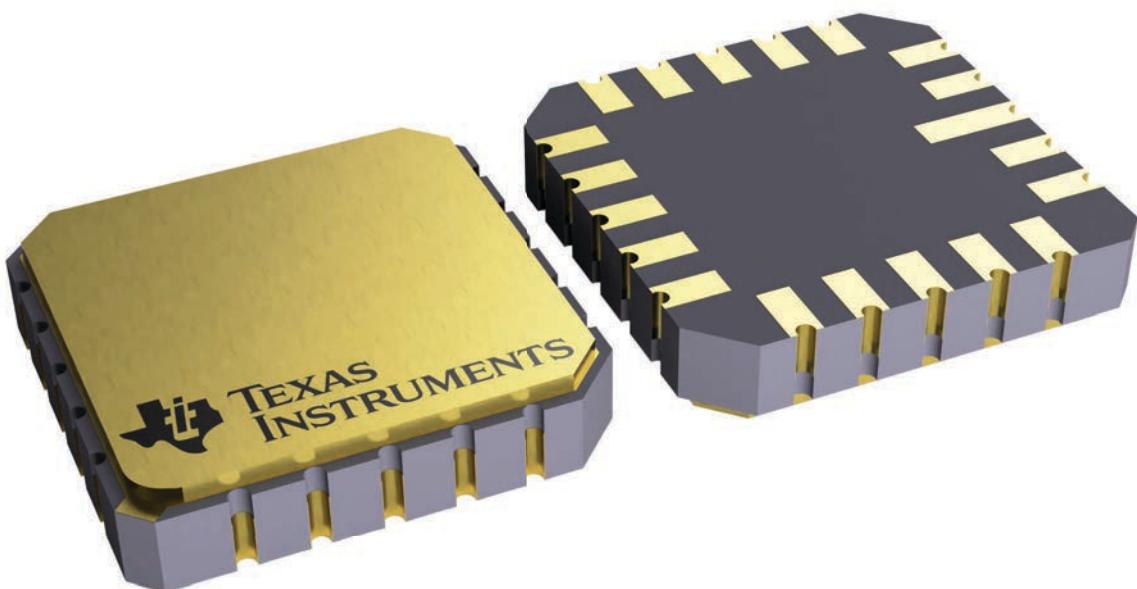
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

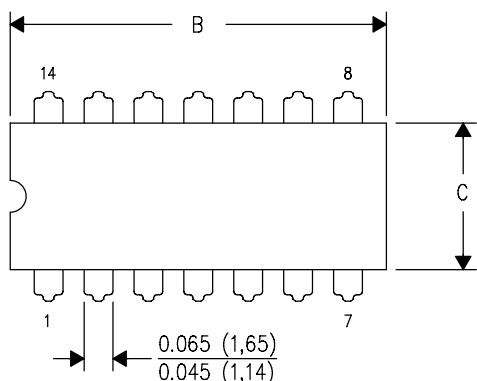


4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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