

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

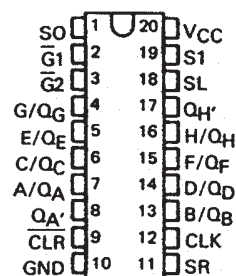
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- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:
Hold (Store) Shift Left
Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear
- Applications:
Stacked or Push-Down Registers
Buffer Storage, and Accumulator Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

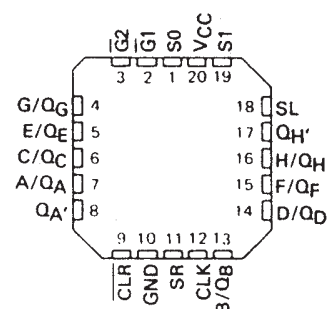
SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS299, SN54S299 . . . FK PACKAGE

(TOP VIEW)



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS										OUTPUTS	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	†	X	H	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn	H	QGn
	H	L	H	L	L	†	X	L	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn	L	QGn
Shift Left	H	H	L	L	L	†	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H	QBn	H
	H	H	L	L	L	†	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

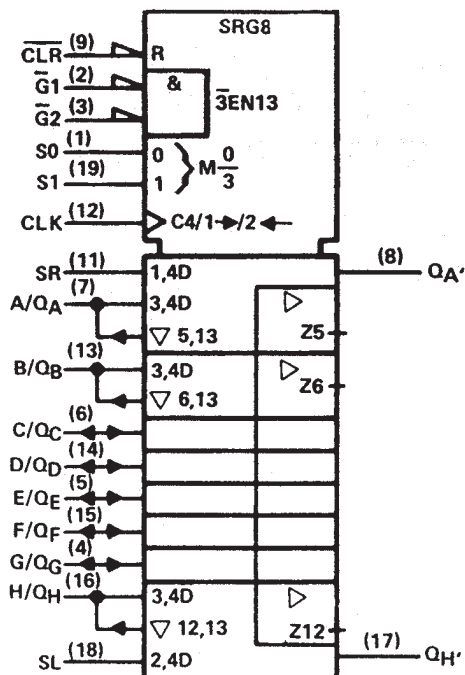
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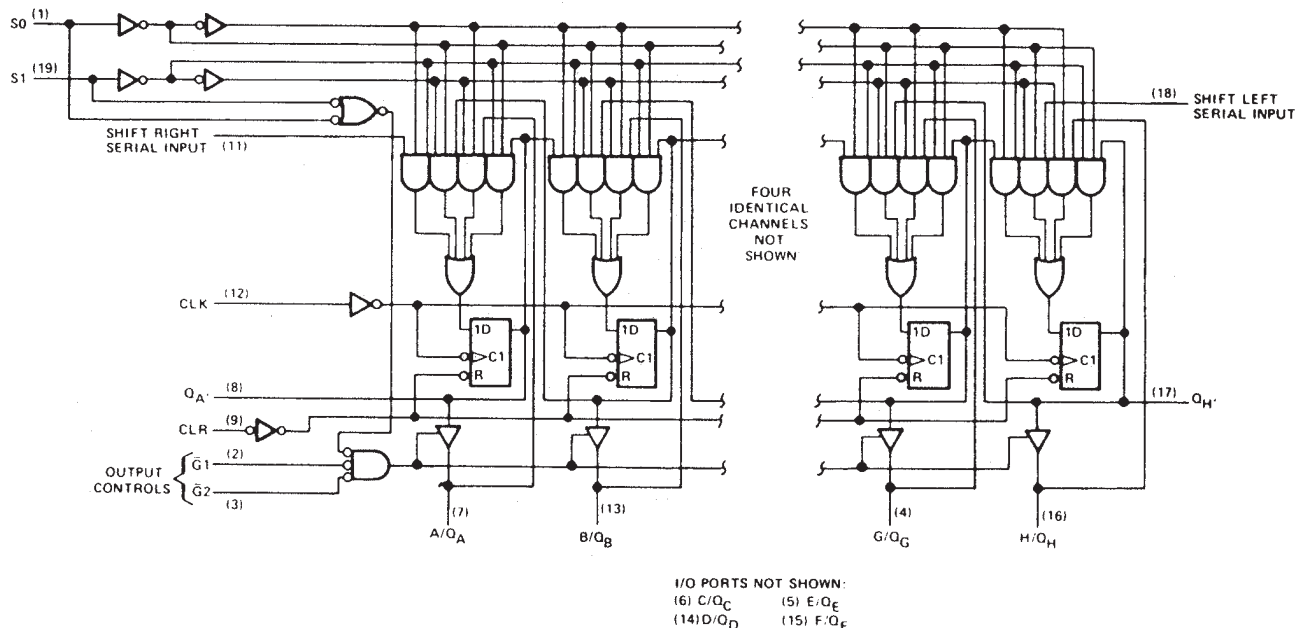
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

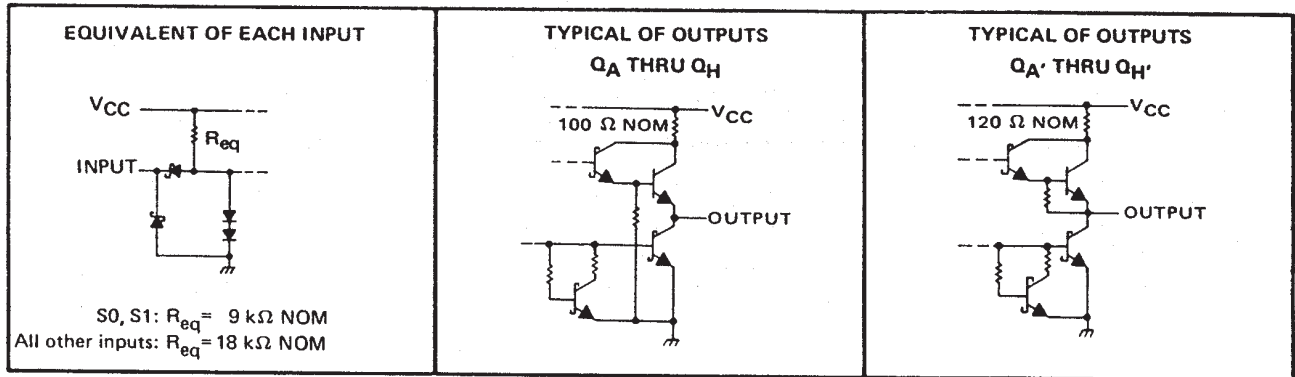


Pin numbers shown are for DW, J, N, and W packages.

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	-55°C to 125°C
SN74LS299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I _{OH}	Q _A thru Q _H	-1			-2.6			mA
	Q _A ' or Q _H '	-0.4			-0.4			
Low-level output current, I _{OL}	Q _A thru Q _H	12			24			mA
	Q _A ' or Q _H '	4			8			
Clock frequency, f _{clock}		0			0			MHz
Width of clock pulse, t _w (clock)	Clock high	30			30			ns
	Clock low	18			10			
Width of clear pulse, t _w (clear)	Clear low	25			20			ns
Setup time, t _{su}	Select	35†			35†			ns
	High-level data†	20†			20†			
	Low-level data†	20†			20†			
	Clear inactive-state	24†			20†			
Hold time, t _h	Select	10†			10†			ns
	Data†	3†			0†			
Operating free-air temperature, T _A		-55			0			°C

† Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS299		SN74LS299		UNIT		
			MIN	TYP‡ MAX	MIN	TYP‡ MAX			
V _{IH}	High-level input voltage		2		2		V		
V _{IL}	Low-level input voltage			0.7		0.8	V		
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA		-1.5		-1.5	V		
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	2.4	3.1	V	
		Q _A ' or Q _H '	V _{IL} = V _{ILmax} , I _{OH} = MAX	2.5	3.4	2.7	3.4		
V _{OL}	Low-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax}	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
				I _{OL} = 24 mA			0.35	0.5	
		Q _A ' or Q _H '		I _{OL} = 4 mA	0.25	0.4	0.25	0.4	
				I _{OL} = 8 mA			0.35	0.5	
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V		40		40	μA	
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V		-400		-400	μA	
I _I	Input current at maximum input voltage	S0, S1	V _{CC} = MAX	V _I = 7 V		200		200	μA
		A thru H		V _I = 5.5 V		100		100	
		Any other		V _I = 7 V		100		100	
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V		40		40	μA	
		Any other			20		20		
I _{IL}	Low-level input current	S0, S1	V _{CC} = MAX, V _I = 0.4 V		-0.8		-0.8	mA	
		Any other			-0.4		-0.4		
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX		-30		-130	mA	
		Q _A ' or Q _H '			-20		-100		
I _{CC}	Supply current	V _{CC} = MAX		33	53	33	53	mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	20	35		MHz
t_{PLH}	CLK	Q_A' or Q_H'	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		22	33	ns
t_{PHL}		Q_A' or Q_H'			26	39	
t_{PHL}		Q_A' or Q_H'			27	40	ns
t_{PLH}	CLK	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 45 \text{ pF}$		17	25	ns
t_{PHL}		Q_A thru Q_H			26	39	
t_{PHL}		Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G1}, \overline{G2}$	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 5 \text{ pF}$		13	21	ns
t_{PZL}		Q_A thru Q_H			19	30	
t_{PHZ}	$\overline{G1}, \overline{G2}$	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 5 \text{ pF}$		10	20	ns
t_{PLZ}		Q_A thru Q_H			10	15	

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

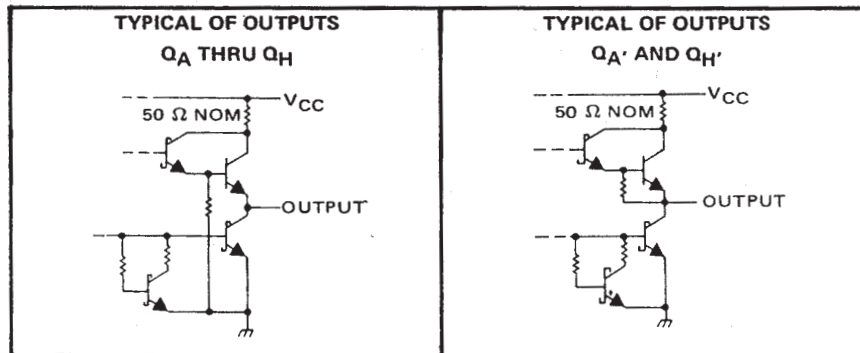
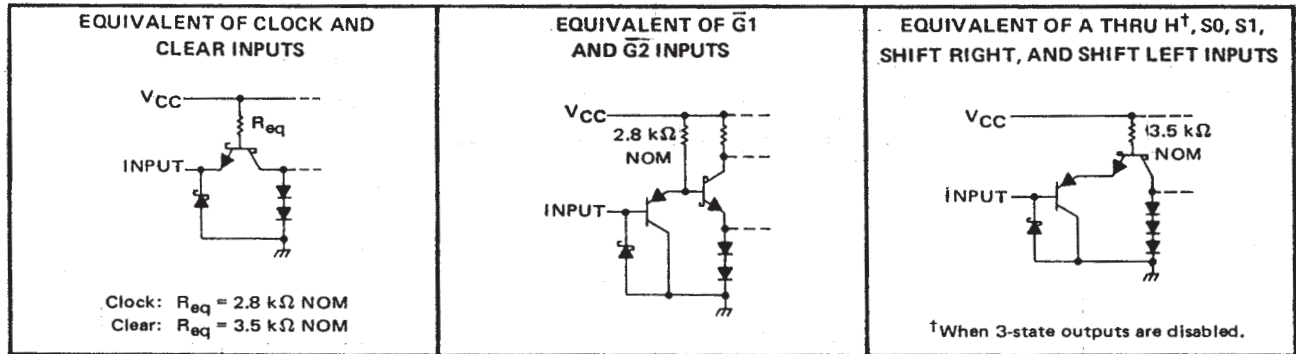


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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S299 (See Note 1)	-55°C to 125°C
SN74S299	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H	-2			-6.5			mA
	Q_A' or Q_H'	-0.5			-0.5			
Low-level output current, I_{OL}	Q_A thru Q_H	20			20			mA
	Q_A' or Q_H'	6			6			
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su}	Select	15†			15†			ns
	High-level data†	7†			7†			
	Low-level data†	5†			5†			
	Clear inactive-state	10†			10†			
Hold time, t_h	Select	5†			5†			ns
	Data†	5†			5†			
Operating free-air temperature, T_A		-55		125	0		70	°C

† Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = –18 mA			–1.2	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	V
		Q _A ' or Q _H '	V _{IL} = 0.8 V, I _{OH} = MAX	2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		100	μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		–250	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V		100	μA
		Any other			50	
I _{IL}	Low-level input current	CLK or CLR	V _{CC} = MAX, V _I = 0.5 V		–2	mA
		S0, S1			–500	μA
		Any other			–250	μA
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX	–40	–100	mA
		Q _A ' or Q _H '		–20	–100	
I _{CC}	Supply current	V _{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 1 kΩ, C _L = 15 pF		12	20	ns
t _{PHL}					13	20	
t _{PHL}	CLR	Q _A ' or Q _H '			14	21	ns
t _{PLH}	CLK	Q _A thru Q _H	R _L = 280 Ω, C _L = 45 pF		15	21	ns
t _{PHL}					15	21	
t _{PHL}	CLR	Q _A thru Q _H			16	24	ns
t _{PZH}	G1, G2	Q _A thru Q _H			10	18	ns
t _{PZL}					12	18	
t _{PHZ}	G1, G2	Q _A thru Q _H	R _L = 280 Ω, C _L = 5 pF		7	12	ns
t _{PLZ}							

¶ f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
78024012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
7802401RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
7802401RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
7802401SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
7802401SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SN54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS299J
SN74LS299DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299
SN74LS299N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SN74LS299N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SN74LS299N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SN74LS299N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS299N
SNJ54LS299FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
SNJ54LS299FK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
SNJ54LS299FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS299FK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK
SNJ54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J
SNJ54LS299W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SNJ54LS299W	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SNJ54LS299W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W
SNJ54LS299W.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LS299, SN74LS299 :

- Catalog : [SN74LS299](#)
- Military : [SN54LS299](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
78024012A	FK	LCCC	20	55	506.98	12.06	2030	NA
7802401SA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS299DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS299N	N	PDIP	20	20	506	13.97	11230	4.32
SN74LS299N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS299FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS299FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS299W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54LS299W.A	W	CFP	20	25	506.98	26.16	6220	NA

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

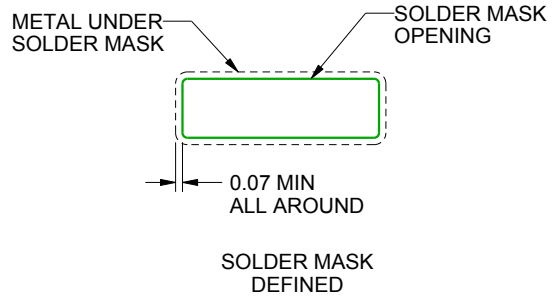
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

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