

## SNx4LVC541A Octal Buffers/Drivers With 3-State Outputs

### 1 Features

- Operates from 1.65V to 3.6V
- Inputs accept voltages to 5.5V
- Maximum  $t_{pd}$  of 5.1ns at 3.3V
- Typical  $V_{OLP}$  (output ground bounce)  $<0.8V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $>2V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Support mixed-mode signal operation on all ports (5V input/output voltage with 3.3V  $V_{CC}$ )
- $I_{off}$  supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted, on all other products, production processing does not necessarily include testing of all parameters

### 2 Applications

- Drive an indicator LED
- Redrive a digital signal
- Drive a transmission line
- Hold a signal during controller reset

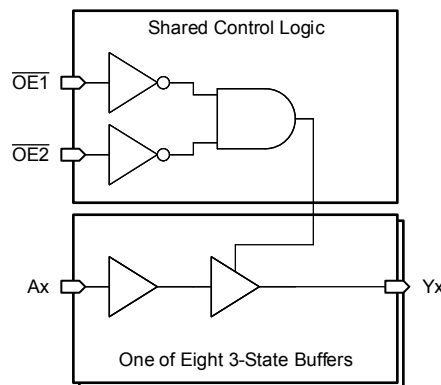
### 3 Description

The SNx4LVC541A contains eight non-inverting buffers with 3-state outputs. The active low output enable pins ( $\overline{OE1}$  and  $\overline{OE2}$ ) control all eight channels, and are configured so that both must be low for the outputs to be active.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>	BODY SIZE <sup>(3)</sup>
SN54LVC541A	J (CDIP, 20)	24.2mm × 7.62mm	24.2mm × 6.92mm
	W (CFP, 20)	13.09mm × 8.13mm	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm	8.89mm × 8.89mm
SN74LVC541A	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	DB (SSOP, 20)	7.2mm × 7.8mm	7.50mm × 5.3mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm
	DGS (VSSOP, 20)	5.1mm × 4.9mm	5.1mm × 3.0mm
	RKS (VQFN, 20)	4.5mm × 2.5mm	4.5mm × 2.5mm
	DGV (TVSOP, 20)	5.0mm × 6.4mm	5.0mm × 4.4mm
	RGY (VQFN, 20)	4.5mm × 3.5mm	4.5mm × 3.5mm

- For more information, see [Mechanical, Packaging, and Orderable Information](#).
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Functional Block Diagram



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## 4 Pin Configuration and Functions

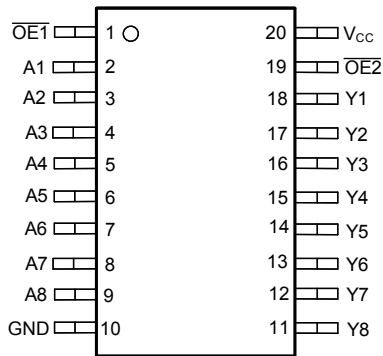


Figure 4-1. SN54LVC541A J , W Package (Top View)

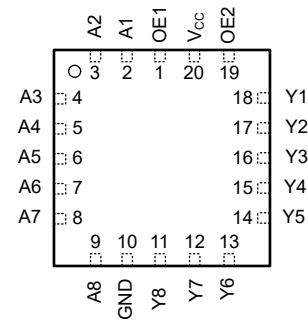


Figure 4-2. SN54LVC541A FK Package (Top View)

### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
OE1	1	I	Output enable 1, active low
OE2	19	I	Output enable 2, active low
V <sub>CC</sub>	20	P	Positive supply
Y1	18	O	Output for channel 1
Y2	17	O	Output for channel 2
Y3	16	O	Output for channel 3
Y4	15	O	Output for channel 4
Y5	14	O	Output for channel 5
Y6	13	O	Output for channel 6
Y7	12	O	Output for channel 7
Y8	11	O	Output for channel 8

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

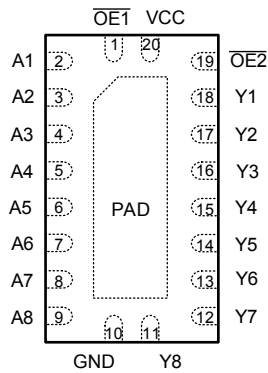


Figure 4-3. SN74LVC541A RKS Package (Top View)

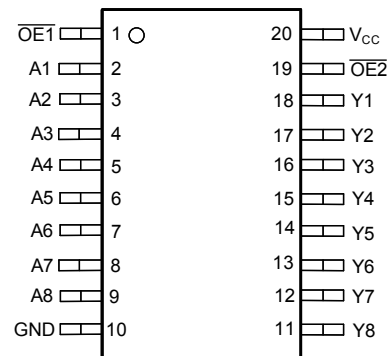


Figure 4-4. SN74LVC541A PW, DW, NS, DB, DGS, DGV Package (Top View)

### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
OE1	1	I	Output enable 1, active low
OE2	19	I	Output enable 2, active low
Thermal Pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.
V <sub>CC</sub>	20	P	Positive supply
Y1	18	O	Output for channel 1
Y2	17	O	Output for channel 2
Y3	16	O	Output for channel 3
Y4	15	O	Output for channel 4
Y5	14	O	Output for channel 5
Y6	13	O	Output for channel 6
Y7	12	O	Output for channel 7
Y8	11	O	Output for channel 8

(1) Signal Types: I = Input, O = Output, G = Ground, P = Power.

(2) RKS package only.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			SN54LVC541A		SN74LVC541A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V			0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V			1.7		
		V <sub>CC</sub> = 2.7V to 3.6V	2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V			0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V			0.7		
		V <sub>CC</sub> = 2.7V to 3.6V		0.8	0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65V				-4	mA
		V <sub>CC</sub> = 2.3V				-8	
		V <sub>CC</sub> = 2.7V		-12		-12	
		V <sub>CC</sub> = 3V		-24		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65V				4	mA
		V <sub>CC</sub> = 2.3V				8	
		V <sub>CC</sub> = 2.7V		12		12	
		V <sub>CC</sub> = 3V		24		24	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to verify proper device operation. Refer to the TI application note, [Implications of Slow or Floating CMOS Inputs](#).

### 5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC <sup>(1)</sup>						UNIT
		R <sub>θJA</sub>	R <sub>θJC(top)</sub>	R <sub>θJB</sub>	Ψ <sub>JT</sub>	Ψ <sub>JB</sub>	R <sub>θJC(bot)</sub>	
PW (TSSOP)	20	120.3	62.5	82.4	16.0	81.5	N/A	°C/W
DGS (VSSOP)	20	129.9	72.4	86.1	18.6	85.8	N/A	°C/W
RKS (VQFN)	20	87.2	93.4	59.8	24.9	59.6	44.3	°C/W
DB (SSOP)	20	121.7	86.8	87.8	44.7	87	N/A	°C/W
DW (SOIC)	20	114.8	84.1	88.8	55.8	87.8	N/A	°C/W
NS (SOP)	20	116.3	82.4	86.2	43.9	85.5	N/A	°C/W
DGV (TVSOP)	20	128.7	43.8	70.4	3.2	69.7	N/A	°C/W
RGV (VQFN)	20	82.84	88.73	56.81	32.37	56.62	42.09	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

## 5.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–55°C TO 125°C			–40°C TO 85°C			–40°C TO 125°C			UNIT
			SN54LVC541A			SN74LVC541A			SN74LVC541A			
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100μA	1.65V to 3.6V			V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.3			V	
		2.7V to 3.6V	V <sub>CC</sub> – 0.2									
	I <sub>OH</sub> = –4mA	1.65V			1.20			1.20				
	I <sub>OH</sub> = –8mA	2.3V			1.7			1.7				
	I <sub>OH</sub> = –12mA	2.7V		2.2		2.2		2.2				
		3V		2.4		2.4		2.4				
I <sub>OH</sub> = –24mA	3V		2.2		2.2		2.2					
V <sub>OL</sub>	I <sub>OL</sub> = 100μA	1.65V to 3.6V					0.2		0.3	V		
		2.7V to 3.6V			0.2							
	I <sub>OL</sub> = 4mA	1.65V					0.45		0.45			
	I <sub>OL</sub> = 8mA	2.3V					0.7		0.7			
	I <sub>OL</sub> = 12mA	2.7V		0.4		0.4		0.4				
	I <sub>OL</sub> = 24mA	3V		0.55		0.55		0.55				
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5V	3.6V		±5		±5		±5	μA			
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0				±10		±10	μA			
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5V	3.6V		±15		±10		±10	μA			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND 3.6V ≤ V <sub>I</sub> ≤ 5.5V <sup>(2)</sup>	I <sub>O</sub> = 0	3.6V		10		10		10	μA		
					10		10		10			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6V, Other inputs at V <sub>CC</sub> or GND	2.7V to 3.6V		500		500		500	μA			
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V		4		4		4	pF			
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3V		5.5		5.5		5.5	pF			

(1) All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## 5.6 Switching Characteristics - SN54LVC541A

over recommended operating free-air temperature range (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC541A				UNIT
			V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y		5.6	1	5.1	ns
t <sub>en</sub>	$\overline{OE}$	Y		7.5	1	7	ns
t <sub>dis</sub>	$\overline{OE}$	Y		7.7	1	7	ns

### 5.7 Switching Characteristics, SN74LVC541A –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A								UNIT
			–40°C TO 85°C								
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	15.7	1	7.8	1	5.6	1.5	5.1	ns
t <sub>en</sub>	$\overline{OE}$	Y	1	17.5	1	10.5	1	7.5	1.5	7	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1	16.5	1	9	1	7.7	1.5	7	ns
t <sub>sk(o)</sub>										1	ns

### 5.8 Switching Characteristics, SN74LVC541A –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Section 6)

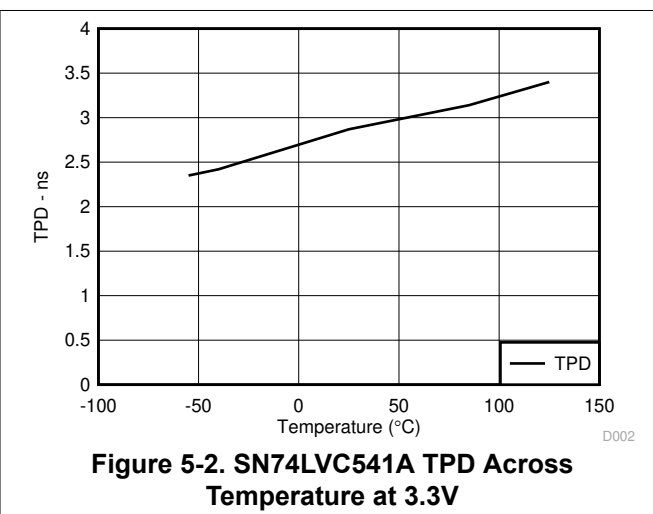
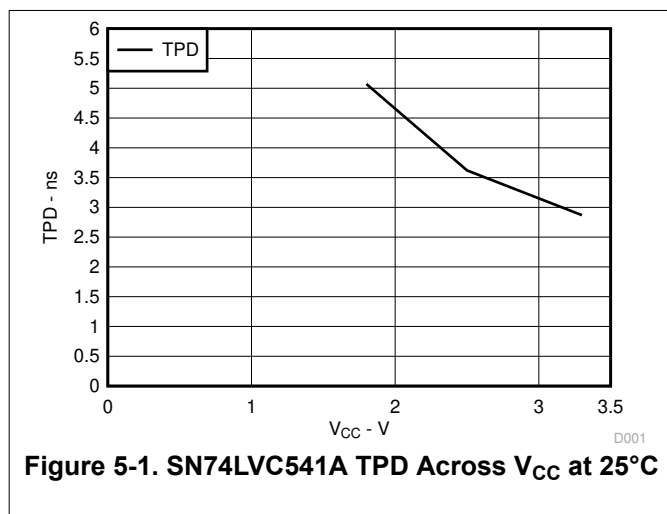
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC541A								UNIT
			–40°C TO 125°C								
			V <sub>CC</sub> = 1.8V ± 0.15V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	16.3	1	8.3	1	6.1	1	5.6	ns
t <sub>en</sub>	$\overline{OE}$	Y	1	18.5	1	11.1	1	8	1	7.5	ns
t <sub>dis</sub>	$\overline{OE}$	Y	1	17.3	1	9.7	1	8.2	1	7.5	ns
t <sub>sk(o)</sub>										1.5	ns

### 5.9 Operating Characteristics

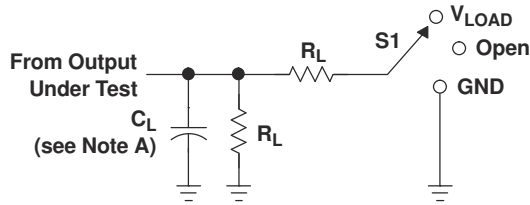
T<sub>A</sub> = 25°C

PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8V	V <sub>CC</sub> = 2.5V	V <sub>CC</sub> = 3.3V	UNIT
				TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10MHz	65	58	33	pF
		Outputs disabled		2	2	2	

### 5.10 Typical Characteristics



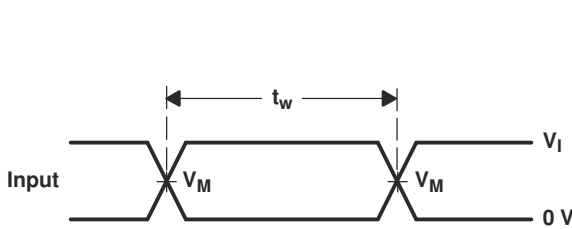
## 6 Parameter Measurement Information



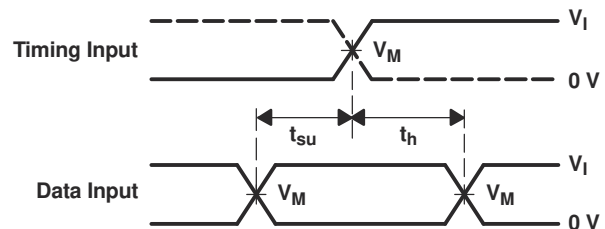
**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

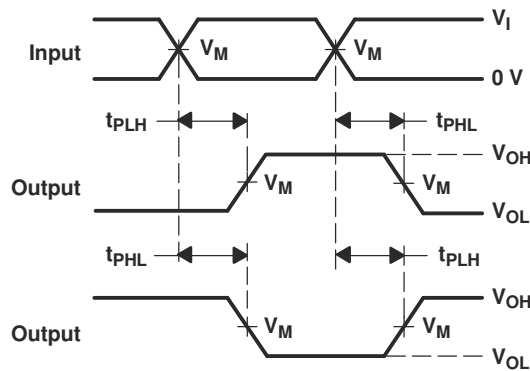
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



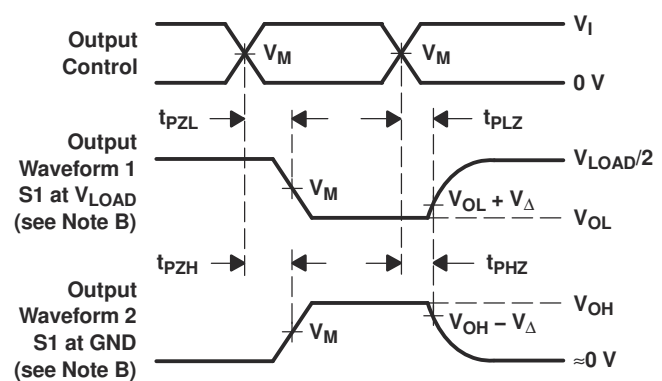
**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SNx4LVC541A contains eight buffers with 3-state outputs. The active low output enable pins ( $\overline{OE1}$  and  $\overline{OE2}$ ) control all eight channels, and are configured so that both must be low for the outputs to be active.

When the outputs are enabled, the outputs are actively driven low or high.

When the outputs are disabled, the outputs are set into the high-impedance state.

### 7.2 Functional Block Diagram

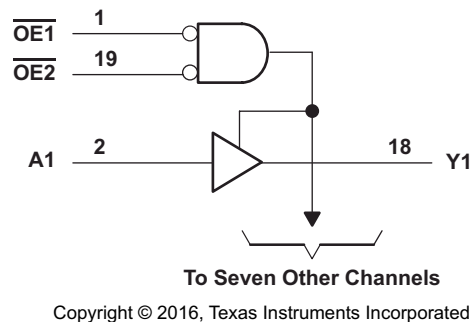


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs: driving high, driving low, and high impedance. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device can create fast edges into light loads, so consider routing and load conditions to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without damage. Limit the output power of the device to avoid damage from overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output does not source or sink current except minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the device does not control the output voltage. The output current is dependent on external factors. A floating node is a node that has no other drivers connected, and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while the device is in the high-impedance state. The value of the resistor depends on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10k $\Omega$  resistor meets these requirements.

Leave unused 3-state CMOS outputs disconnected.

#### 7.3.2 Partial Power Down ( $I_{off}$ )

This device includes circuitry to disable all outputs when the supply pin is held at 0V. When disabled, the outputs neither source nor sink current, regardless of the input voltages. The amount of leakage current at each output is defined by the  $I_{off}$  specification in the *Electrical Characteristics* table.

#### 7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification

results in excessive power consumption and can cause oscillations. See more details in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Terminate unused inputs at  $V_{CC}$  or GND. If a system does not always drive an input, consider adding a pull-up or pull-down resistor to provide a valid input voltage. The resistor value depends on multiple factors; a 10k $\Omega$  resistor, however, is recommended and typically meets all requirements.

### 7.3.4 Clamp Diode Structure

Figure 7-2 shows the inputs and outputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

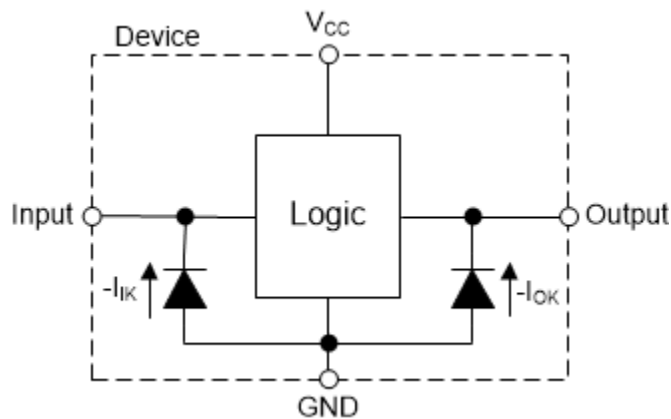


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

## 7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS <sup>(1)</sup>			OUTPUT <sup>(2)</sup>
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

- (1) L = input low, H = input high, X = don't care  
 (2) L = output low, H = output high, Z = high impedance

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

SNx4LVC541A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

### 8.2 Typical Application

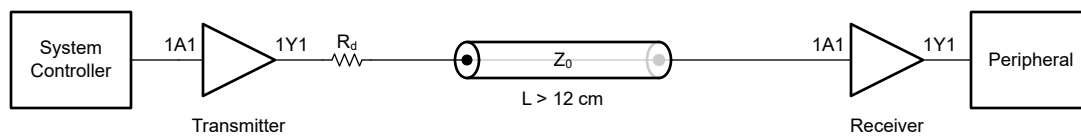


Figure 8-1. Application Schematic

#### 8.2.1 Design Requirements

##### 8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SNx4LVC541A plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Verify that the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SNx4LVC541A plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into the ground connection. Verify that the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SNx4LVC541A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied; however, do not exceed 50pF.

The SNx4LVC541A can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SNx4LVC541A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

The SNx4LVC541A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the Electrical Characteristics table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that can be in opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is  $\leq 50$ pF. Low load capacitance can be accomplished by providing short, appropriately sized traces from the SNx4LVC541A to the receiving device.
3. Verify that the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Never violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in M $\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

### 8.2.3 Application Curves

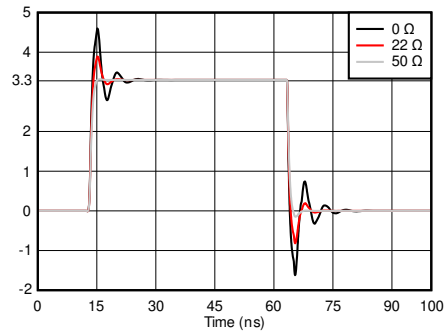


Figure 8-2. Simulated Signal Integrity at the Receiver With Different Damping Resistor ( $R_d$ ) Values

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal must have a good bypass capacitor to prevent power disturbance.

A  $0.1\mu\text{F}$  capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The  $0.1\mu\text{F}$  and  $1\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid  $90^\circ$  corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

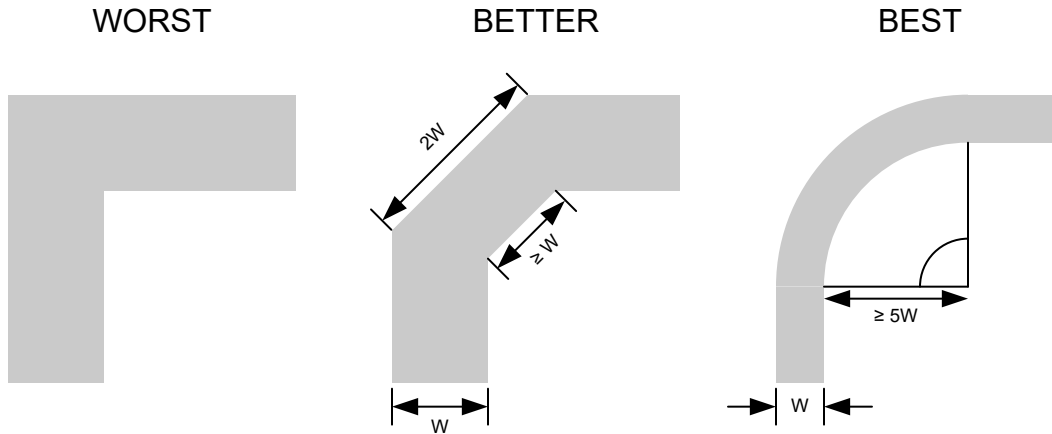


Figure 8-3. Example Trace Corners for Improved Signal Integrity

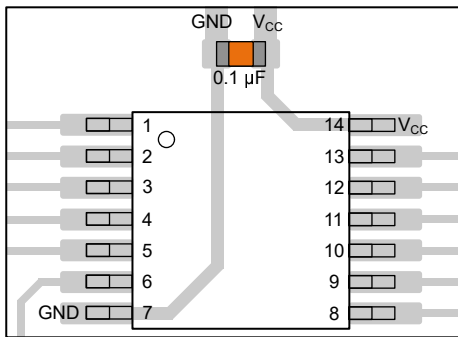


Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages

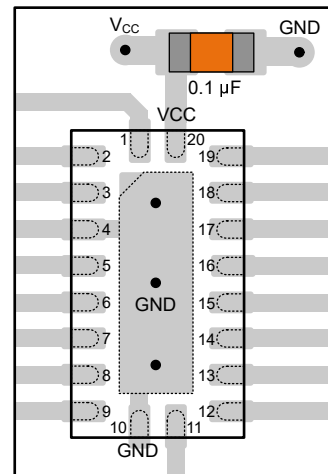


Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages

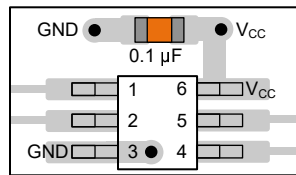


Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

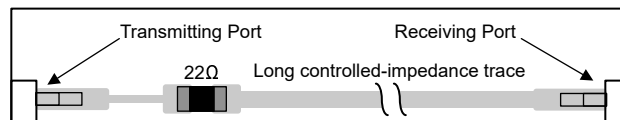


Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
 All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from June 1, 2014 to June 17, 2026 (from Revision N (June 2014) to Revision O (June 2026))

	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Moved ESD ratings to <i>ESD Ratings</i> table.....	1
• Updated latch-up ratings to latest standards.....	1
• Updated <i>Device Information</i> format and included package size.....	1
• Updated <i>Simplified Schematic</i> .....	1
• Updated <i>Applications</i> .....	1
• Added DGS and RKS package information.....	1
• Changed R $\theta$ JA for DB package from: 112.1°C/W to: 121.7°C/W.....	6
• Changed R $\theta$ JC(top) for DB package from: 73.6°C/W to: 86.8°C/W.....	6

• Changed $\Psi$ JT for DB package from: 67.3°C/W to: 87.8°C/W.....	6
• Changed $\Psi$ JB for DB package from: 33.3°C/W to: 44.7°C/W.....	6
• Changed R $\theta$ JC(bot) for DB package from: 66.9°C/W to: 87°C/W.....	6
• Changed R $\theta$ JA for DW package from: 99.4°C/W to: 114.8°C/W.....	6
• Changed R $\theta$ JC(top) for DW package from: 66.9°C/W to: 84.1°C/W.....	6
• Changed $\Psi$ JT for DW package from: 66.9°C/W to: 88.8°C/W.....	6
• Changed $\Psi$ JB for DW package from: 33.8°C/W to: 55.8°C/W.....	6
• Changed R $\theta$ JC(bot) for DW package from: 66.5°C/W to: 87.8°C/W.....	6
• Changed R $\theta$ JA for NS package from: 90.3°C/W to: 116.3°C/W.....	6
• Changed R $\theta$ JC(top) for NS package from: 56.6°C/W to: 82.4°C/W.....	6
• Changed $\Psi$ JT for NS package from: 57.8°C/W to: 86.2°C/W.....	6
• Changed $\Psi$ JB for NS package from: 28.7°C/W to: 43.9°C/W.....	6
• Changed R $\theta$ JC(bot) for NS package from: 57.4°C/W to: 85.5°C/W.....	6
• Changed R $\theta$ JA for PW package from: 100.8°C/W to: 120.3°C/W.....	6
• Changed R $\theta$ JC(top) for PW package from: 35.2°C/W to: 62.5°C/W.....	6
• Changed $\Psi$ JT for PW package from: 51.8°C/W to: 82.4°C/W.....	6
• Changed $\Psi$ JB for PW package from: 2.2°C/W to: 16°C/W.....	6
• Changed R $\theta$ JC(bot) for PW package from: 51.2°C/W to: 81.5°C/W.....	6
• Added parallel trace spacing recommendation to layout guidelines. Changed wording of "Avoid branches; buffer signals that must branch separately" to "Avoid branches; buffer each signal that must branch separately".....	14

**Changes from Revision M (May 2005) to Revision N (June 2014)**

**Page**

• Updated document to new TI data sheet format.....	1
• Removed Ordering Information table.....	1
• Updated I <sub>off</sub> Feature bullet.....	1
• Updated Features to include Military Disclaimer.....	1
• Added Device Information table.....	1
• Added Applications .....	1
• Changed MAX operating free-air temperature from 85°C to 125°C for SN74LVC541A.....	6
• Updated Thermal Information table. ....	6
• Added –40°C TO 125°C temperature range to Electrical Characteristics table for SN74LVC541A.....	7
• Added Switching Characteristics table –40°C TO 125°C temperature range for SN74LVC541A.....	8
• Added Typical Characteristics.....	8

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-9759501Q2A</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501Q2A SNJ54LVC541AFK
<a href="#">5962-9759501QRA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501QRA SNJ54LVC541AJ
<a href="#">5962-9759501QSA</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501QSA SNJ54LVC541AW
<a href="#">SN74LVC541ADBR</a>	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADBR.A	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADBR.B	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADBRG4	Active	Production	SSOP (DB)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541ADGSR</a>	Active	Production	VSSOP (DGS)   20	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C541A
<a href="#">SN74LVC541ADGVR</a>	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADGVR.B	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADGVRE4	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541ADGVRG4	Active	Production	TVSOP (DGV)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541ADW</a>	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADW.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADWG4	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADWG4.B	Active	Production	SOIC (DW)   20	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
<a href="#">SN74LVC541ADWR</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADWR.A	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADWR.B	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ADWRE4	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ANS.B	Active	Production	SOP (NS)   20	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC541A
SN74LVC541ANS.G4	Active	Production	SOP (NS)   20	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ANS.G4.B	Active	Production	SOP (NS)   20	40   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
<a href="#">SN74LVC541ANSR</a>	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC541ANSR.A	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
SN74LVC541ANSR.B	Active	Production	SOP (NS)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC541A
<a href="#">SN74LVC541APW</a>	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APW.B	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWG4	Active	Production	TSSOP (PW)   20	70   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541APWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWR.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWR.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWRE4	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541APWRG4</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWRG4.A	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWRG4.B	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541APWT</a>	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
SN74LVC541APWT.B	Active	Production	TSSOP (PW)   20	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC541A
<a href="#">SN74LVC541ARGYR</a>	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A
SN74LVC541ARGYR.A	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A
SN74LVC541ARGYR.B	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A
SN74LVC541ARGYRG4	Active	Production	VQFN (RGY)   20	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC541A
<a href="#">SNJ54LVC541AFK</a>	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501Q2A SNJ54LVC541AFK
<a href="#">SNJ54LVC541AJ</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501QR A SNJ54LVC541AJ
<a href="#">SNJ54LVC541AW</a>	Active	Production	CFP (W)   20	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9759501QS A SNJ54LVC541AW

(1) Status: For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC541A, SN74LVC541A :**

- Catalog : [SN74LVC541A](#)
- Automotive : [SN74LVC541A-Q1](#), [SN74LVC541A-Q1](#)
- Enhanced Product : [SN74LVC541A-EP](#), [SN74LVC541A-EP](#)
- Military : [SN54LVC541A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

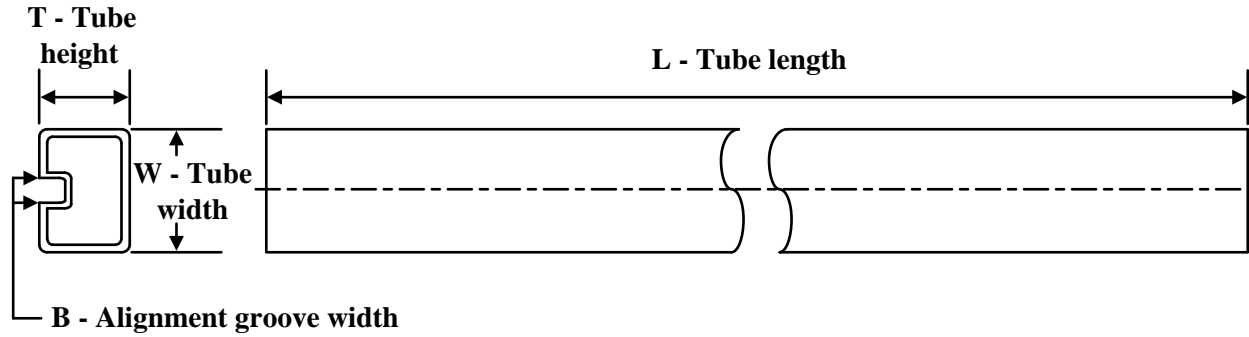

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC541ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC541ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LVC541ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC541ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVC541ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVC541APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC541APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC541APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVC541ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC541ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVC541ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LVC541ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVC541ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVC541ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVC541APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC541APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVC541APWT	TSSOP	PW	20	250	353.0	353.0	32.0
SN74LVC541ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9759501Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9759501QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LVC541ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC541ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC541ADWG4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC541ADWG4.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVC541ANS.B	NS	SOP	20	40	530	10.5	4000	4.1
SN74LVC541ANSG4	NS	SOP	20	40	530	10.5	4000	4.1
SN74LVC541ANSG4.B	NS	SOP	20	40	530	10.5	4000	4.1
SN74LVC541APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC541APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVC541APWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54LVC541AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LVC541AW	W	CFP	20	25	506.98	26.16	6220	NA

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

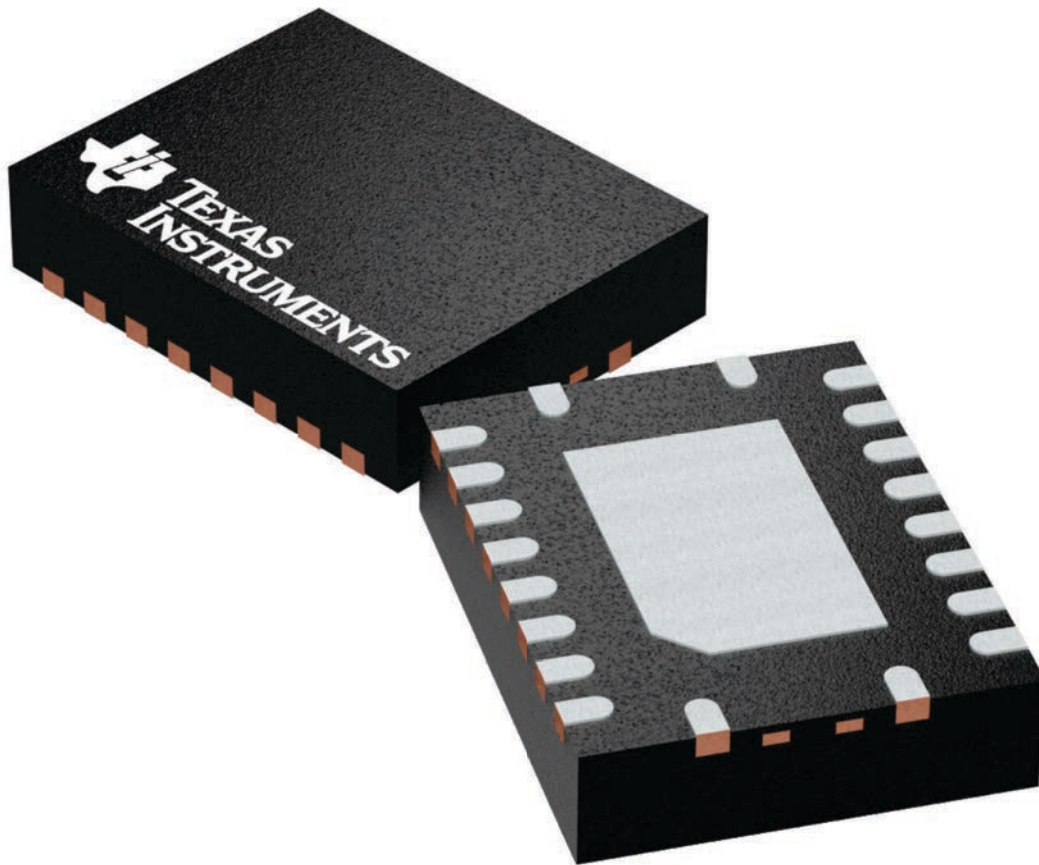
**RGY 20**

**VQFN - 1 mm max height**

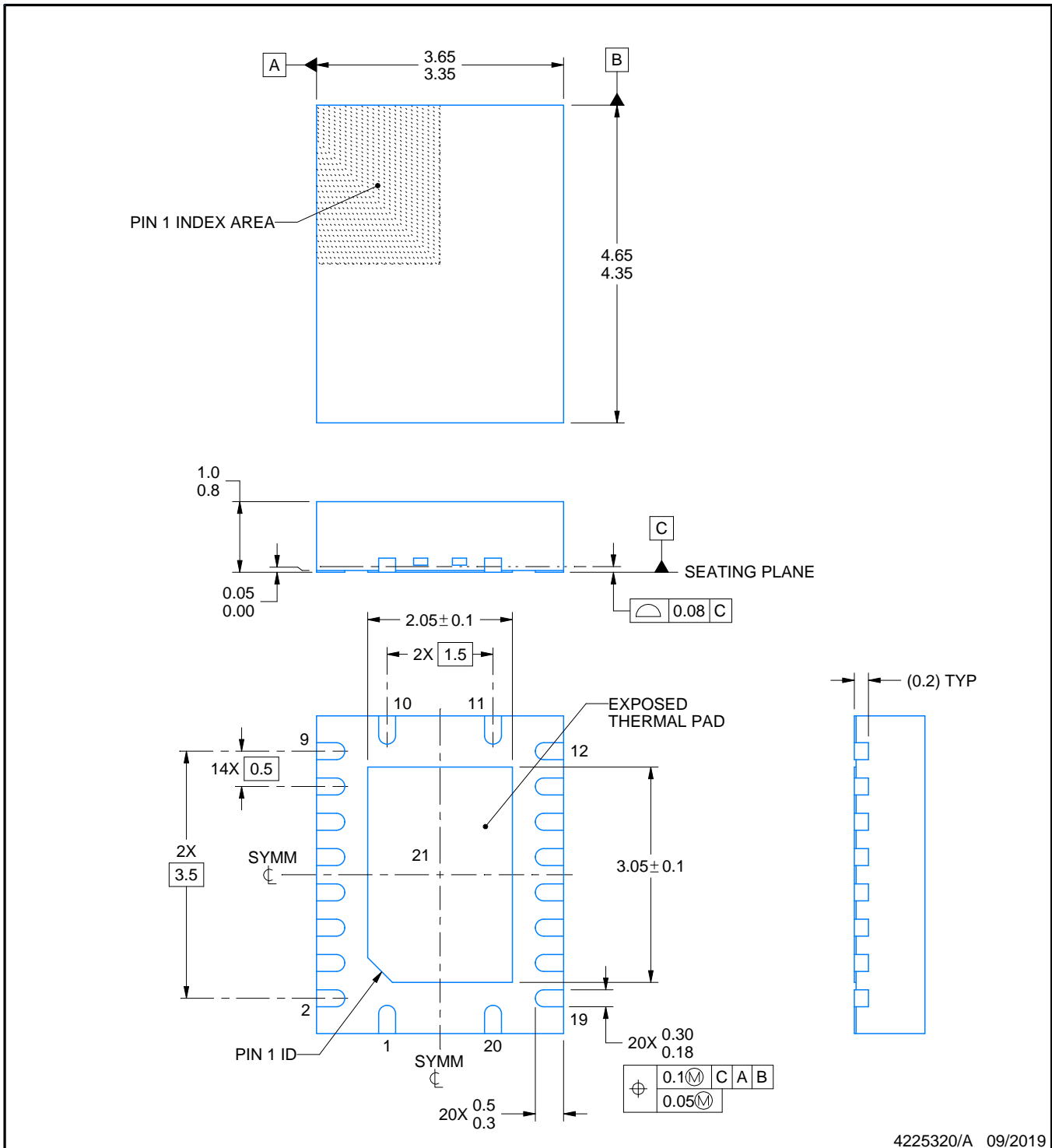
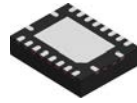
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

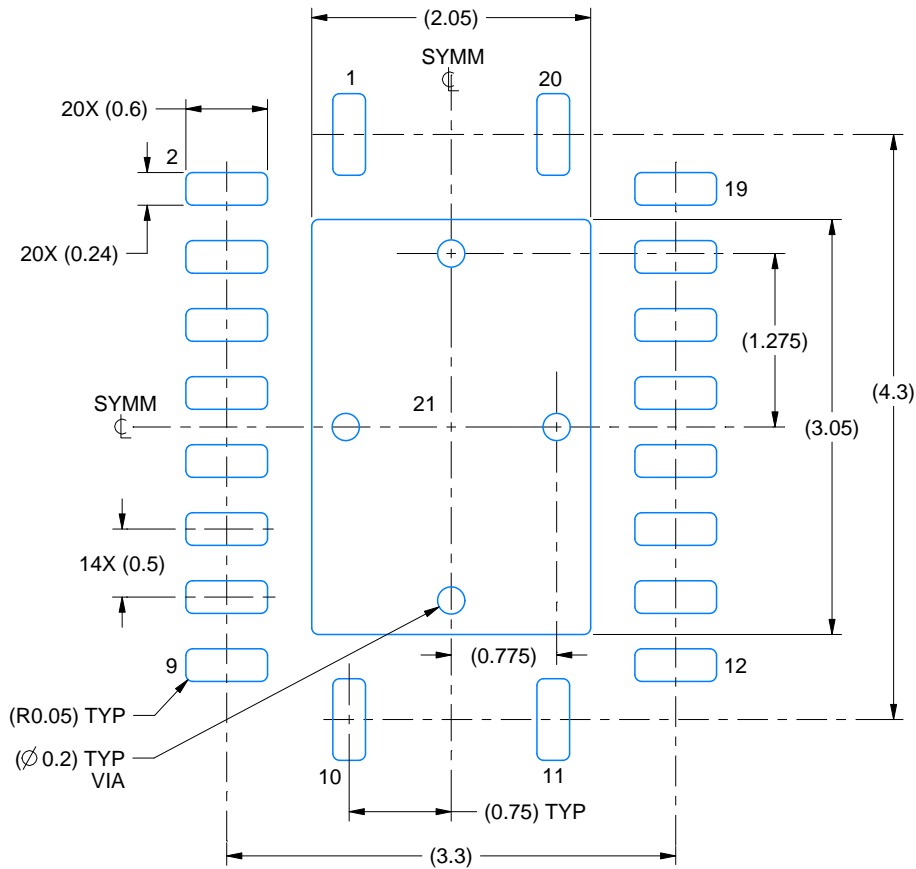
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

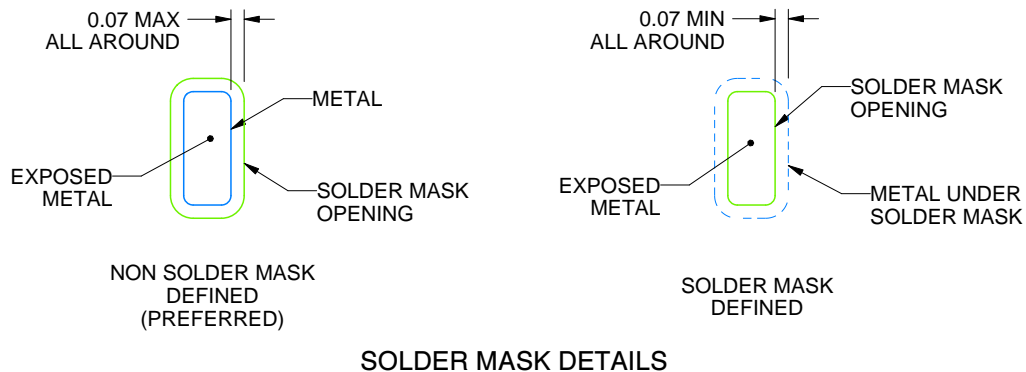
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:18X



**SOLDER MASK DETAILS**

4225320/A 09/2019

NOTES: (continued)

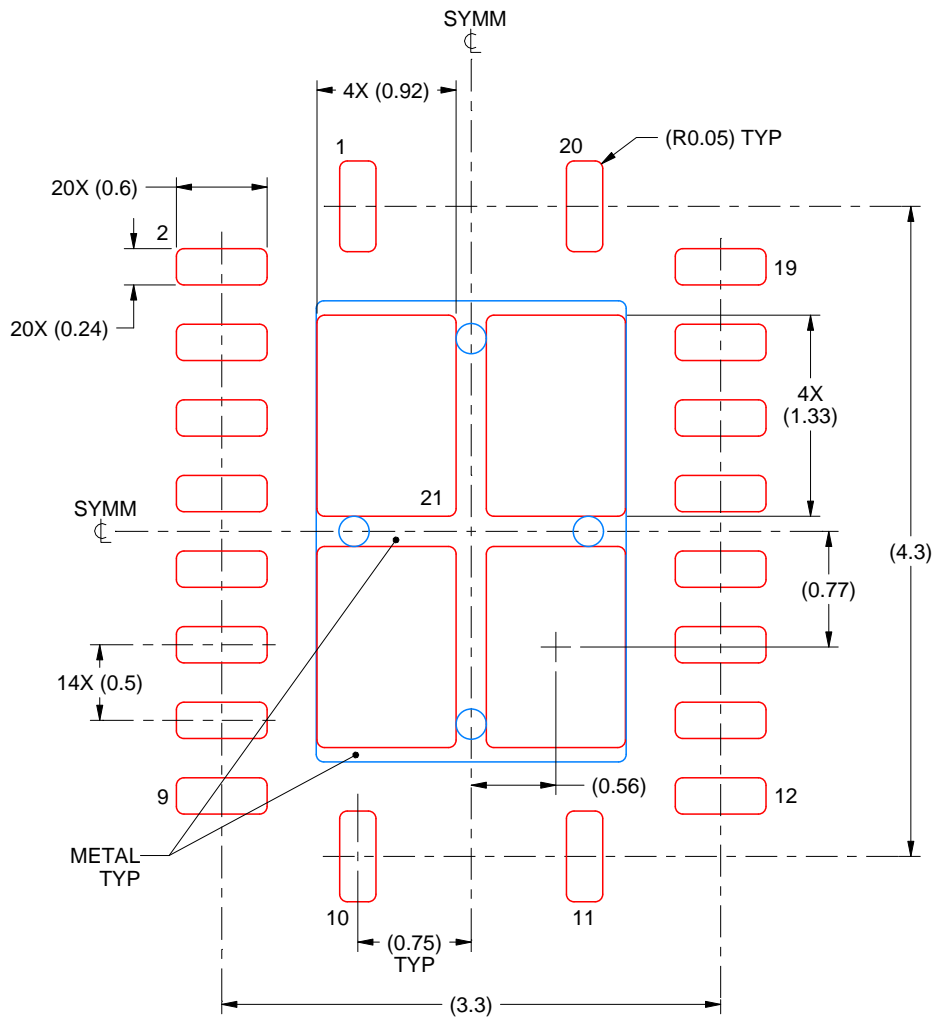
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

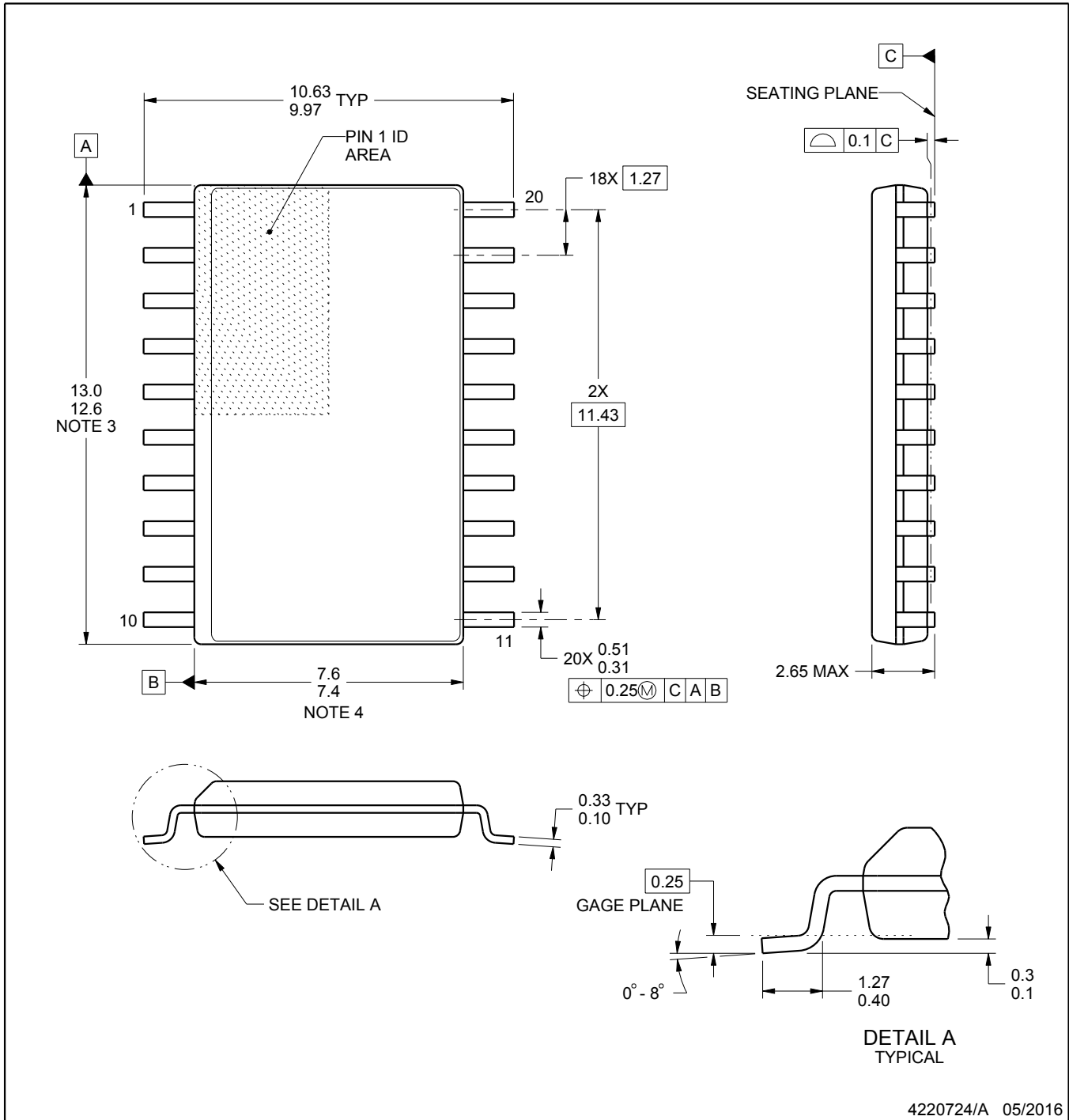
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

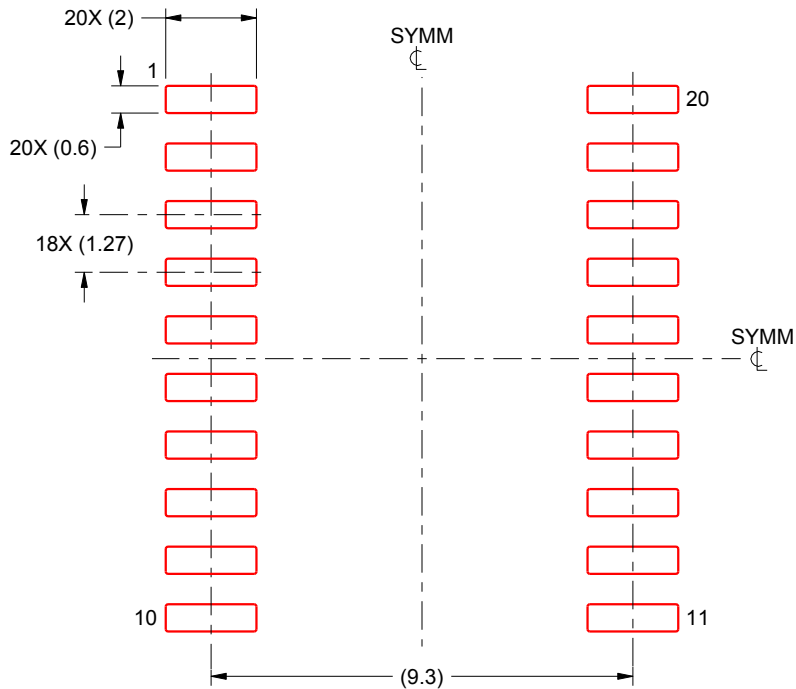
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

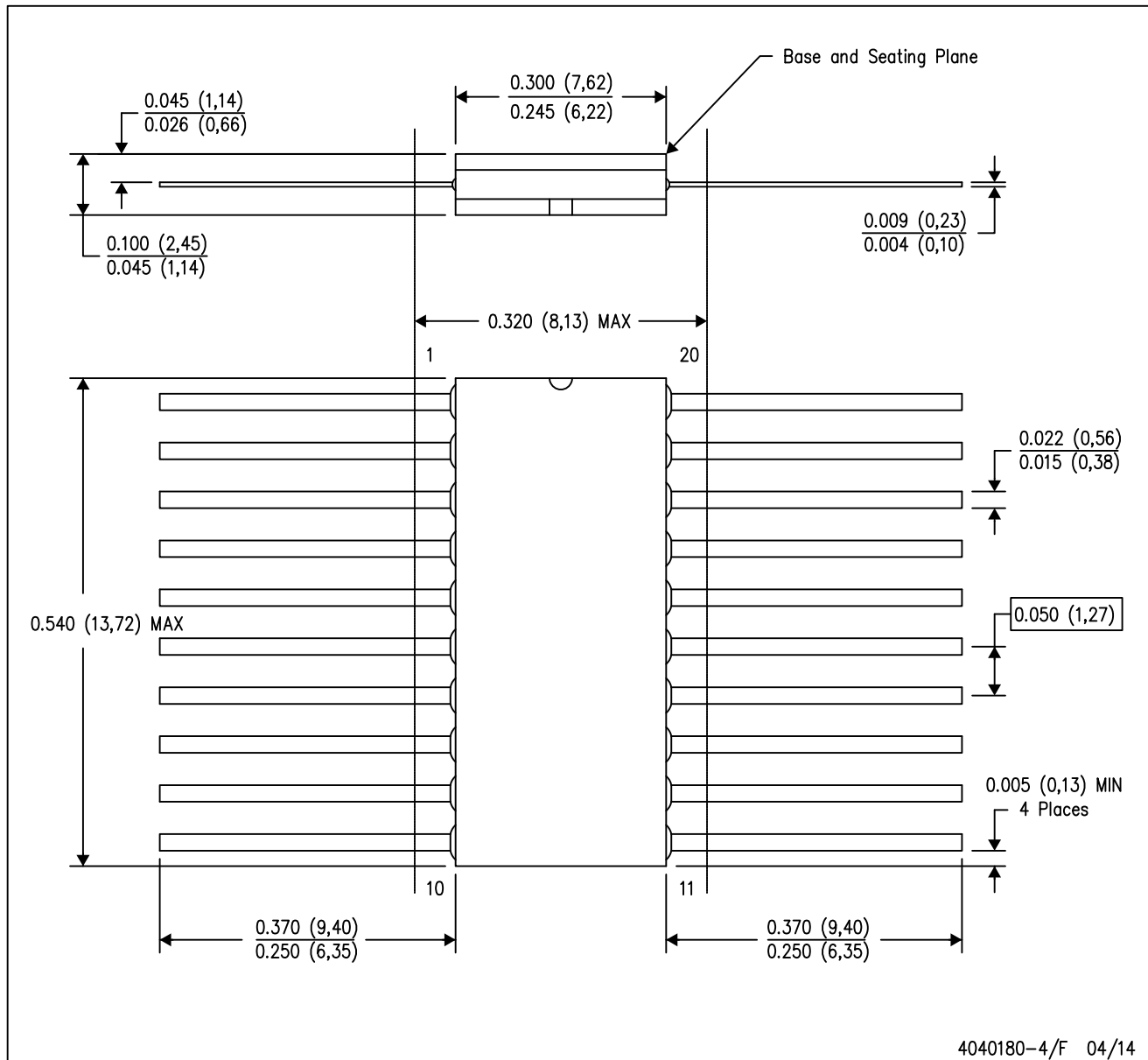
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

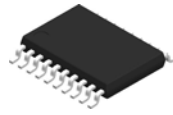
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

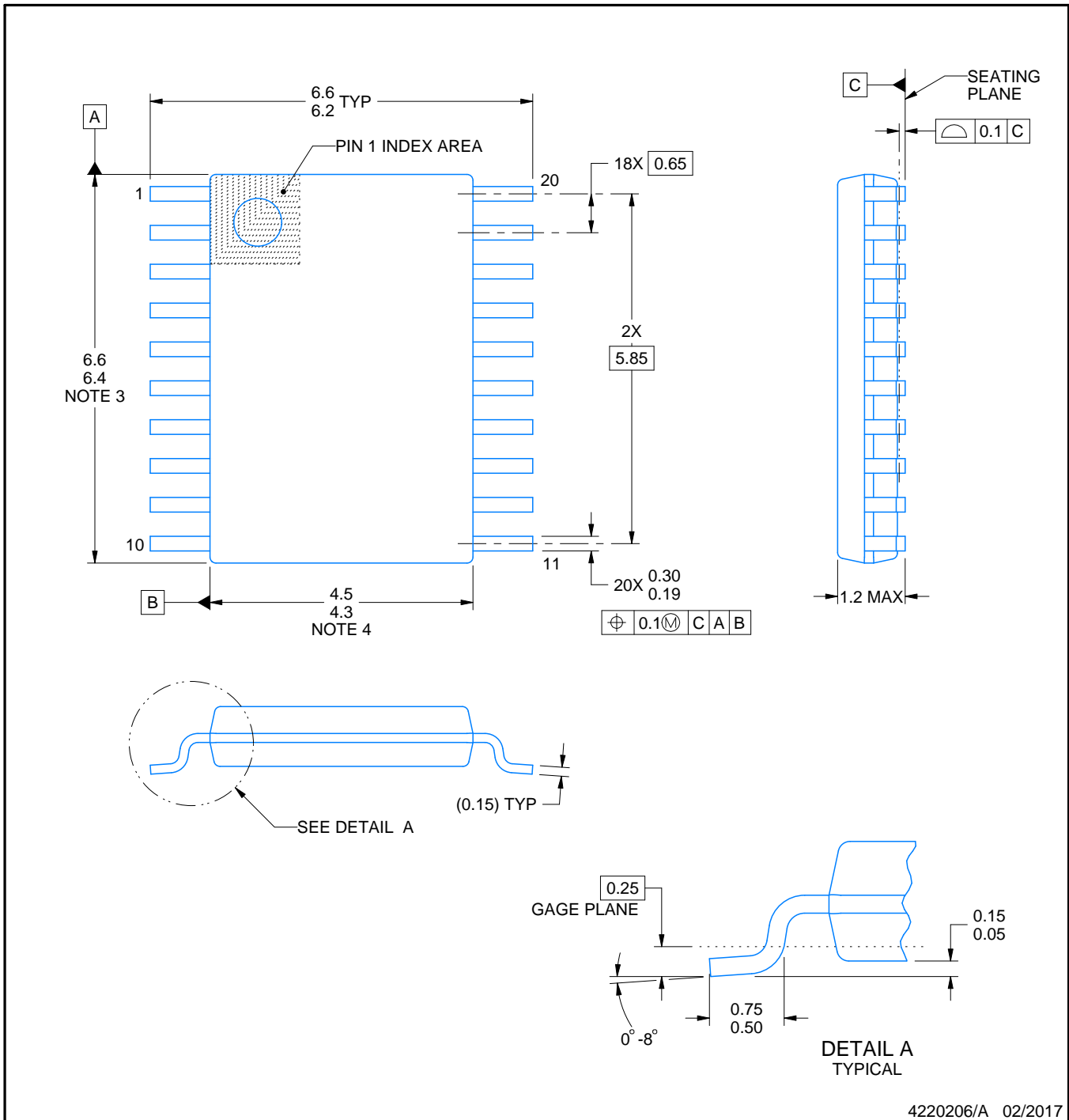
PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

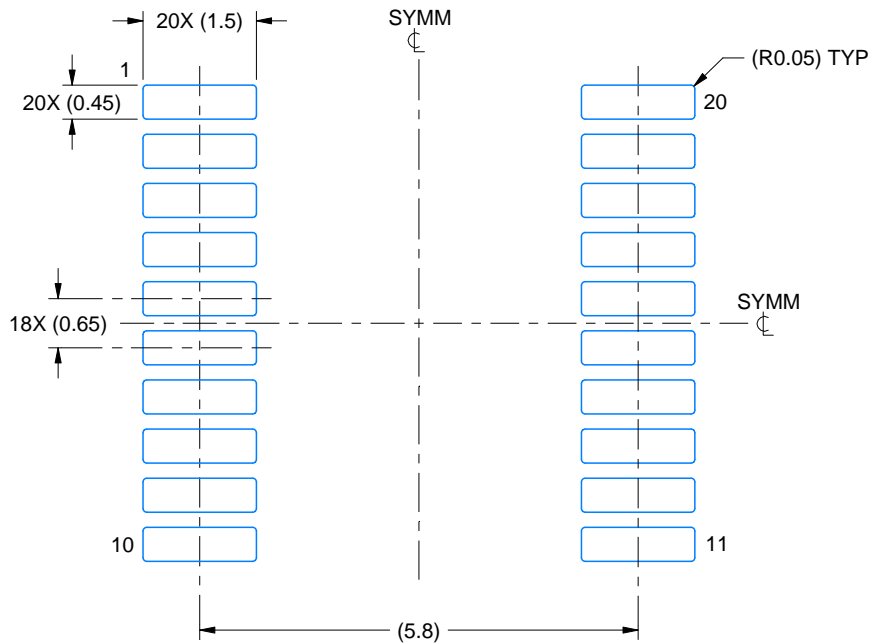
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

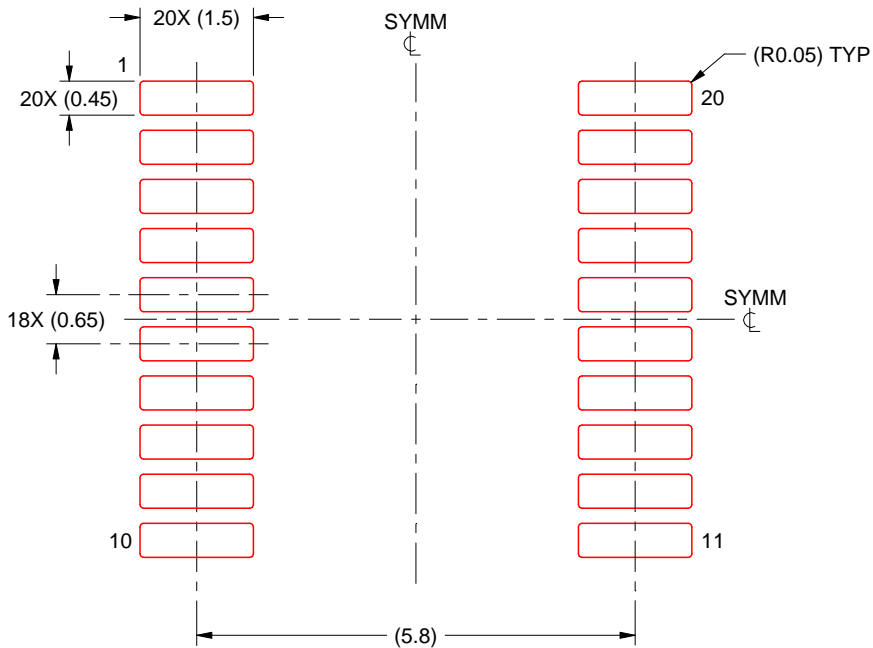
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

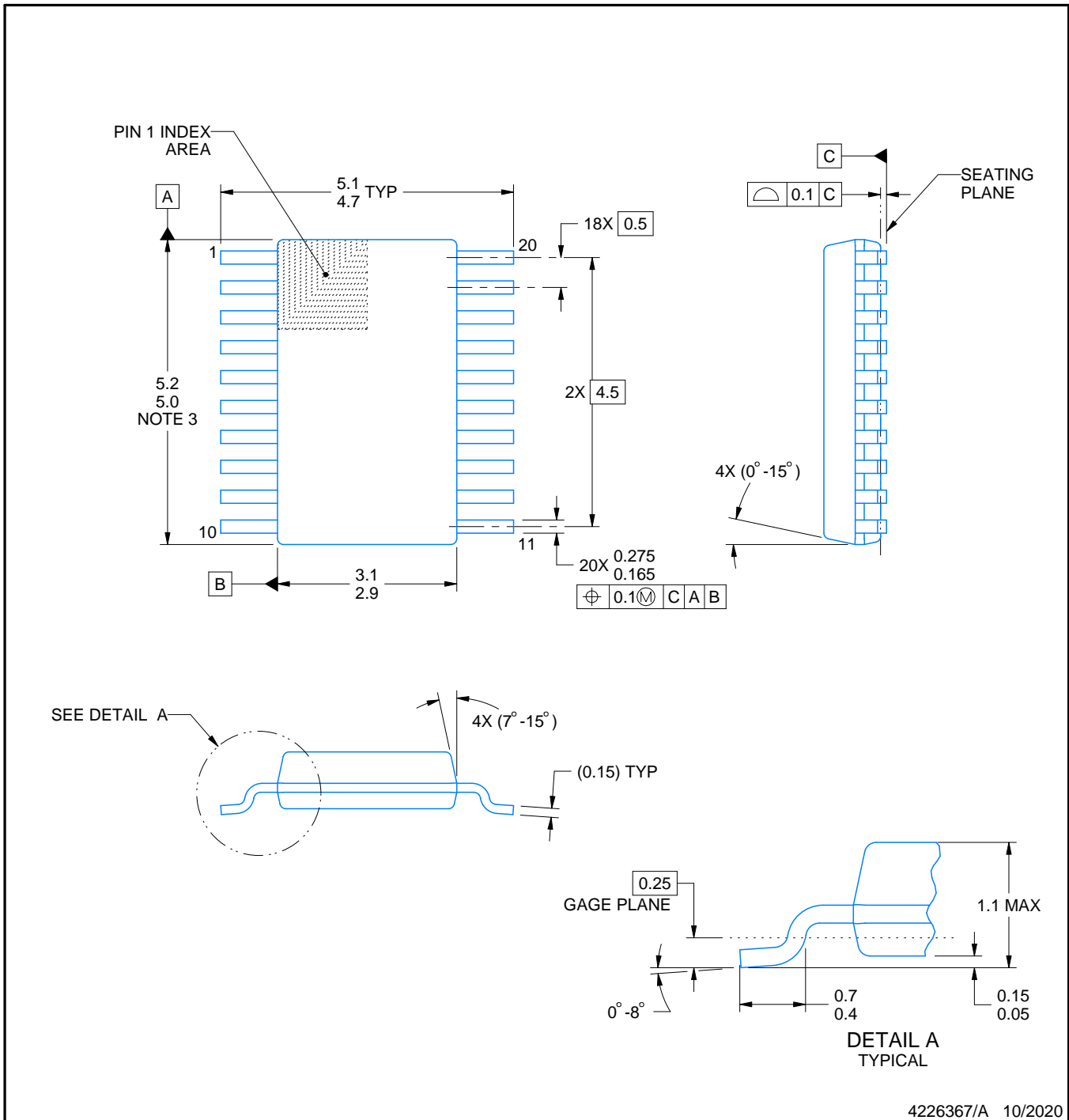
# DGS0020A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

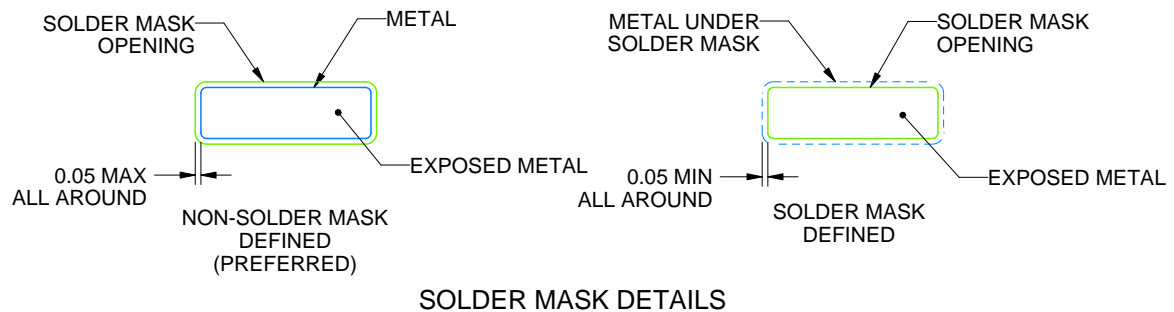
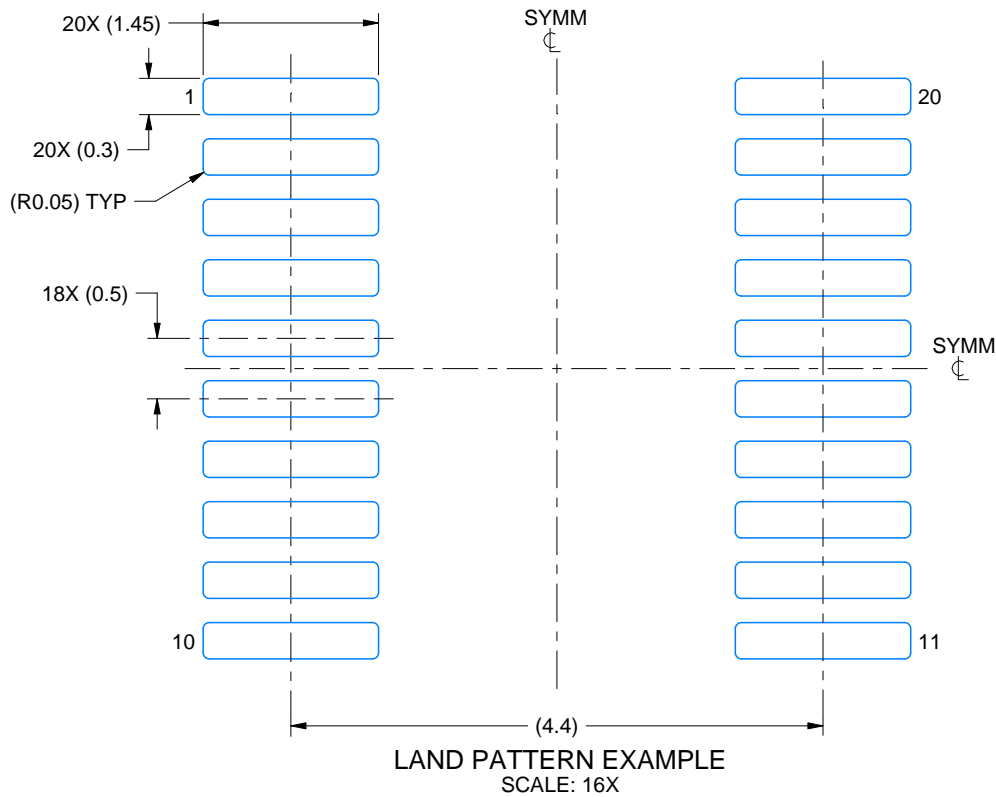
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- No JEDEC registration as of September 2020.
- Features may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

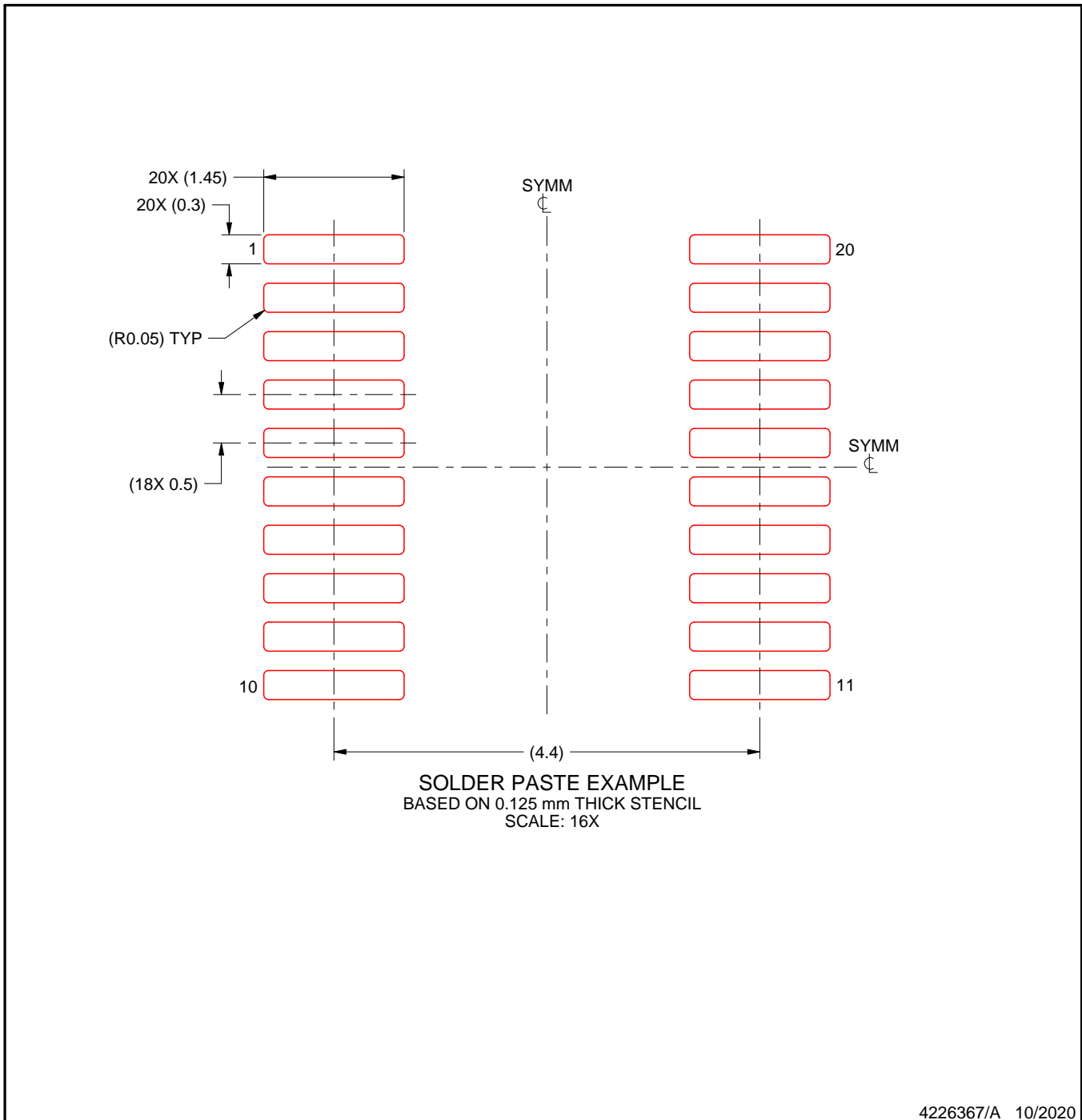
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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