SN55LVRA4-SEP Radiation Tolerant Quad Channel High-Speed Differential Receiver

1 Features

- VID V62/25606-01XE
- Total ionizing dose characterized at 30krad (Si)
  - Total ionizing dose radiation lot acceptance testing (TID RLAT) for every wafer lot to 30krad (Si)
- Single-event effects (SEE) characterized:
  - Single event latch-up (SEL) immune to linear energy transfer (LET) = 50MeV-cm2 /mg
  - Single event transient (SET) characterization report available
- 400Mbps signaling rate
- Operates with a single 3.3V supply
- –4V to 5V extended common-mode input voltage range
- Differential input thresholds < ±50mV with 50mV of hysteresis over entire common-mode input voltage range
- Complies with TIA/EIA-644 (LVDS)
- Active fail-safe assures a high-level output with no input and input remains high-impedance on power down
- Bus-pin ESD protection exceeds 15kV HBM
- TTL control inputs are 5V tolerant
- Space enhanced plastic (SEP)
  - Controlled baseline
  - Gold wire, NiPdAu lead finish
  - One assembly and test site, one fabrication site
  - Extended product life cycle
  - Military (–55°C to 125°C) temperature range
  - Product traceability
  - Meets NASA ASTM E595 outgassing specification

2 Applications

- Low Earth orbit (LEO) satellite systems
- Command & data handling (C&DH)
- Communications payload
- Optical imaging payload
- Radar imaging payload

3 Description

The SN55LVRA4-SEP offers the widest common-mode input voltage range in the industry. These receivers provide an input voltage range specification compatible with a 5V PECL signal as well as an overall increased ground-noise tolerance.

The SN55LVRA4-SEP include a failsafe circuit that provides a high-level output within 60ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. The failsafe circuit prevents noise from being received as valid data under these fault conditions.

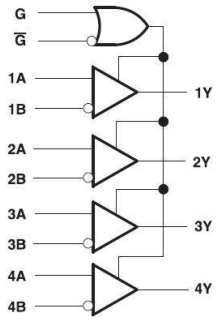
The intended application and signaling technique of these devices is point-to-point baseband data transmission over controlled impedance media of approximately 100Ω. The transmission media can be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN55LVRA4-SEP is characterized for operation from –55°C to 125°C.

Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE (2)
SN55LVRA4-SEP	D (SOIC, 16)	9.9mm × 6mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

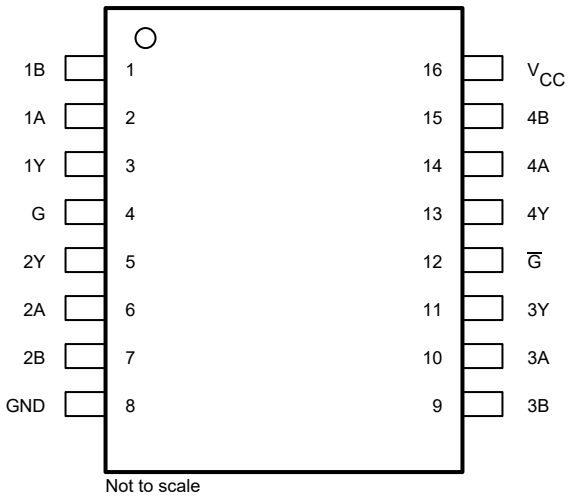


Figure 4-1. D Package 16-Pin, SOIC (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	P	Supply voltage
GND	8	G	Ground
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
1Y	3	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
2Y	5	O	LVTTL output signal
3A	10	I	Differential (LVDS) non-inverting input
3B	9	I	Differential (LVDS) inverting input
3Y	11	O	LVTTL output signal
4A	14	I	Differential (LVDS) non-inverting input
4B	15	I	Differential (LVDS) inverting input
4Y	13	O	LVTTL output signal
G	4	I	Enable (HI = ENABLE)
$\overline{G}$	12	I	Enable (LO = ENABLE)

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		–0.5	4	V
Input Voltage (A or B)		–5	6	V
Input Voltage (G, $\overline{G}$)		–0.5	VCC + 0.4	V
Differential Voltage |A - B| for LVDS		0	3	V
Output Voltage (R_{OUT})		–0.5	4	V
Lead Temperature Range Soldering	(4 sec.)		260	°C
Junction Temperature		-55	140	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended* Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, and performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(BUS\_ESD)}$	Electrostatic discharge	Bus pins; A & B; Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
$V_{(HBM\_ESD)}$	Electrostatic discharge	All other pins: Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
$V_{(CDM\_ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (3.3V mode)	3.0	3.3	3.6	V
V_{IH}	High-level input voltage (G, $\overline{G}$)	2		V_{CC}	V
V_{IL}	Low-level input voltage (G, $\overline{G}$)	0		0.8	V
$\|V_{ID}\|$	Magnitude of Receiver input voltage (LVDS)	0.1		3.0	V
V_I or V_{CM}	Voltage at any LVDS terminal (separately or common-mode)	-4		+5	V
T_A	Operating free-air temperature	-55		125	°C
T_{PCB}	PCB temperature (Standard)	-55		128	°C
T_J	Junction temperature (Standard)	-55		135	°C

5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT1}	Positive-going differential input voltage threshold	V_{IB} = -4V or 5V, V_{CC} = 3.0V to 3.6V, See Figure 6-2			90	mV
V_{IT2}	Negative-going differential input voltage threshold		-90			
V_{IT3}	Differential input failsafe voltage threshold	V_{CC} = 3.0V to 3.6V See Figure 6-2 and Figure 6-5	-32		-100	mV
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT1} – V_{IT2}$	V_{CC} = 3.0V to 3.6V		50		mV
V_{CM_RANGE}	Input common mode voltage range	VCC = 3.0V to 3.6V	-4	1.2	5	V
V_{OH}	High-level output voltage	I_{OH} = –4mA, V_{CC} = 3.0V to 3.6V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4mA, V_{CC} = 3.0V to 3.6V			0.4	V
I_{CC}	Supply current	G at V_{CC}, No load, Steady-state VID=200mV/-200mV, V_{CC} = 3.0V to 3.6V	2	16	25	mA
		Disable and in deep sleep (Disable for >100us), G at GND, V_{CC} = 3.0V to 3.6V		1.1	6	
I_I	Input current (A or B inputs)	V_I = 0V, Other input open	-25		25	µA
I_I	Input current (A or B inputs)	V_I = 2.4V, Other input open	-25		25	µA
I_I	Input current (A or B inputs)	V_I = –4V, Other input open	-80		80	µA
I_I	Input current (A or B inputs)	V_I = 5V, Other input open	-45		45	µA
I_{ID}	Differential input current ($I_{IA} – I_{IB}$)	V_{ID} = 100 mV, V_{IC} = –4V or 5V	-5		5	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = –4V or 5V, V_{CC} = 0V	-70		70	µA
$I_{I(OFF)}$	Power-off input current (A or B inputs)	V_A or V_B = 0V or 2.4V, V_{CC} = 0V	-25		25	µA
V_{IH}	High-level input voltage (enables)	V_{CC} = 3.0V to 3.6V			2	V
I_{IH}	High-level input current (enables)	V_{IH} = 2V, V_{CC} 3.0V to 3.6V			15	µA
V_{IL}	Low-level input voltage (enables)	V_{CC} = 3.0V to 3.6V	0.8			V
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8V, V_{CC} 3.0V to 3.6V			15	µA
I_{OZ}	High-impedance output current		-12		12	µA

5.6 Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1) (2) (3)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
t_{PHL}	Differential Propagation Delay High to Low	-55℃ ≤ T_A ≤ 125℃, V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See Figure 6-3	1.8	3.6	8.5	ns
t_{PLH}	Differential Propagation Delay Low to High	-55℃ ≤ T_A ≤ 125℃, V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See Figure 6-3	1.3	3	7.5	ns
t_{d1}	Delay time, failsafe deactivate time	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See Figure 6-3 and Figure 6-6			16	ns
t_{d2}	Delay time, failsafe activate time				2.5	µs
$tSK_{(p)}$	Differential Pulse Skew (t_{PHLD} – t_{PLHD}) (4)	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See Figure 6-3		500		ps
$t_{SK(o)}$	Differential Channel-to-Channel Skew-same device (5)			130		ps
$t_{SK(pp)}$	Differential Part to Part Skew (6)				1.2	ns
t_{TPHZ}	Propagation delay time, high level-to-high impedance output	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10% Figure 6-4		6.5	15	ns
t_{TPLZ}	Propagation delay time, low level-to-high impedance output			4.4	12	ns
t_{TPZH}	Propagation delay time, high impedance to high level output			3.8	12	ns
t_{TPZL}	Propagation delay time, high impedance to low level output			7	12	ns
t_{TLH}	Output Rise Time	V_{ID} = 400mV, C_L = 10pF, trf≤1ns, VCC=3.3V +/-10%. See Figure 6-3		800		ps
t_{THL}	Output Fall Time			800		ps

(1) All typicals are given for: V_{CC} = 3.3V and T_A = +25°C.
(2) C_L includes probe and jig capacitance.
(3) Generator waveform for all tests unless otherwise specified: f = 1MHz, Z_O = 50Ω, t_r and t_f (0% to 100%) ≤ 3ns for R_{IN}.
(4) $t_{SK(p)}$ is the magnitude difference in differential propagation delay time between the positive-going-edge and the negative-going-edge of the same channel.
(5) $t_{SK(o)}$ is the differential channel-to-channel skew of any event on the same device. This specification applies to devices having multiple receivers within the integrated circuit.
(6) $t_{SK(pp)}$, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

5.7 Typical Characteristics

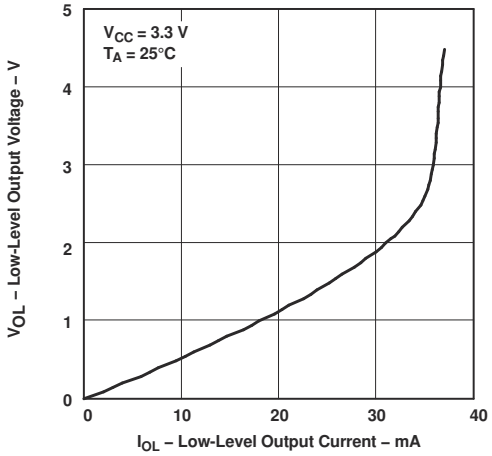


Figure 5-1. Low-Level Output Voltage vs Low-Level Output Current

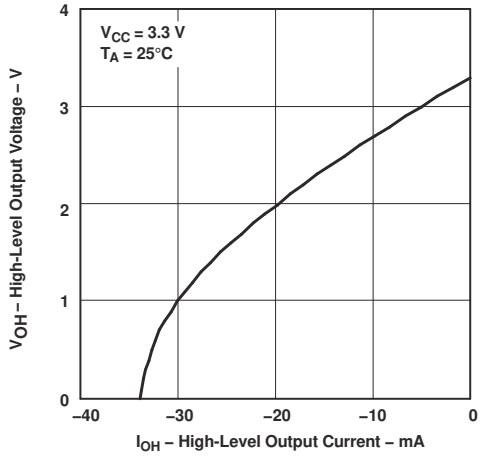


Figure 5-2. High-Level Output Voltage vs High-Level Output Current

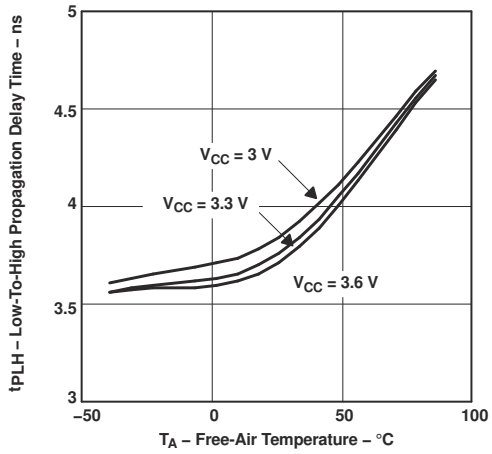


Figure 5-3. Low-to-High Propagation Delay Time vs Free-Air Temperature

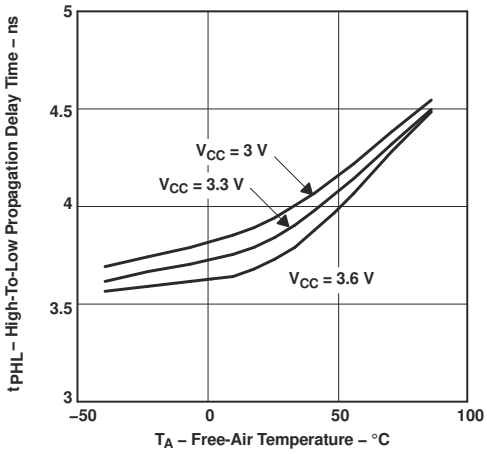


Figure 5-4. High-to-Low Propagation Delay Time vs Free-Air Temperature

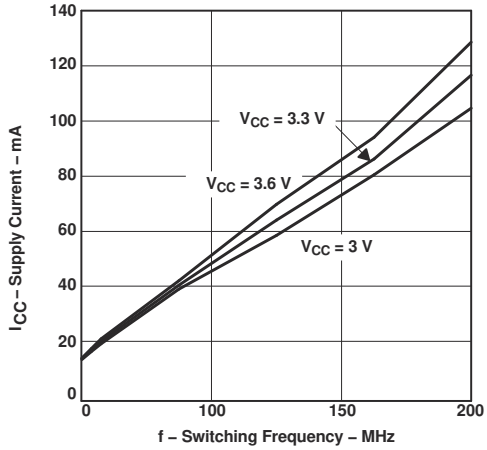


Figure 5-5. Supply Current vs Frequency (all channels active)

6 Parameter Measurement Information

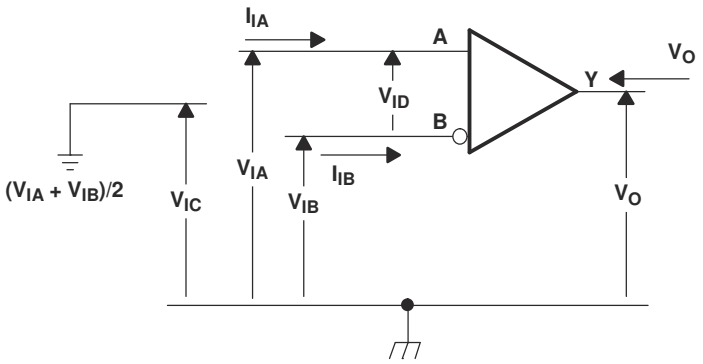
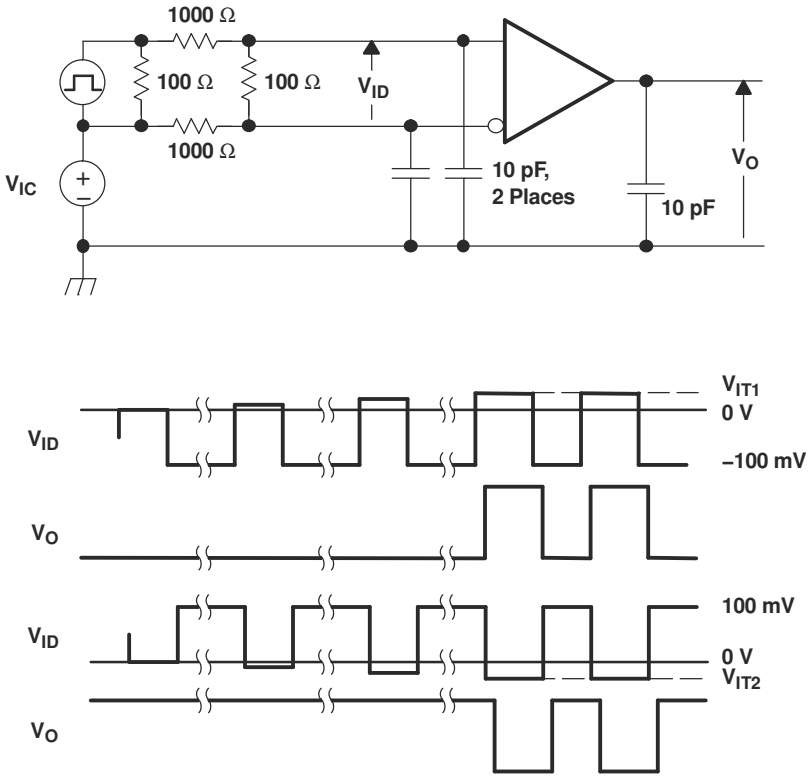
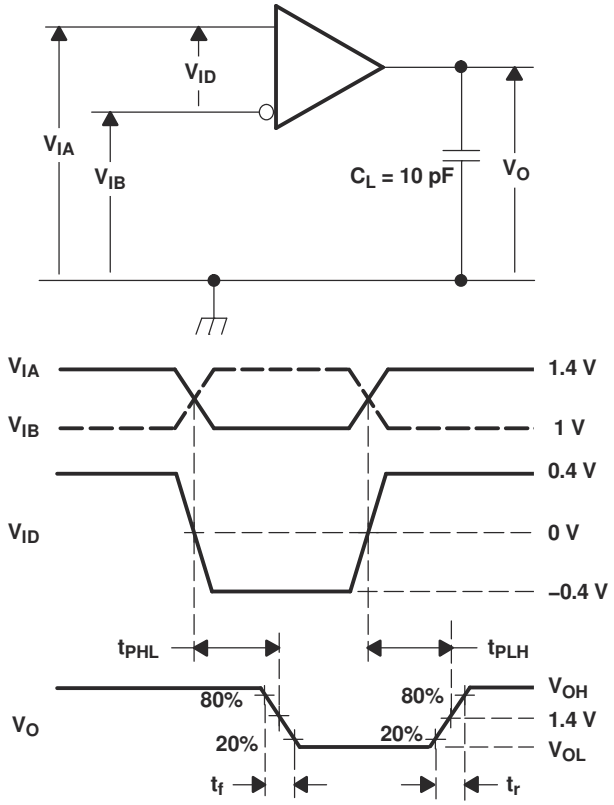


Figure 6-1. Voltage and Current Definitions



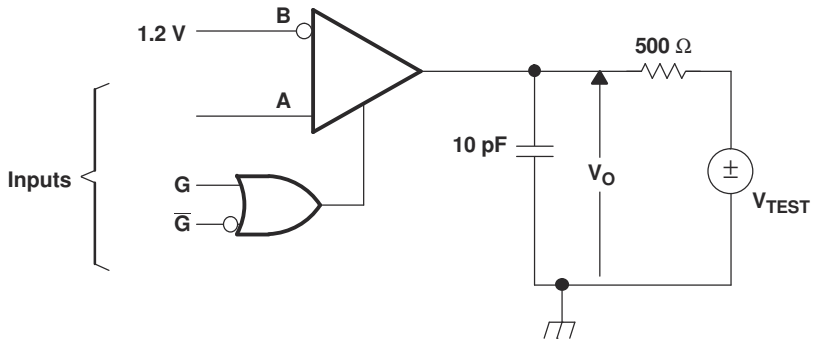
NOTE: Input signal of 3 Mpps, duration of 167 ns, and transition time of <1 ns.

Figure 6-2. V_{IT1} and V_{IT2} Input Voltage Threshold Test Circuit and Definitions



All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1ns, pulse repetition rate (PRR) = 50Mpps [pps : pulse per second], pulse width = 10 ±0.2ns . C_L includes instrumentation and fixture capacitance within 0,06mm of the D.U.T.

Figure 6-3. Timing Test Circuit and Waveforms



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ±10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

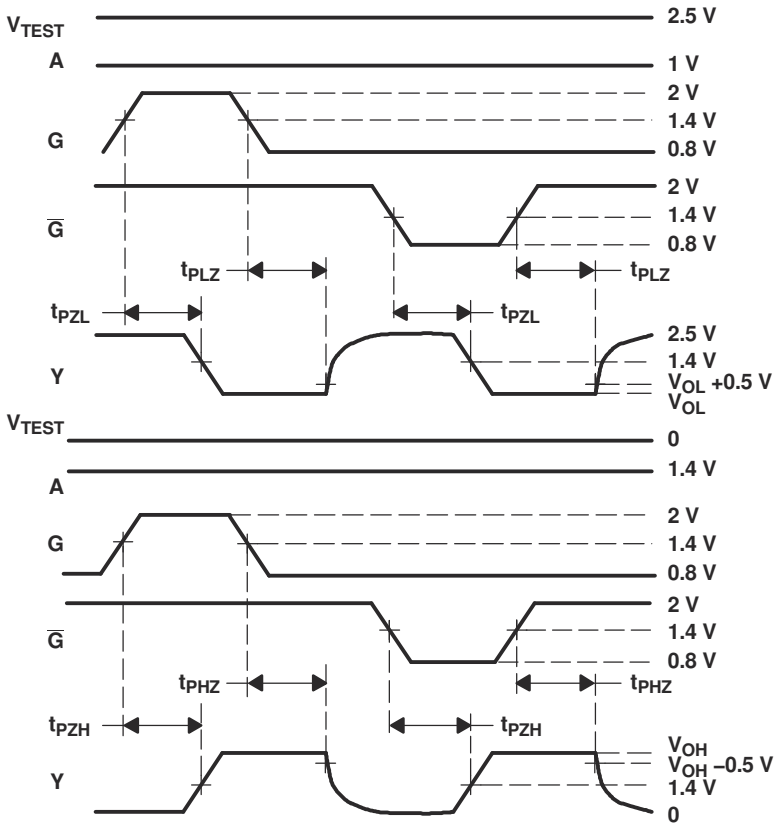


Figure 6-4. Enable/Disable Time Test Circuit and Waveforms

Table 6-1. Receiver Minimum and Maximum V_{IT3} Input Threshold Test Voltages

APPLIED VOLTAGES(1)		RESULTANT INPUTS		
V_{IA} (mV)	V_{IB} (mV)	V_{ID} (mV)	V_{IC} (mV)	Output
–4000	–3900	–100	–3950	L
–4000	–3968	–32	–3984	H
4900	5000	–100	4950	L
4968	5000	–32	4984	H

(1) These voltages are applied for a minimum of 1.5µs.

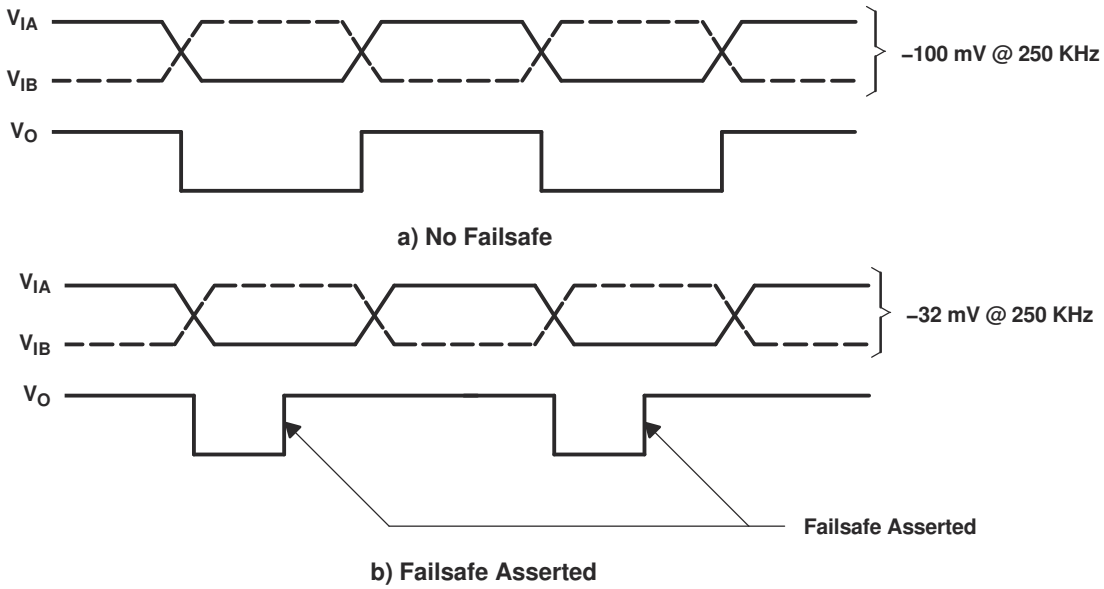


Figure 6-5. V_{IT3} Failsafe Threshold Test

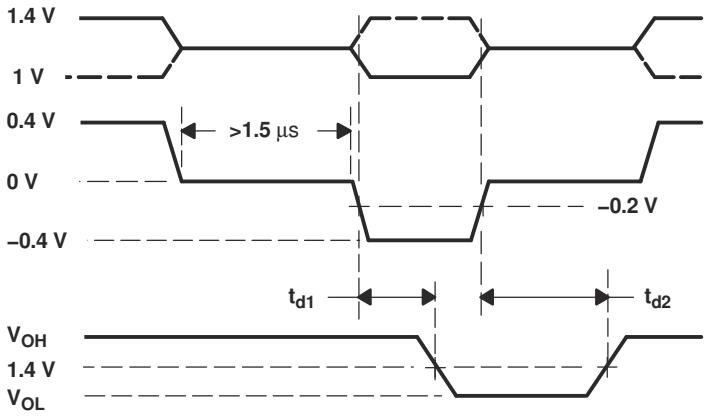


Figure 6-6. Waveforms for Failsafe Activate and Deactivate

7 Detailed Description

7.1 Overview

Figure 7-1 shows how LVDS drivers and receivers are intended to be used primarily in a simple point-to-point configuration. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the source through a impedance controlled 100Ω differential PCB traces. Use a termination resistor of 100Ω and place it as close to the receiver input pins as possible. The termination resistor converts the driver output (current mode) into a voltage that is detected by the receiver.

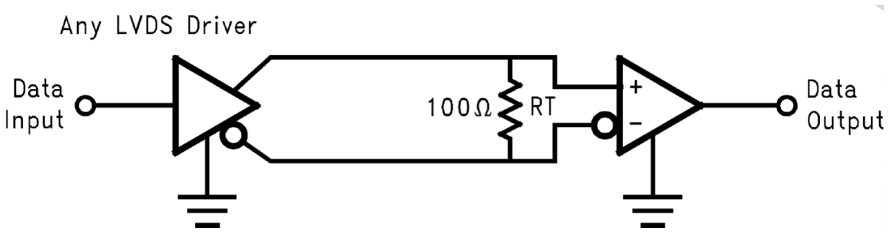
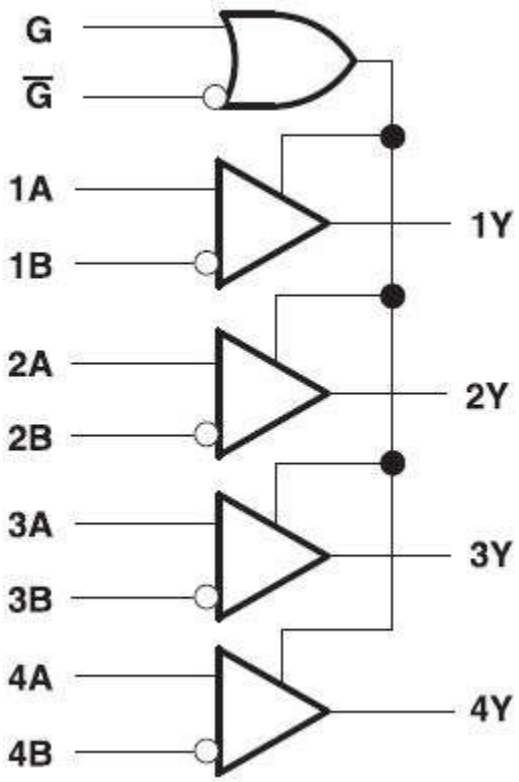


Figure 7-1. Application Diagram

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Receiver Output States

When the receiver differential input signal is greater than 100mV, the receiver output is high; and when the differential input voltage is below –100mV, the receiver output is low. When the input voltage is between these thresholds (for example, between –100mV and 100mV), the receiver output is indeterminate. The output state can be high or low. A special case occurs when the input to the receiver is open-circuited, which is covered in *Section 8.3*. When the receiver is disabled, the receiver outputs are high-impedance.

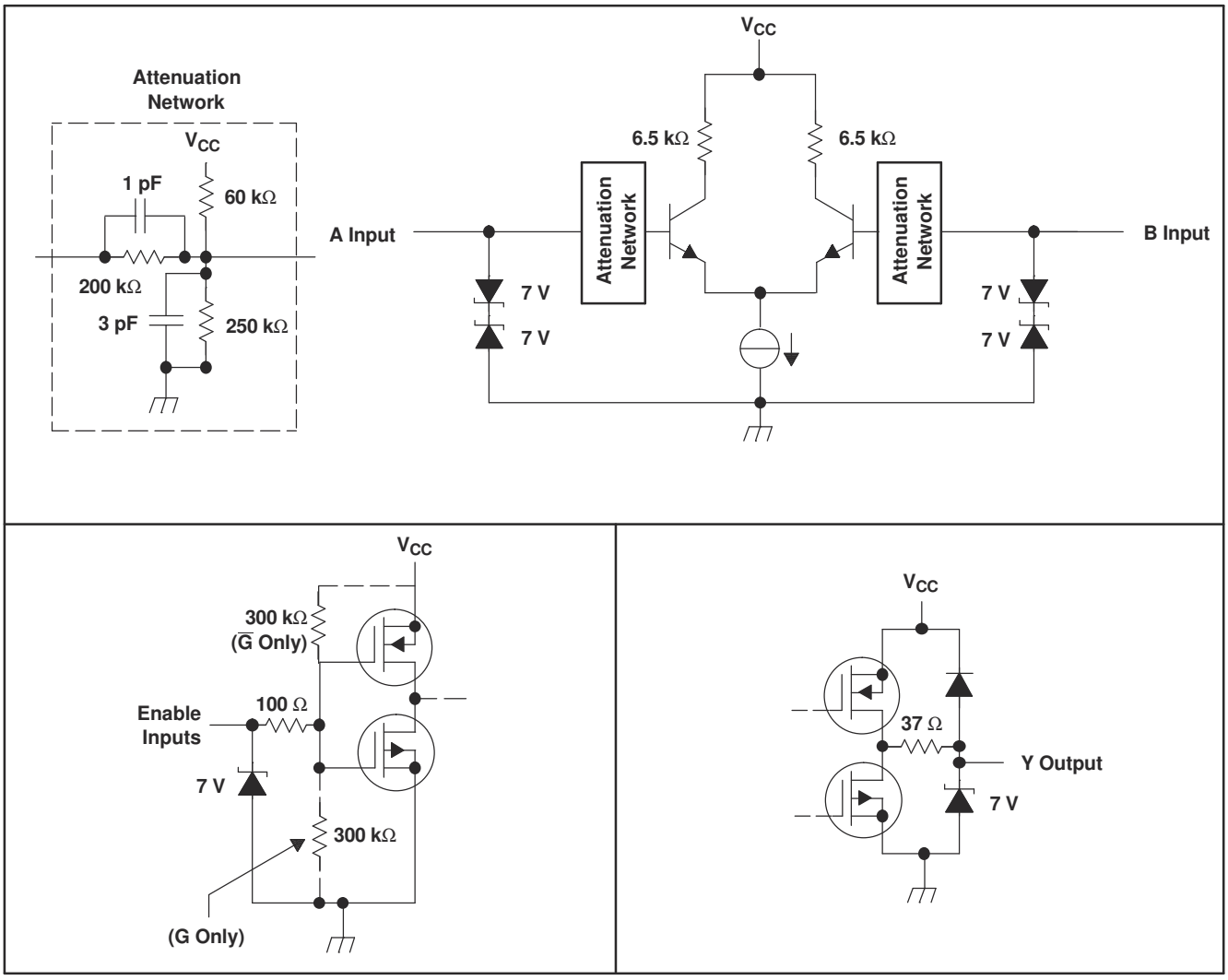
7.3.2 General Purpose Comparator

While the SN55LVRA4-SEP receivers are LVDS standard-compliant receivers, utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output follows a faithful representation of the input signal.

7.3.3 Common-Mode Range vs Supply Voltage

The SN55LVRA4-SEP receivers operate over an input extended common-mode range of -4V to 5V, allowing significant amount of ground shift between transmitter and receiver. If the input common mode is anywhere within this range and has a differential magnitude greater than or equal to 100mV, the receivers correctly output the LVDS bus state.

7.4 Equivalent Input and Output Schematic Diagrams



7.5 Device Functional Modes

Table 7-1. Function Table

SN55LVRA4-SEP (1)			
DIFFERENTIAL INPUT	ENABLES		OUTPUT
$V_{ID} = V_A - V_B$	G	$\overline{G}$	Y
$V_{ID} \geq -32mV$	H	X	H
	X	L	H
$-100\ mV < V_{ID} \leq -32mV$	H	X	?
	X	L	?
$V_{ID} \leq -100mV$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

8 Application and Implementation

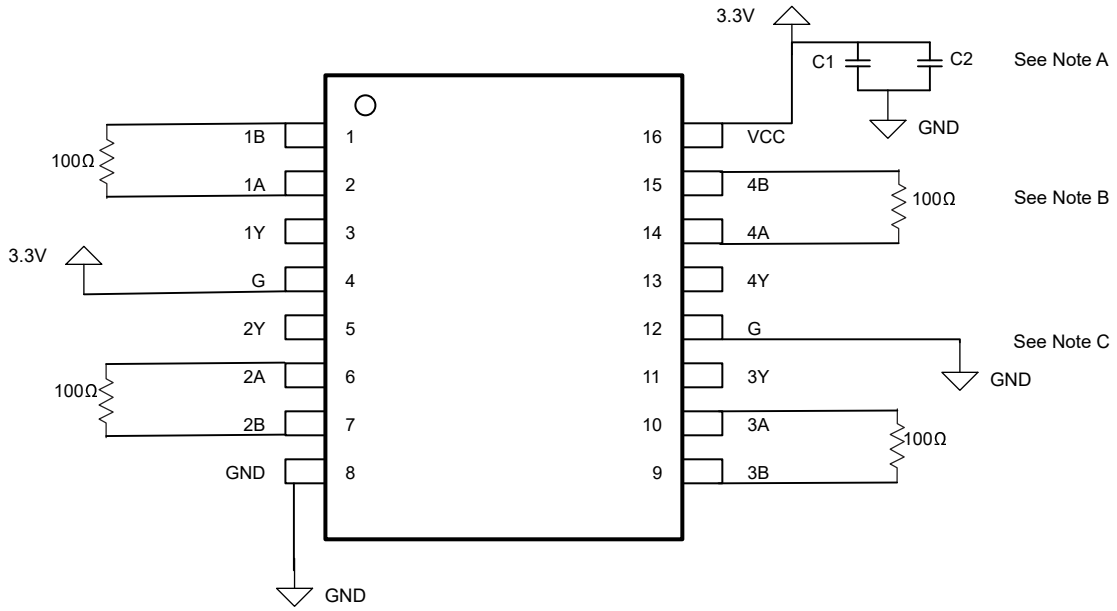
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

For general application guidelines and hints about LVDS drivers and receivers, refer to the *LVDS application notes and design guides*.

8.2 Typical Application



A. The capacitors should be located as close as possible to the device terminals. See Supply Bypass Capacitance for capacitor values.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 8-1. Operation With 3.3V Supply

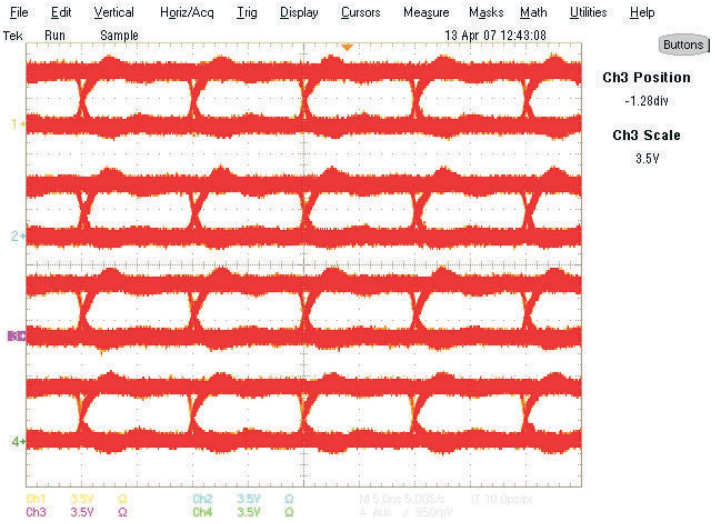
8.2.1 Detailed Design Procedure

The physical communication channel between the driver and the receiver can be any balanced paired metal conductors meeting the requirements of the LVDS standard. This media can be a twisted pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect shall be between typical 100Ω with a variation of no more than 10% (90Ω to 110Ω).

8.2.2 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6V
Driver Input Voltage	0.8 to 3.3V
Driver Signaling Rate	DC to 100Mbps
Interconnect Characteristic Impedance	100Ω
Termination Resistance	100Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6V
Receiver Input Voltage	0 to 24V
Receiver Signaling Rate	DC to 100Mbps
Ground shift between driver and receiver	±1V

8.2.3 Application Performance Plots



All Rx running at 100Mbps; Channel 1: 1Y Channel 2: 2Y Channel 3: 3Y Channel 4: 4Y T = 25°C V_{CC} = 3.6V PRBS = 2^{23} – 1

Figure 8-2. Typical Eye Patterns

8.2.4 Cold Sparing

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

8.3 Active Failsafe Feature

A differential line receiver commonly has a failsafe circuit to prevent the output from switching on input noise. Current LVDS failsafe implementation require either external components with subsequent reductions in signal quality or integrated solutions with limited application. This family of receivers has a new integrated failsafe that solves the limitations seen in present solutions. A detailed theory of operation is presented in the Active Fail-Safe in TI's LVDS Receivers application note.

Figure 8-3 shows one receiver channel with active failsafe, which consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two failsafe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and the comparator detects when the input differential falls below 80mV. A 600ns failsafe timer filters the window comparator outputs. When failsafe is asserted, the failsafe logic drives the main receiver output to logic high.

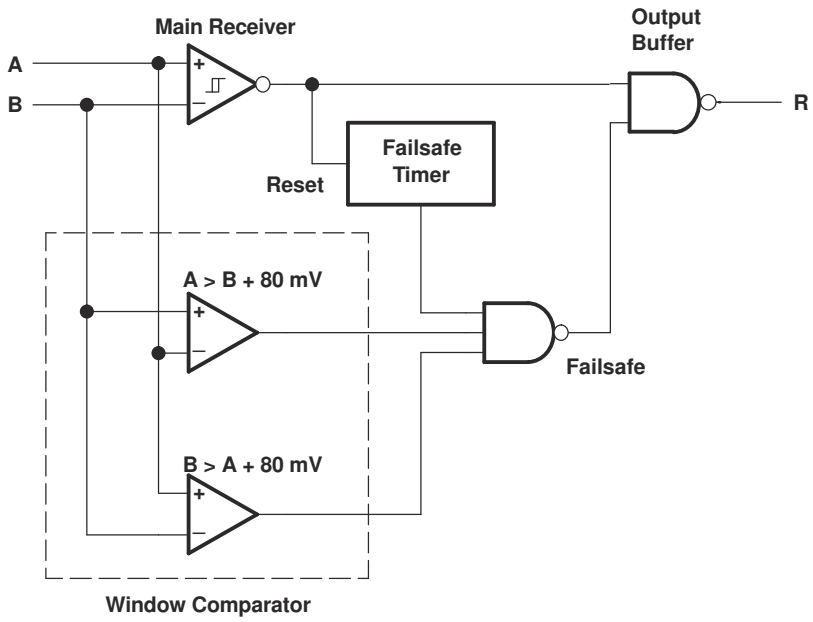


Figure 8-3. Receiver with active failsafe

8.4 ECL/PECL-to-LVTTL Conversion with TI's LVDS Receiver

The various versions of emitter-coupled logic (for example, ECL, PECL and LVPECL) are often the physical layer of choice for system designers. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS is not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. Texas Instruments has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination (V_{CC} – 2V).

Figure 8-4 and Figure 8-5 show the use of an LV/PECL driver driving five meters of CAT-5 cable and being received by Texas Instruments wide common-mode receiver and the resulting eye-pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of 50Ω. The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

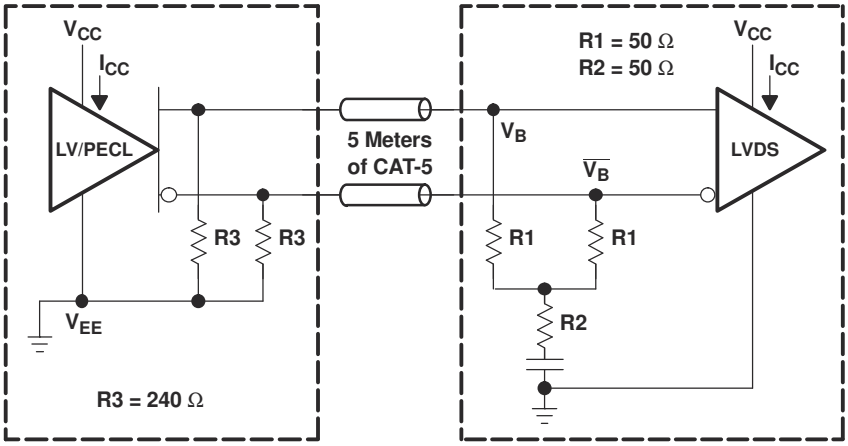


Figure 8-4. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

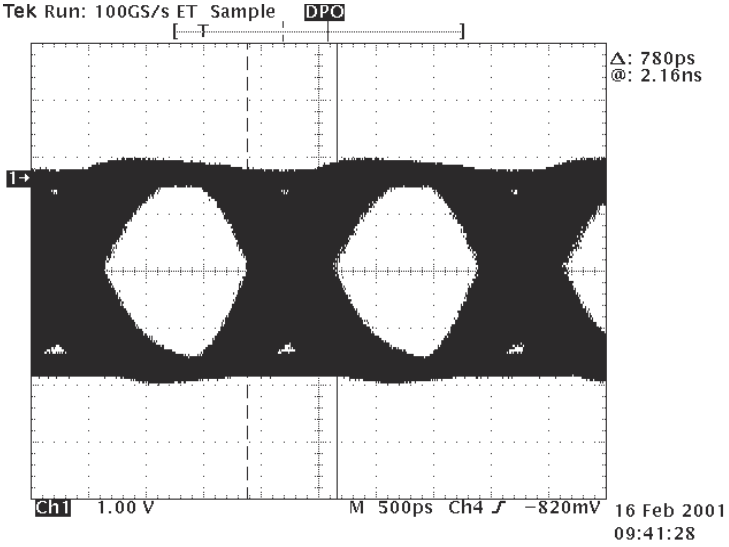


Figure 8-5. LV/PECL to Remote SN55LVRA4-SEP at 500Mbps Receiver Output (CH1)

8.5 Test Conditions

- V_{CC} = 3.3V
- T_A = 25°C (ambient temperature)
- All four channels switching simultaneously with NRZ data. The scope is pulse-triggered simultaneously with NRZ data.

8.6 Equipment

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

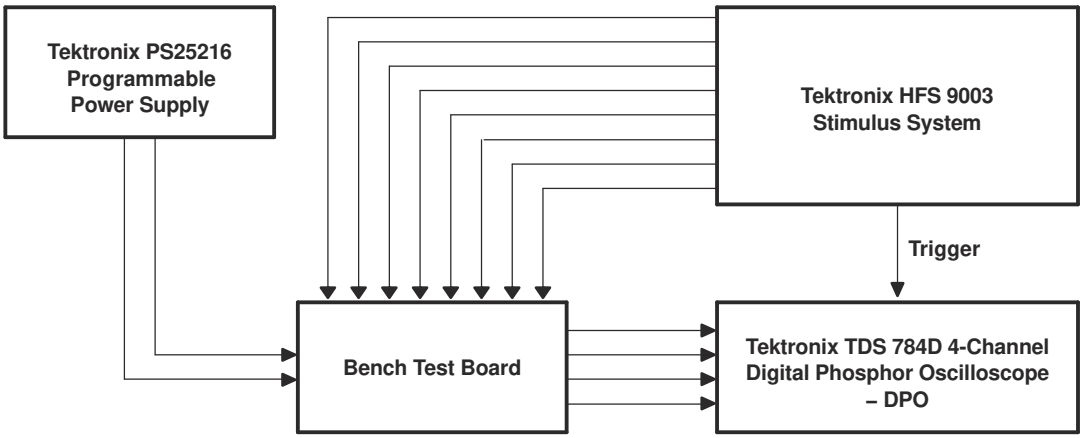


Figure 8-6. Equipment Setup

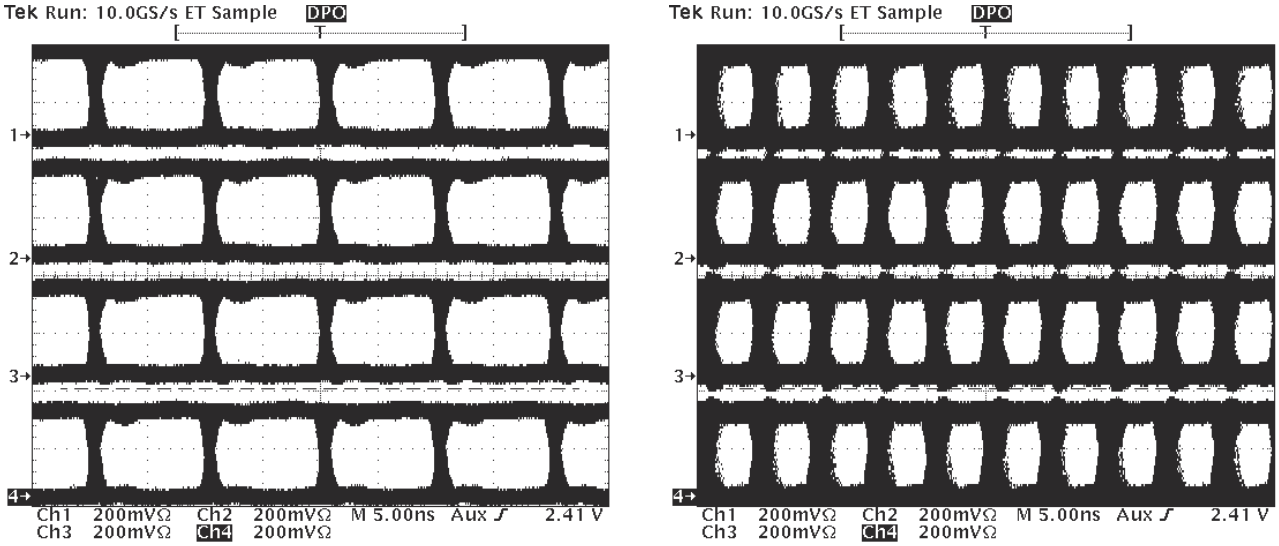


Figure 8-7. Typical Eye Pattern SN55LVRA4-SEP

9 Power Supply Recommendations

9.1 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, bypass capacitors create low-impedance paths between power and ground at particular frequency depending on the value. At low frequencies, a voltage regulator offers low-impedance paths between the terminal and ground. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10µF to 1000µF) at the board-level do a good job up into the kHz range. Due to the size and length of the leads, large capacitors tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one can resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0402 or 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because the lead inductance is about 1nH. In addition, the inductance from the PCB trace length connecting V_{CC} to capacitor also impact resonance and effectiveness of the capacitor.

Figure 8-1 shows C1 and C2 close to supply pin.

Recommended value for C1 is 10nF and C2 should be based on operating frequency of the application and capacitor distance from the supply pin. For example at 100MHz operating frequency, use 10nF for C1 and 1nF for C2 with both C1 and C2 within 3mm of the supply pin. The recommended capacitor value need to change for 6mm distance. Do not have long trace between C1 and C2 which could create a resonance circuit that can make power supply noise worse. In that case just have C1 will be better.

Multiple C2 capacitors can used if the primary operating frequency could change based on application of the system. For example, 10nF, 1nF and 0.47nF can be used if the system can operate at 100MHz or 150MHz primary frequencies.

Note

If power supply decoupling is not optimum the duty cycle distortion can occur when multiple channels are switching simultaneously.

Table 9-1. Recommended Capacitor Values

trace length (supply capacitor to VCC pin)	C2 Value	Resonance Frequency
3mm	4.7nF	50MHz
3mm	1nF	100MHz
3mm	0.47nF	150MHz
3mm	0.27nF	200MHz
6mm	2.2nF	50MHz
6mm	0.51nF	100MHz
6mm	0.22nF	150MHz
6mm	0.13nF	200MHz

10 Layout

10.1 Layout Guidelines

10.1.1 Microstrip vs. Stripline Topologies

As per the LVDS Application and Data Handbook, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 10-1.

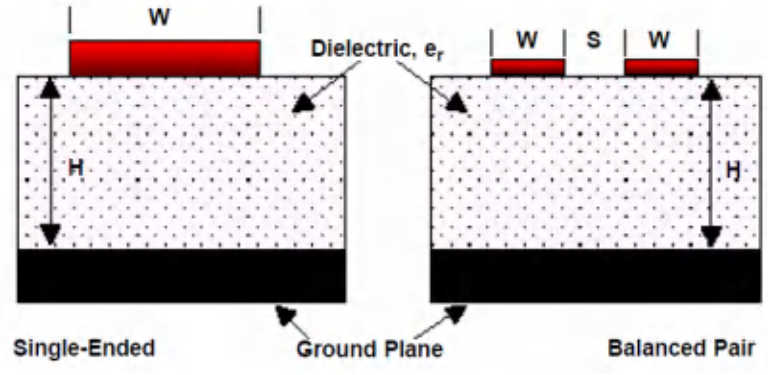


Figure 10-1. Microstrip Topology

Also, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances.

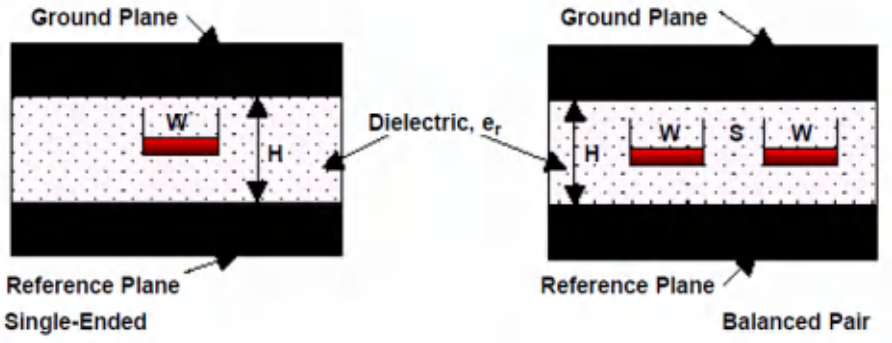


Figure 10-2. Stripline Topology

10.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15g or 1/2oz start, plated to 30g or 1oz
- All exposed circuitry should be solder-plated (60/40) to 7.62µm or 0.0003in (minimum).
- Copper plating should be 25.4µm or 0.001in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

10.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the user should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, a good practice is to have at least two separate signal planes as shown in Figure 10-3.

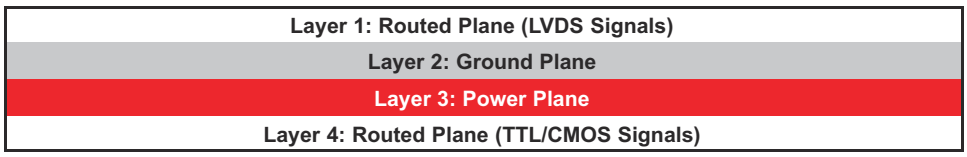


Figure 10-3. Four-Layer PCB Board

Note

The separation between layers 2 and 3 should be 127µm (0.005in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 10-4.

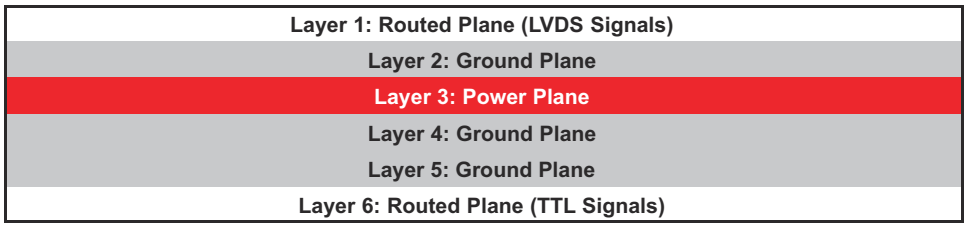


Figure 10-4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

10.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to make sure the pairs are balanced; thus, minimizing problems with skew and signal reflection.

For two adjacent single-ended traces, one should use the 3W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

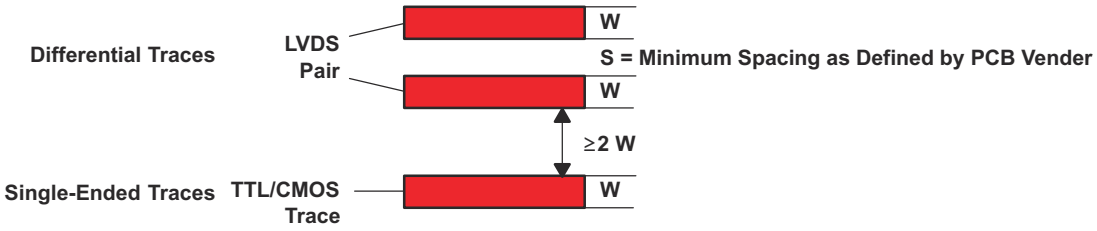


Figure 10-5. 3-W Rule for Single-Ended and Differential Traces (Top View)

The user should exercise caution when using auto-routers, because auto-routers do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

10.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

10.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 10-6.

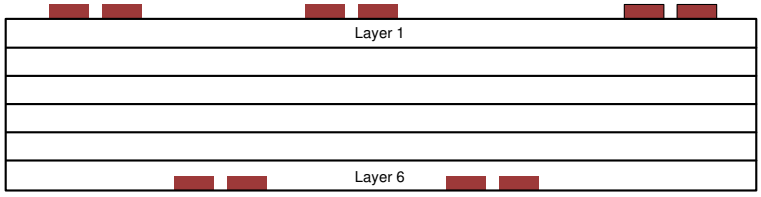


Figure 10-6. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 10-7. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2pF to 1pF in FR4.

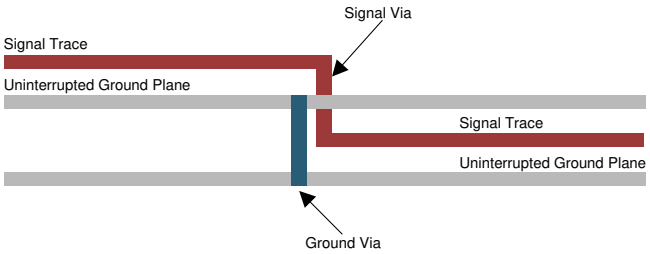


Figure 10-7. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

IBIS modeling is available for this device. Contact the local Texas Instruments sales office or the Texas Instruments Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- Texas Instruments, *Low-Voltage Differential Signalling Design Notes*
- Texas Instruments, *Interface Circuits for TIA/EIA-644* (LVDS)
- Texas Instruments, *Reducing EMI With LVDS*
- Texas Instruments, *Slew Rate Control of LVDS Circuits*
- Texas Instruments, *Using an LVDS Receiver With RS-422 Data*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

Changes from Revision * (February 2025) to Revision A (December 2025) **Page**

- Added "radiation tolerant" to data sheet title.... 1
- Added VID number.... 1
- Added SET characterization report availability and updated SEL to 50MeV.... 1
- Updated data sheet status from *Advanced Information* to *Production Data* 1
- Changed the D (SOIC) Package Size in the *Package Information* table.... 1
- Added bus pin ESD rating.... 4
- Changed HBM ESD from 2kV to 4kV.... 4
- Changed CDM ESD from 750V to 1000V.... 4
- Changed ROC V_{IH} max for enable to V_{CC} 4
- Changed V_{IT1} and $V_{IT2}$from 50mV to 90mV 6
- Changed TPHL max from 8ns to 8.5ns.... 7
- Changed TLH min from 1.8ns to 1.3ns, max from 8ns to 7.5ns.... 7
- Changed td1 max from 11ns to 16ns.... 7
- Changed td2 max from 2µs to 2.5µs and removed min limit.... 7
- Changed tSK(p) typical from 200ns to 500ns.... 7
- Changed typical tsk(o) from 150ns to 130ns.... 7
- Changed max TPHZ from 12ns to 15ns.... 7
- Changed Application Diagram to 3.3V supply and add more details on C1 and C2 decoupling capacitors.... 16
- Added link to Bypass Capacitance recommendation section.... 16
- Added more information decoupling cap.... 21
- Added NOTE on impact on system performance.... 21

DATE	REVISION	NOTES
February 2025	*	Initial Release

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PSN55LVRA4MDTSEP	Active	Preproduction	SOIC (D) | 16	250 | SMALL T&R	-	Call TI	Call TI	-55 to 125	
SN55LVRA4MDTSEP	Active	Production	SOIC (D) | 16	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-55 to 125	LVRA4SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

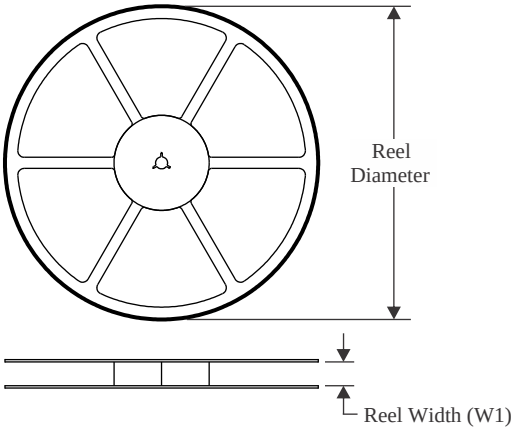
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

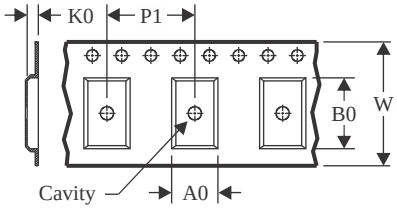
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

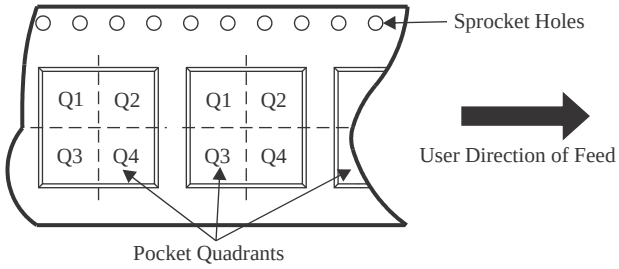


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

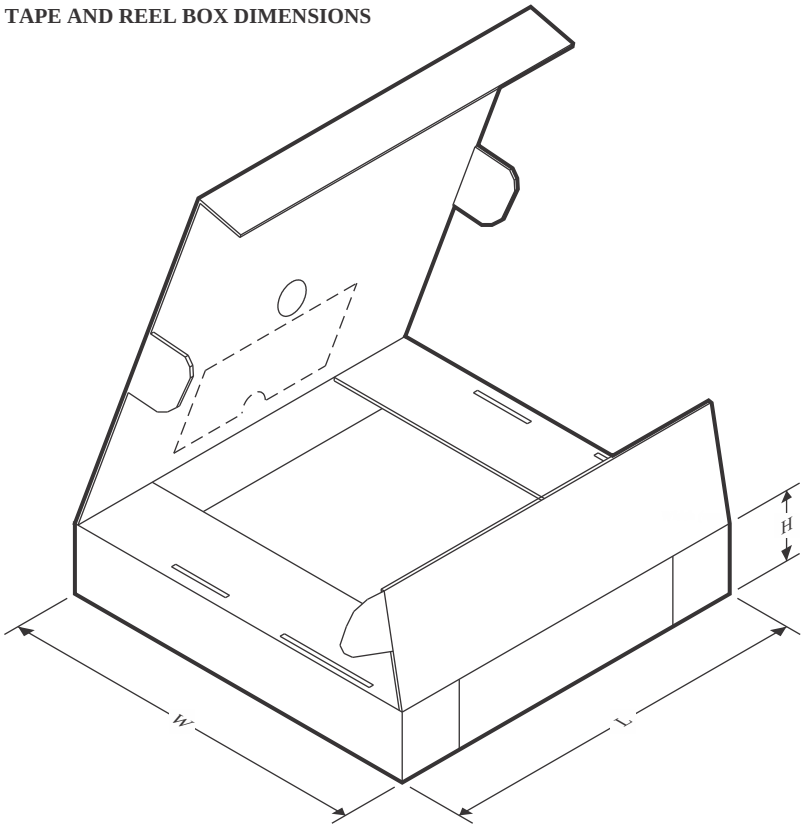
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN55LVRA4MDTSEP	SOIC	D	16	250	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

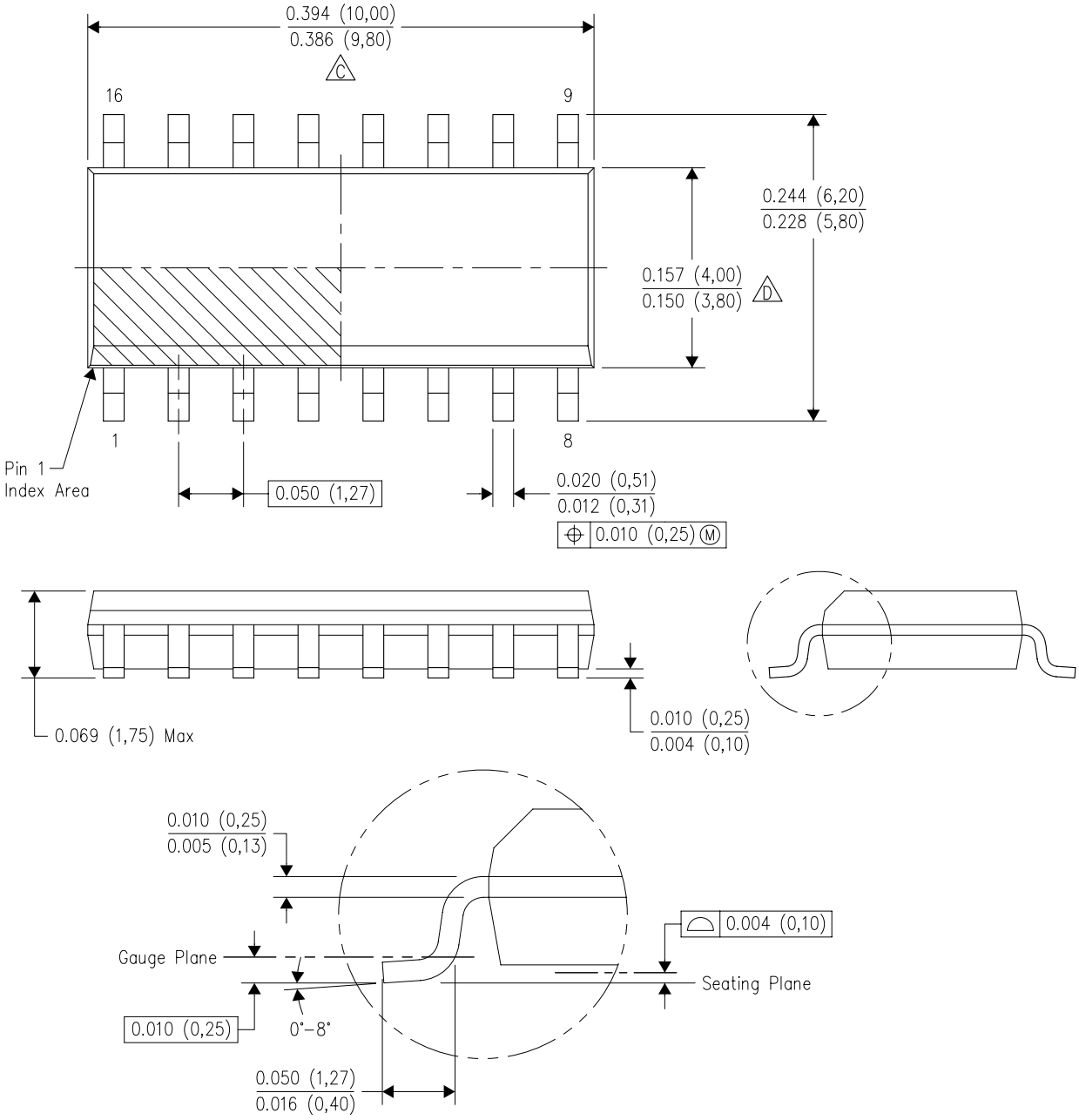
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN55LVRA4MDTSEP	SOIC	D	16	250	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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Last updated 10/2025