SN65HVD62 AISG On-Off Keying Coax Modem Transceiver

1 Features

- Supply Ranging From 3V to 5.5V
- Independent Logic Supply of 1.6V to 5.5V
- Wide Input Dynamic Range of –15dBm to +5dBm for Receiver
- Power Delivered by the Driver to the Coax can be Adjusted From 0dBm to +6dBm
- AISG Compliant Output Emission Profile
- Low-power Standby Mode
- Direction Control Output for RS-485 Bus Arbitration
- Supports up to 115 kbps Signaling
- Integrated Active Bandpass Filter with Center Frequency at 2.176MHz
- 3mm × 3mm 16-Pin QFN Package

2 Applications

- AISG – Interface for Antenna Line Devices
- Tower Mounted Amplifiers (TMA)
- General Modem Interfaces

3 Description

These transceivers modulate and demodulate signals between the logic (baseband) and a frequency suitable for long coaxial media.

The HVD62 is an integrated AISG transceiver designed to be compliant with Antenna Interface Standards Group v2.0 specification.

The HVD62 receiver integrates an active bandpass filter to enable demodulation of signals even in the presence of spurious frequency components. The filter has a 2.176 MHz center frequency.

The transmitter supports adjustable output power levels varying from +0dBm to +6dBm delivered to the 50 Ω coax cable. The HVD62 transmitter is compliant with the spectrum emission requirement provided by the AISG standard.

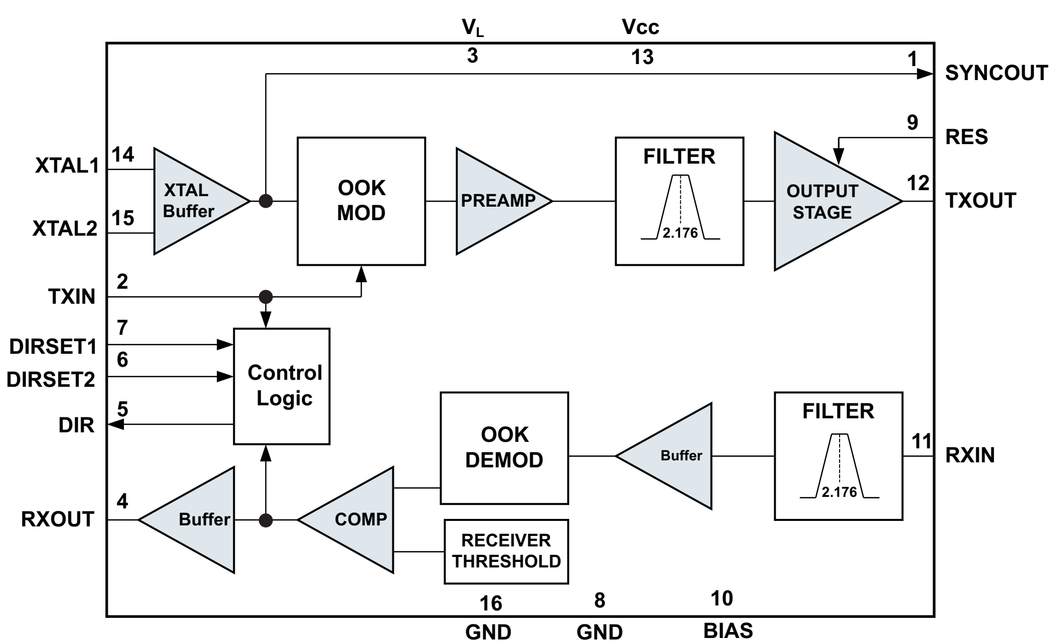
A direction control output is provided which facilitates bus arbitration for an RS-485 interface. These devices integrate an oscillator input for a crystal, and also accept standard clock inputs to the oscillator.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD62	VQFN (16)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Block Diagram



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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2013) to Revision C — Page

- Added *Device Information* table,*ESD Ratings* table, *Device Functional Modes*, *Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging*, and *Orderable Information* section. ... 1
- Moved the Storage temperature From: *Thermal Information* To: *Absolute Maximum Ratings*(1) ... 4
- Changed T_A in the *Recommended Operating Conditions* From: MAX = 85°C To: MAX = 105°C ... 5

Changes from Revision A (January 2012) to Revision B — Page

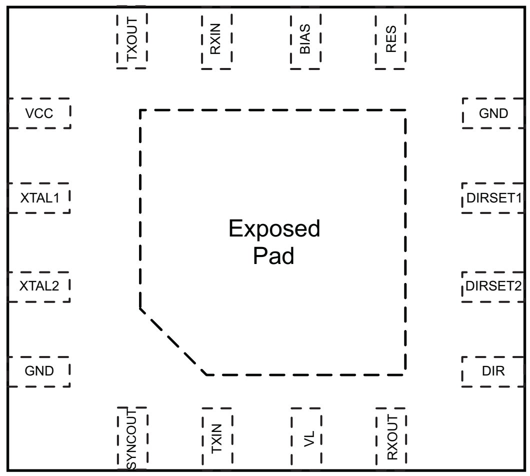
- Changed *Features* From: "Power Delivered by the Driver to the Coax can be Adjusted +3dBm to +6dBm" To: "Power Delivered by the Driver to the Coax can be Adjusted 0dBm to +6dBm" ... 1
- Added Storage temperature to the *Thermal Information* ... 4
- Change the MIN value of V_{RES} in the ROC table From: 0.84 To: 0.7 V ... 5
- Change the TYP value of C_C in the ROC table From: 270 To: 220 nF ... 5
- Changed the *Electrical Characteristics* ... 6
- Changed the *Switching Characteristics* ... 7
- Added the *Typical Characteristics* section ... 8
- Changed the *Parameter Measurement Information* section ... 11
- Changed the *Application Information* section ... 16

Changes from Original (September 2011) to Revision A — Page

- Changed Pin 4 label (lower right) in the *Pin Configuration and Functions* diagram from TXIN to RXOUT ... 3
- Changed the *Pin Functions* table by merging the DESCRIPTION cells for pins 5, 6, and 7 and deleted the word DIRSET from the beginning of the second line in that description field. ... 3
- Added rows 162 and 163 to the *Electrical Characteristics* table, under RECEIVER FILTER section ... 6
- Added rows 210 and 211 to the *Switching Characteristics* table ... 7
- Added Table 1 and Table 2 ... 15
- Added Figure 22 State Transition Diagram ... 15

6 Pin Configuration and Functions

RGT (VQFN) Package
16 Pins
Top View



Pin Functions

PIN	HVD62 PIN NAME	DESCRIPTION
1	SYNCOUT	Open drain output to synchronize other devices to the 4x-carrier oscillator at XTAL1,2. (8.704 MHz for HVD62)
2	TXIN	Digital data bit stream to driver.
3	VL	Logic supply voltage for the device.
4	RXOUT	Digital data bit stream from receiver.
5	DIR	DIR: Direction control output signal for bus arbitration. DIRSET1 and DIRSET2: Bits to set the duration of DIR DIRSET[2,1]:[L,L]=9.6kbps [L,H]=38.4kbps [H,L]=115kbps [H,H]=Standby Mode
6	DIRSET2	
7	DIRSET1	
8	GND	Ground
9	RES	Input voltage to adjust driver output power. Set by external resistors from BIAS pin to GND.
10	BIAS	Bias voltage output for setting driver output power by external resistors.
11	RXIN	Modulated input signal to the receiver.
12	TXOUT	Modulated output signal from the driver.
13	VCC	Analog supply voltage for the device.
14	XTAL1	Crystal oscillator's IO pins. Connect a 4 x f_C crystal between these pins. Or connect XTAL1 to an 8.704 MHz clock and connect XTAL2 to GND.
15	XTAL2	
16	GND	Ground
-	EP	Exposed pad. Recommended to be connected to ground plane for best thermal conduction.

7 Specifications

7.1 Absolute Maximum Ratings[1]

	VALUES		UNIT
	MIN	MAX	
Supply voltage, V_{CC} and V_L	–0.5	6	V
Voltage range at coax pins	–0.5	6	V
Voltage range at logic pins	–0.3	V_L + 0.3	V
Logic Output Current	–20	20	mA
TXOUT output current	Internally limited		
SYNCOUT output current	Internally limited		
Junction Temperature, T_J		170	°C
Storage temperature, T_{STG}	–65	150	
Continuous total power dissipation	See the *Thermal Information*		°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC[1]		SN65HVD62 RGT (VQFN) (16) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	64.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	22.9	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	25.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		3		5.5	V
V_L	Logic supply voltage		1.6		5.5	V
$V_{I(pp)}$	Input signal amplitude at RXIN				1.12	Vpp
V_{IH}	High-level input voltage	TXIN, DIRSET1, DIRSET2	70%V_L		V_L	V
		XTAL1, XTAL2	70%V_{CC}		V_{CC}	
V_{IL}	Low-level input voltage	TXIN, DIRSET1, DIRSET2	0		30%V_L	V
		XTAL1, XTAL2	0		30%V_{CC}	
$1/t_{UI}$	Data signaling rate		9.6		115	kbps
F_{OSC}	Oscillator frequency	HVD62	–30 ppm	8.704	30 ppm	MHz
T_A	Operating free-air temperature		–40		105	°C
T_J	Junction Temperature		–40		125	°C
R_{LOAD}	Load impedance between TXOUT to RXIN			50		Ω
	Load impedance between RXIN and GND at f_C (channel)			50		
R1	Bias resistor between BIAS and RES			4.1		kΩ
R2	Bias resistor between RES and GND			10		kΩ
R_{SYNC}	Pull-up resistor between SYNCOUT and V_{CC}			1		kΩ
V_{RES}	Voltage at RES pin		0.7		1.5	V
C_C	Coupling capacitance between RXIN and Coax (channel)			220		nF
C_{BIAS}	Capacitance between BIAS and GND			1		µF

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY								
100	I_{CC}	Supply current (V_{CC})	TXIN = L (Active)	DIRSET1 = L DIRSET2 = H		28	33	mA
101			TXIN = H (Quiescent)			25	31	
102			TXIN = 115 kbps, 50% duty cycle			27	33	
99			(Standby) DIRSET1 = DIRSET2=H			12	17	
103	I_L	Logic supply current	TXIN = H, RXIN = DC input				50	µA
104	ΔV_{RXIN}/ ΔV_{CC}	Receiver power supply rejection ratio	$V_{TXIN} = V_L$		45	60		dB
LOGIC PINS								
112	V_{OH}	High-level logic output voltage (RXOUT, DIR)	I_{OH} = –4 mA for V_L > 2.4V, I_{OH} = –2 mA for V_L < 2.4V		90%V_L			V
113	V_{OL}	Low-level logic output voltage (RXOUT, DIR)	I_{OL} = 4 mA for V_L > 2.4V, I_{OL} = 2 mA for V_L < 2.4V				10%V_L	V
114	I_{IH}/I_{IL}	Logic input current (DIRSET1/2)			-1		10	µA
	I_{IH}/I_{IL}	Logic input current (TXIN)			-2		1	µA
COAX DRIVER								
130	V_{OPP}	Peak-to-peak output voltage at device pin TXOUT (See Figure 19)	V_{RES} = 1.5 V (Maximum setting)		2.24	2.5		V_{PP}
132			V_{RES} = 0.7 V (Minimum setting)			1.17	1.3	
130A	V_{OPP}	Peak-to-peak voltage at coax out (See Figure 19)	V_{RES} = 1.5 V		5	6		dBm
132A			V_{RES} = 0.7 V			-0.6	0.3	
134	V_{OZ}	Off-state output voltage	At TXOUT				1	mVpp
134A			At coax out				-60	dBm
136		Output emissions	Coupled to coaxial cable with characteristic impedance 50 Ohms, as shown in Figure 1. With a recommended 470 pF capacitor between RXIN and GND. Measurements above 150 MHz are determined by setup.		Conforms to AISG spectrum emissions mask, 3GPP TS 25.461, see Figure 21			
41	fo	Output frequency (HVD62)				2.176		MHz
142	Δf	Output frequency variation			–100		100	ppm
143	Zo	Output impedance	At 100 kHz			0.03		Ω
144			At 10 MHz			3.5		Ω
145	$\| I_{OS} \|$	Short-circuit output current	TXOUT is also protected by a thermal shutdown circuit during short-circuit faults			300	450	mA
COAX RECEIVER								
152	V_{IT}	Input threshold	f_{IN} = 2.176 MHz		79	112	158	mVPP
152A					–18	–15	–12	dBm
154	Z_{IN}	Input impedance	f = f_O		11	21		kΩ
RECEIVER FILTER								
160	f_{PB}	Passband	VRXIN = 1.12VP_P		1.1		4.17	MHz
161	f_{REJ}	Receiver rejection range	2.176MHz carrier amplitude of 112.4 mV_{PP}, Frequency band of spurious components with 800 mVPP allowed.		1.1		4.17	MHz
162	$t_{noise\ filter}$	Receiver noise filter time (slow bit rate)	DIRSET for 9.6kbps			4		µs
163		Receiver noise filter time (fast bit rate)	DIRSET for > 9.6 kbps			2		
XTAL AND SYNC								
171	I_I	Input leakage current	XTAL1, XTAL2, 0V < V_{IN} < V_{CC}		–15		15	µA
172	V_{OL}	Output low voltage	SYNCOUT, with 1 kΩ resistor from SYNCOUT to V_{CC}				0.4	V

7.6 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

		PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
201	t_{pAQ}, t_{pQA}	Coax driver propagation delay	See Figure 19			5	µs
202	t_r, t_f	Coax receiver output rise/fall time	C_L = 15 pF, R_L = 1 kΩ, See Figure 19			20	ns
203	t_{PHL}, t_{PLH}	Receiver propagation delay	See Figure 20		5.5	11	µs
204	Duty Cycle	Coax receiver output duty cycle	$V_{RXIN(ON)}$ = 630 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
214			$V_{RXIN(ON)}$ = 200 mVpp, $V_{RXIN(OFF)}$ < 5 mVpp, 50% duty cycle	40%		60%	
206	t_{DIR}	Direction control active duration	DIRSET2 = DIRSET1 = GND or OPEN		1667		µs
207			DIRSET2 = GND, DIRSET1 = VL		417		
208			DIRSET2 = VL, DIRSET1 = VL		137		
209	$t_{DIR\ Skew}$	Direction control skew (DIR to RXOUT)		270			ns
210	t_{DIS}	Standby disable delay	300 mV_{PP} at 2.176 MHz on RXIN		2		ms
211	t_{EN}	Standby enable delay			2		

7.7 Typical Characteristics

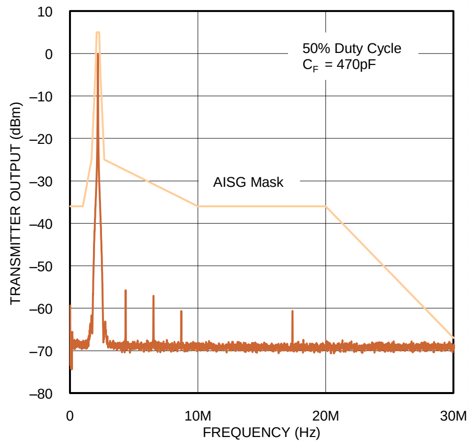


Figure 1. Low Frequency Emissions Spectrum with 9.6 kbps Signaling Rate

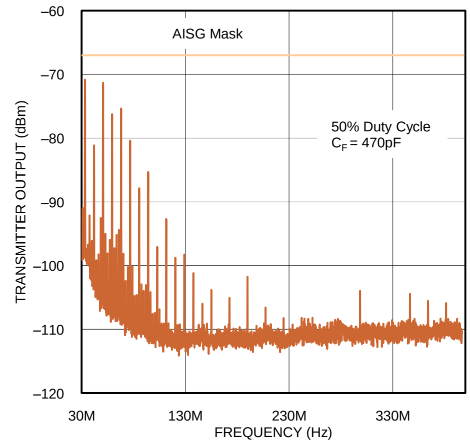


Figure 2. High Frequency Emissions Spectrum with 9.6 kbps Signaling Rate

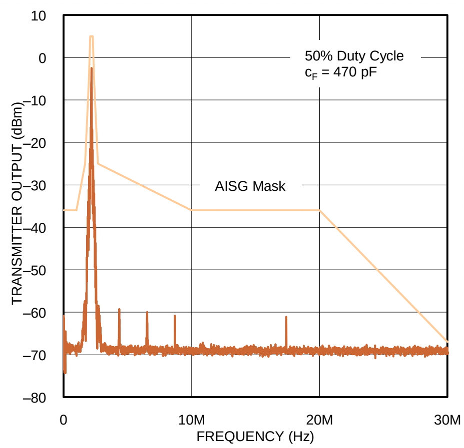


Figure 3. Low Frequency Emissions Spectrum with 38.4 kbps Signaling Rate

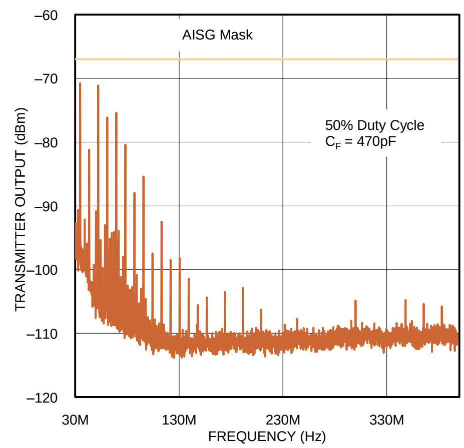


Figure 4. High Frequency Emissions Spectrum with 38.4 kbps Signaling Rate

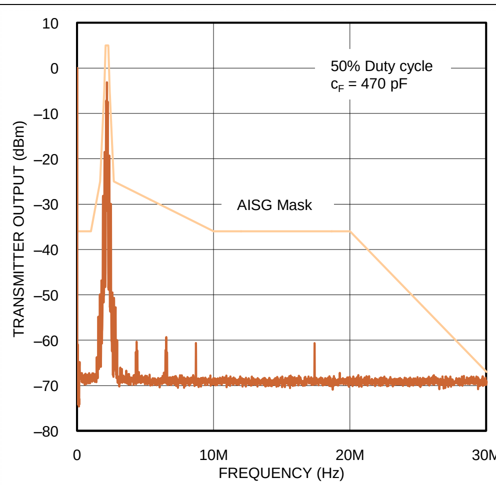


Figure 5. Low Frequency Emissions Spectrum with 115.2 kbps Signaling Rate

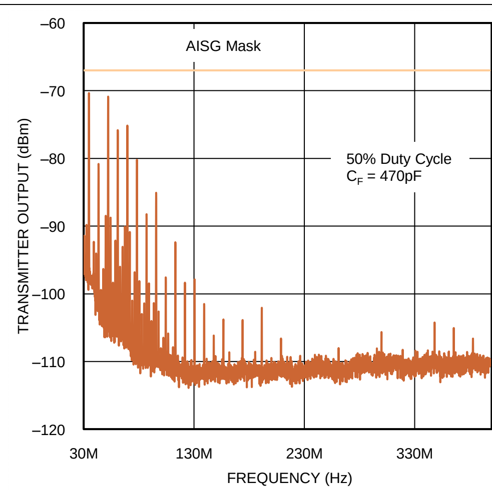


Figure 6. High Frequency Emissions Spectrum with 115.2 kbps Signaling Rate

Typical Characteristics (continued)

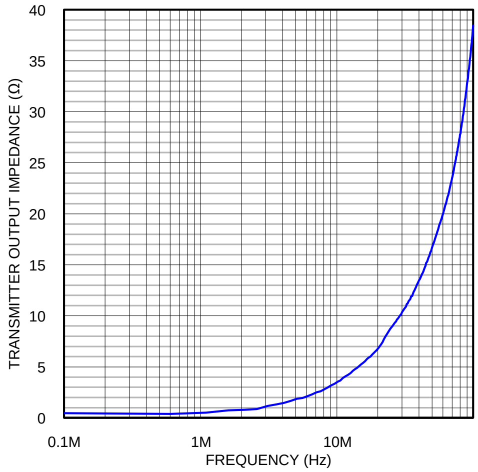


Figure 7. Transmitter Output Impedance

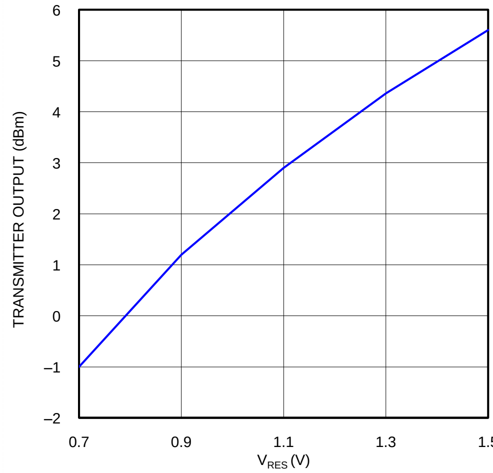


Figure 8. Transmit Power Adjustment

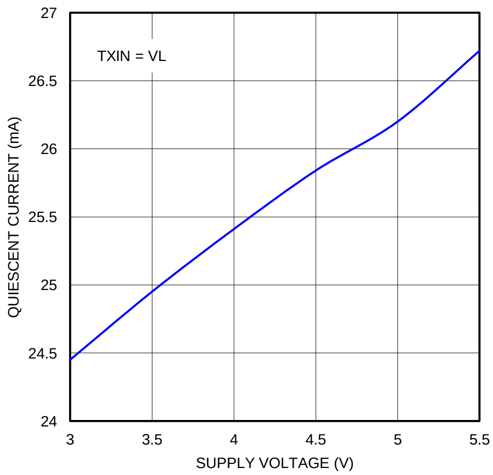


Figure 9. Supply Current versus Supply Voltage while Transmitting

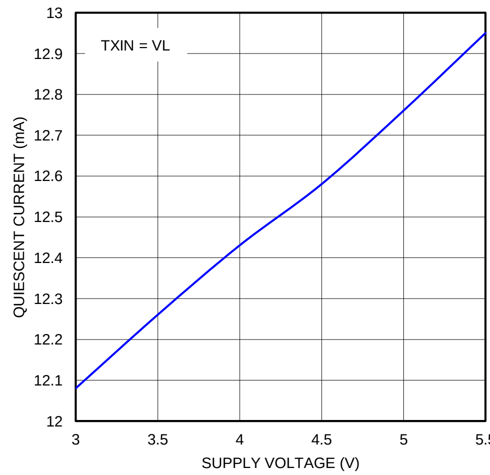


Figure 10. Supply Current versus Supply Voltage in Standby Mode

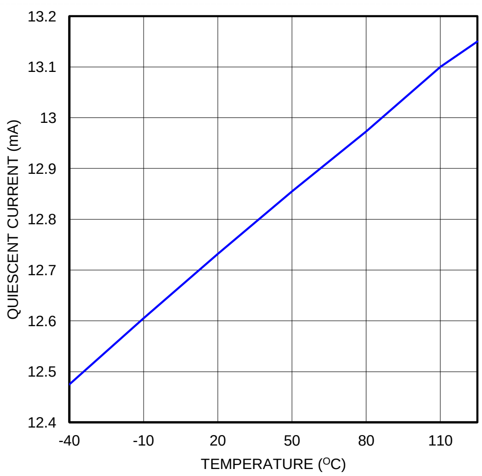


Figure 11. Supply Current versus Temperature in Standby Mode

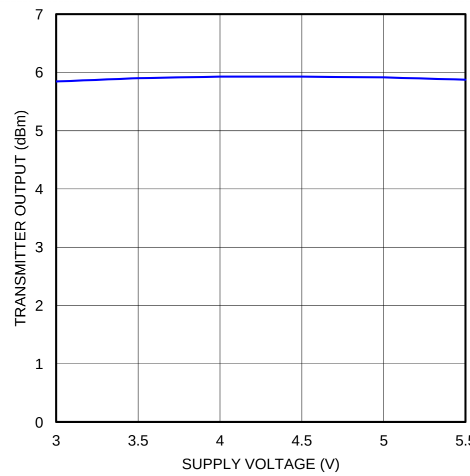


Figure 12. Transmitter Output Power versus Supply Voltage

Typical Characteristics (continued)

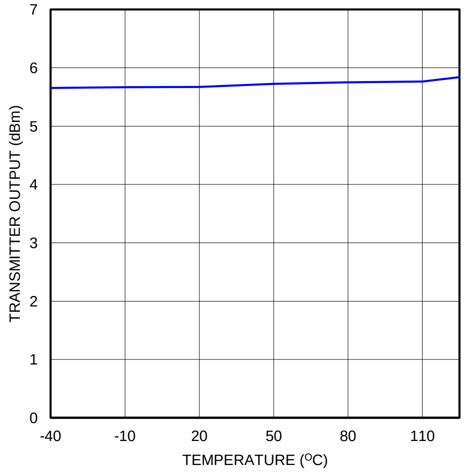


Figure 13. Transmitter Output Power versus Temperature

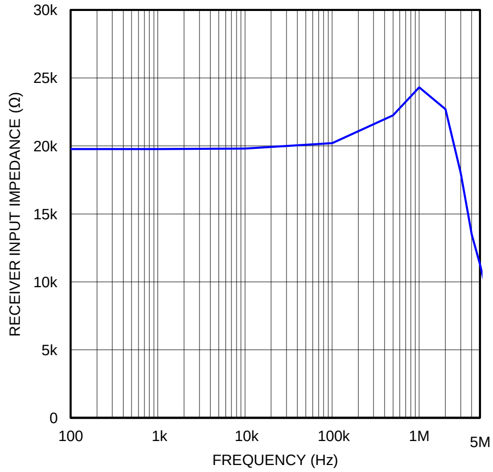


Figure 14. Receiver Input Impedance versus Frequency

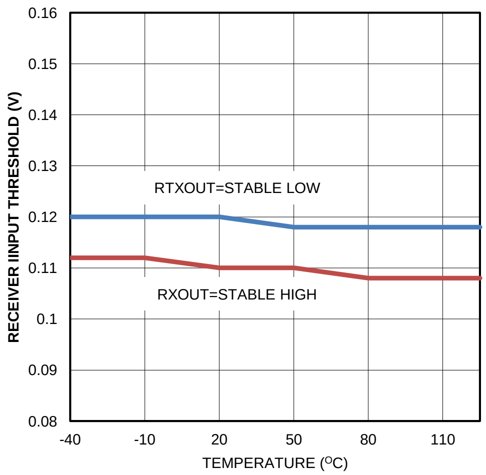


Figure 15. Receiver Input Threshold versus Temperature

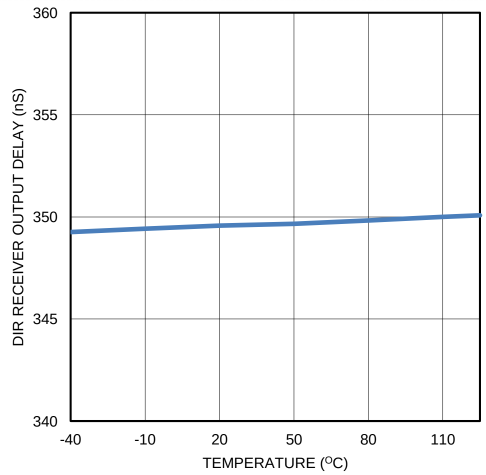


Figure 16. DIR Output Delay versus Temperature

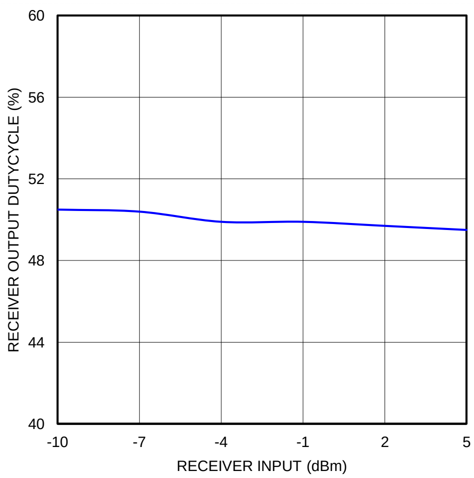


Figure 17. Receiver Duty Cycle with 9.6 kbps Signaling Rate

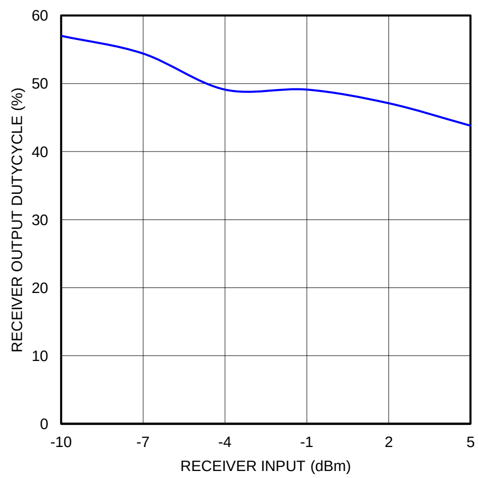


Figure 18. Receiver Duty Cycle with 115.2 kbps Signaling Rate

8 Parameter Measurement Information

Signal generator rate is 115 kbps, 50% duty cycle, rise and fall times less than 6 nsec, nominal output levels 0V and 3V. Coupling capacitor Cc is 220 nF.

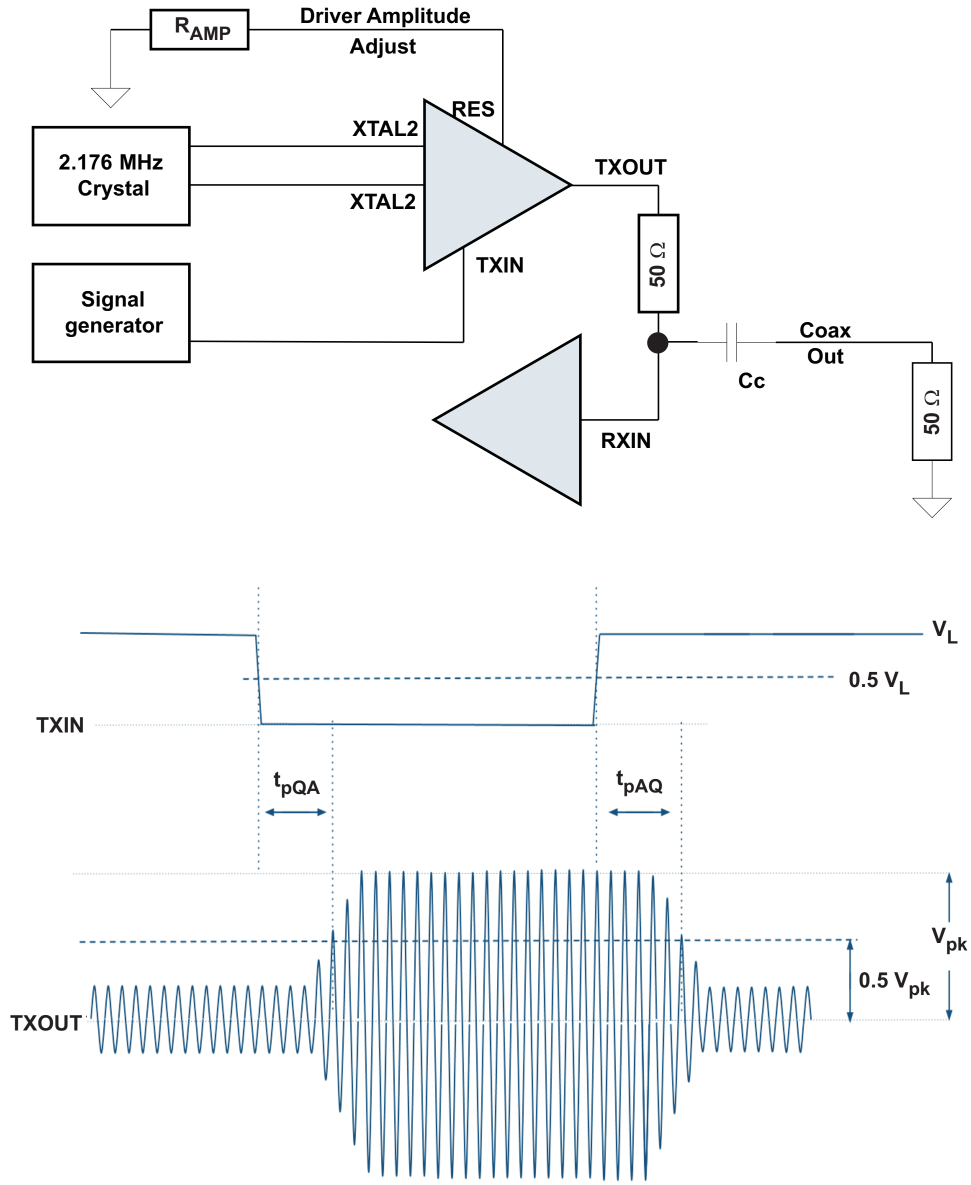


Figure 19. Measurement of Modem Driver Output Voltage With 50 Ω Loads

Parameter Measurement Information (continued)

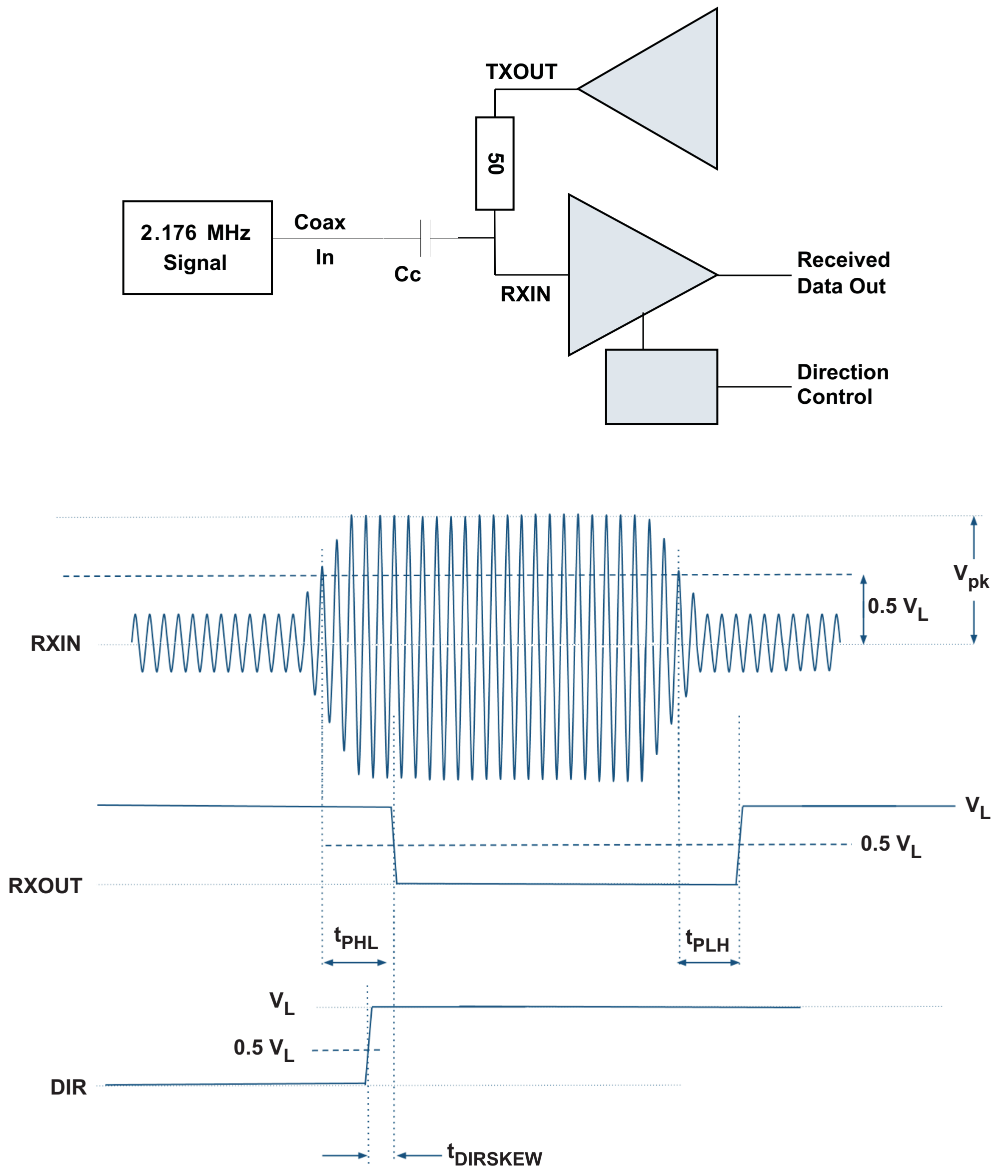


Figure 20. Measurement of Modem Receiver Propagation Delays

Parameter Measurement Information (continued)

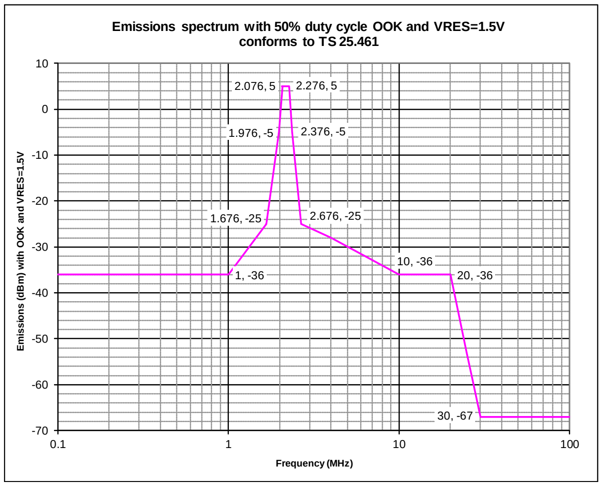


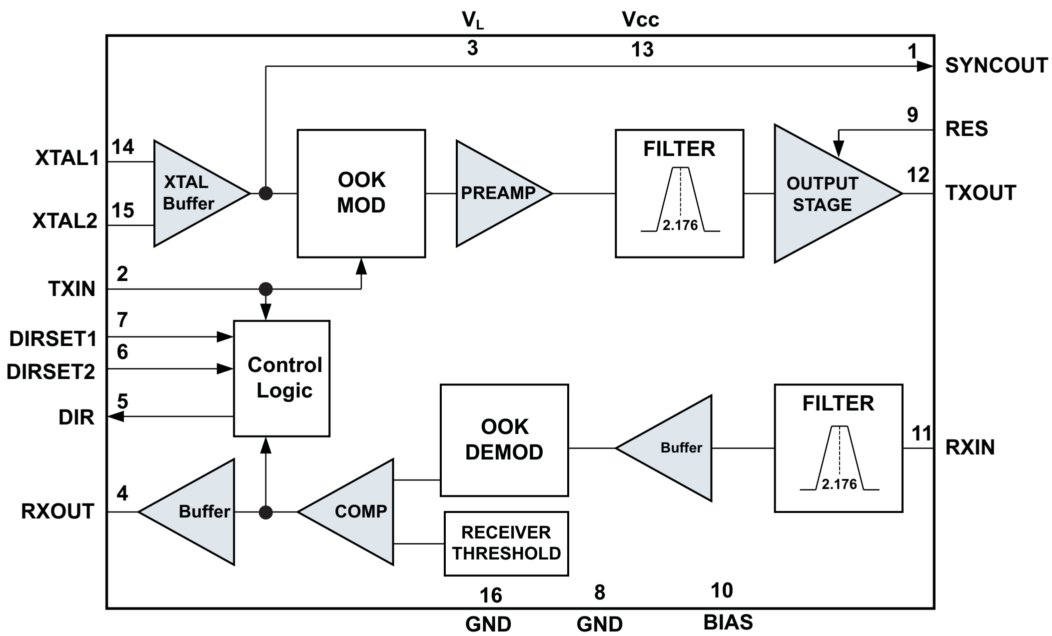
Figure 21. AISG Emissions Template

9 Detailed Description

9.1 Overview

If DIRSET1 and DIRSET2 are in a logic High state, the device will be in STANDBY mode. While in STANDBY mode, the Receiver functions normally, detecting carrier frequency activity on the RXIN pin and setting the RXOUT state as discussed below. But the Transmitter circuits are not active in STANDBY, thus the TXOUT pin is idle regardless of the logic state of TXIN. The supply current in STANDBY mode is significantly reduced, allowing power savings when the node is not transmitting.

9.2 Functional Block Diagram



9.3 Device Functional Modes

When not in STANDBY mode, the default power-on state is IDLE. When in IDLE mode, RXOUT is High, and TXOUT is quiet. The device transitions to RECEIVE mode when a valid modulated signal is detected on the RXIN line <OR> the device transitions to TRANSMIT mode when TXIN goes Low. The device stays in either RECEIVE or TRANSMIT mode until DIR Timeout (nominal 16 bit times) after the last activity on RXOUT or TXIN.

When in RECEIVE mode:

- RXOUT responds to all valid modulated signals on RXIN, whether from the local transmitter, a remote transmitter, or long noise burst.
- TXOUT responds to TXIN, generating 2.176 MHz signals on TXOUT when TXIN is Low, and TXOUT is quiet when TXIN is High. (In normal operation, TXIN is expected to remain High when the device is in RECEIVE mode).
- The device stays in RECEIVE mode until 16 bit times after the last rising edge on RXOUT, caused by valid modulated signal on the RXIN line.

When in TRANSMIT mode:

- RXOUT stays High, regardless of the input signal on RXIN.
- TXOUT responds to TXIN, generating 2.176 MHz signals on TXOUT when TXIN is Low, and TXOUT is quiet when TXIN is High.
- The device stays in TRANSMIT mode until 16 bit times after TXIN goes High.

Device Functional Modes (continued)

Table 1. Driver Function Table(1)

TXIN	[DIRSET1, DIRSET2]	TXOUT	COMMENT
H	[L,L], [L,H] or [H,L]	< 1 mV_{PP} at 2.176 MHz	Driver not active
L		V_{OPP} at 2.176 MHz	Driver active
X	[H,H]	< 1 mV_{PP} at 2.176 MHz	Standby mode

(1) H = High, L = Low, X = Indeterminate

Table 2. Receiver and DIR Function Table(1)

RXIN	RXOUT	DIR	COMMENT (see Figure 22)
IDLE mode (not transmitting or receiving)			
< V_{IT} at 2.176 MHz for longer than DIR timeout	H	L	No outgoing or incoming signal
RECEIVE mode (not already transmitting)			
< V_{IT} at 2.176 MHz for less than $t_{DIR\ Timeout}$	H	H	Incoming '1' bit, DIR stays HIGH for DIR Timeout
> V_{IT} at 2.176 MHz for longer than $t_{noise\ filter}$	L	H	Incoming '0' bit, DIR output is HIGH
TRANSMIT mode (not already receiving)			
X	H	L	Outgoing message, DIR stays LOW for DIR Timeout

(1) H = High, L = Low

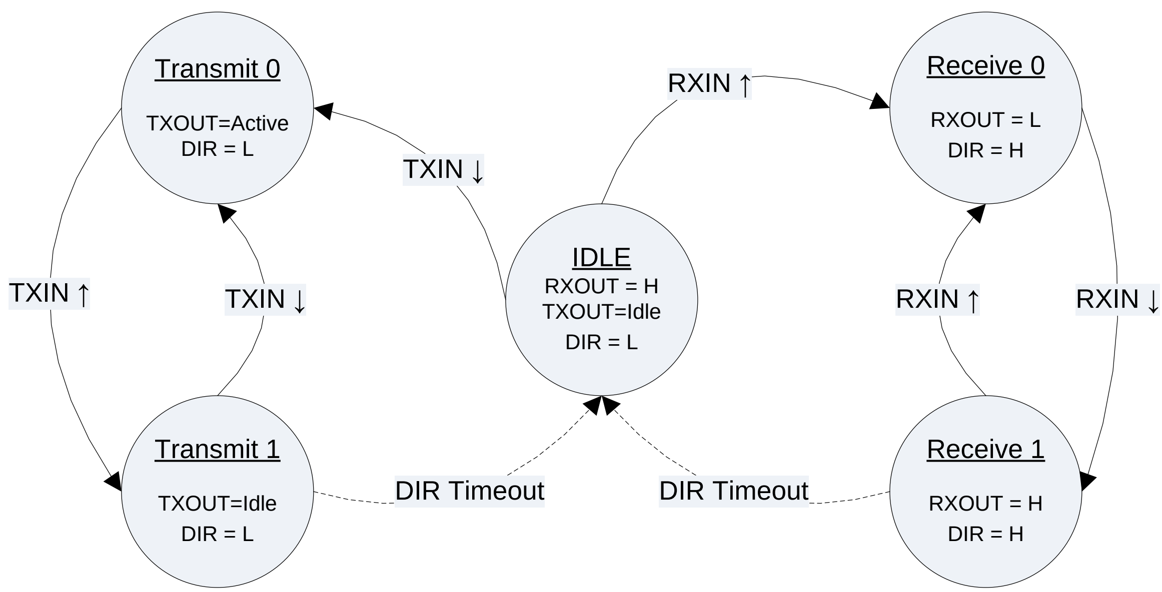


Figure 22. State Transition Diagram

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Driver Amplitude Adjust

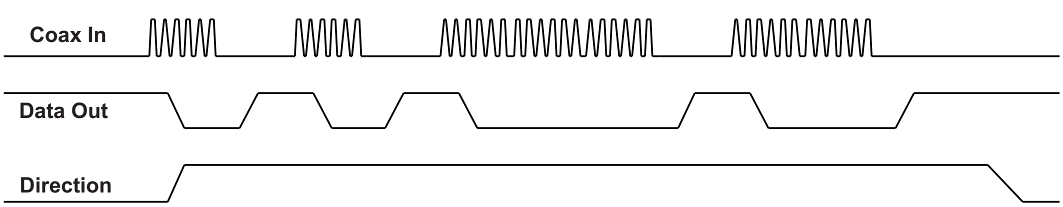
The SN65HVD62 can provide up to 2.5 V peak-to-peak of output signal at the TXOUT pin to compensate for potential loss within the external filter, cable, connections, and termination. External resistors are used to set the amplitude of the modulated driver output signal. Resistors connected across RES and BIAS set the output amplitude. The maximum peak-to-peak voltage at TXOUT is 2.5 V, corresponding to +6 dBm on the coaxial cable. The TXOUT voltage level can be adjusted by choice of resistors to set the voltage at the RES pin. according to the following equation:

$$VTXOUT\ (V_{P\text{-}P}) = (2.5\ V_{P\text{-}P} \times V_{RES}\ (V))/1.5\ V \quad V_{RES}\ (V) = 1.5\ V \times R2/(R1 + R2) \quad V_{TXOUT}\ (V_{P\text{-}P}) = 2.5\ V_{P\text{-}P} \times R2/(R1 + R2). \quad (1)$$

The voltage at the RES pin should be between 0.7 V and 1.5 V. Connect RES directly to the BIAS (R1 = 0 Ω) for maximum output level of 2.5 V peak-to-peak. This gives a minimum voltage level at TXOUT of 1.2 V peak-to-peak, corresponding to about 0 dBm at the coaxial cable. A 1 µF capacitor should be connected between the BIAS pin and GND. To obtain a nominal power level of +3 dBm at the feeder cable as the AISG standard requires, use R1 = 4.1k Ω and R2 = 10k Ω that provide 1.78 $V_{P\text{-}P}$ at TXOUT.

10.1.2 Direction Control

In many applications the mast-top modem which receives data from the base will then distribute the received data through an RS-485 network to several mast-top devices. When the mast-top modem receives the first logic 0 bit (active modulated signal) it will take control of the mast-top RS-485 network by asserting the Direction Control signal. The duration of the Direction Control assertion should be optimized to pass a complete message of length B bits at the known signaling rate ($1/t_{BIT}$) before relinquishing control of the mast-top RS-485 network. For example, if the messages are 10 bits in length (B=10) and the signaling rate is 9600 bits per second (t_{BIT} = 0.104 msec) then a positive pulse of duration 1.7 msec is sufficient (with margin to allow for network propagation delays) to enable the mast-top RS-485 drivers to distribute each received message.



10.1.3 Direction Control Time Constant

The time constant for the Direction Control function can be set by the Control Mode pins, DIRSET1/DIRSET2. These pins should be set to correspond to the desired data rate. With no external connections to the Control Mode pins, the internal time constant is set to the maximum value, corresponding to the minimum data rate.

Application Information (continued)

10.1.4 Conversion Between dBm and Peak-to-peak Voltage

$$\text{dBm} = 20 \times \text{LOG10}\,[\text{Volts-pp} / \text{SQRT}(0.008 \times Z_o)] = 20 \times \text{LOG10}\,[\text{Volts-pp} / 0.63] \text{ for } Z_o = 50\ \Omega \quad (2)$$

$$\text{Volts-pp} = \text{SQRT}(0.008 \times Z_o) \times 10^{(\text{dBm}/20)} = 0.63 \times 10^{(\text{dBm}/20)} \text{ for } Z_o = 50\ \Omega \quad (3)$$

The following table shows conversions between dBm and peak-to-peak voltage with 50 Ω load, for various levels of interest including reference levels from the 3GPP TS 25.461 Technical Specification.

SIGNAL ON COAX (Iuant Layer 1)	dBm	Vpp (V)
Maximum Driver ON Signal	5	1.12
Nominal Driver ON Signal	3	0.89
Minimum Driver ON Signal	1	0.71
AISG Maximum Receiver Threshold	–12	0.16
Nominal Receiver Threshold	–15	0.11
Minimum Receiver Threshold	–18	0.08
Maximum Driver OFF Signal	–40	0.006

11 Device and Documentation Support

11.1 Documentation Support

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD62RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62
SN65HVD62RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62
SN65HVD62RGTRG4	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62
SN65HVD62RGTRG4.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62
SN65HVD62RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62
SN65HVD62RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	HVD62

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

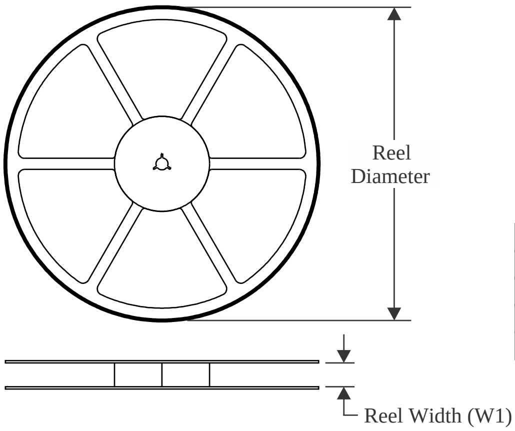
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

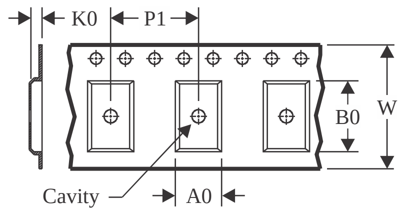
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

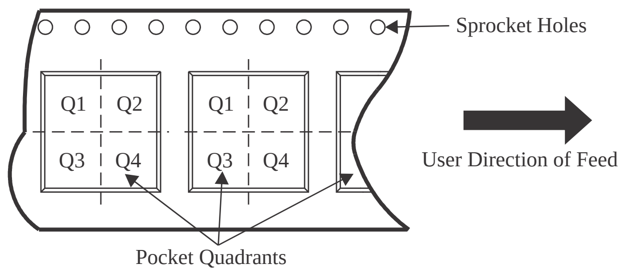


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

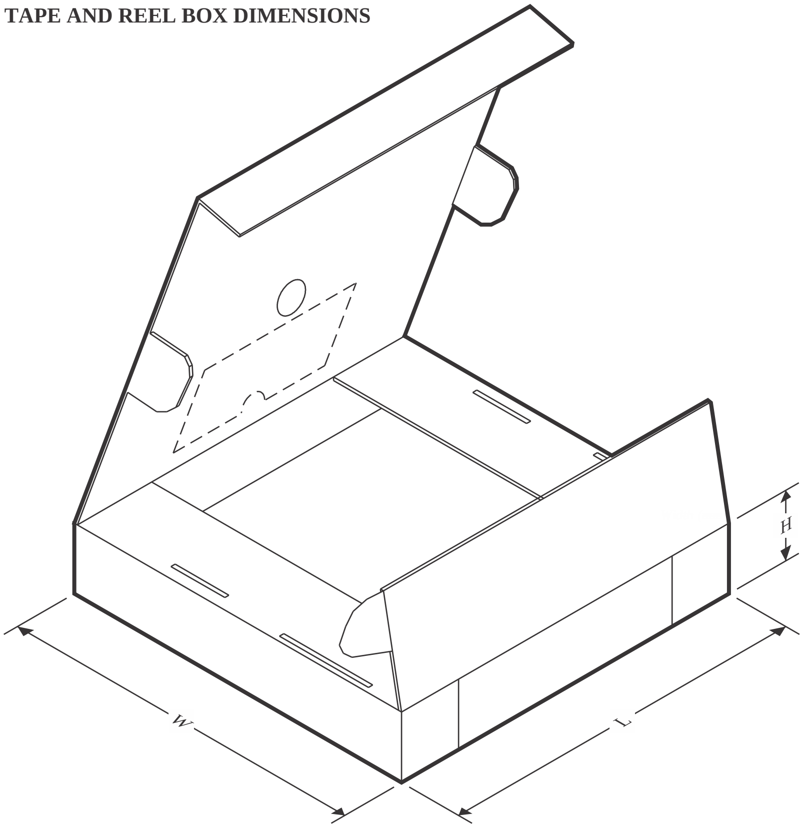
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD62RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD62RGTRG4	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD62RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



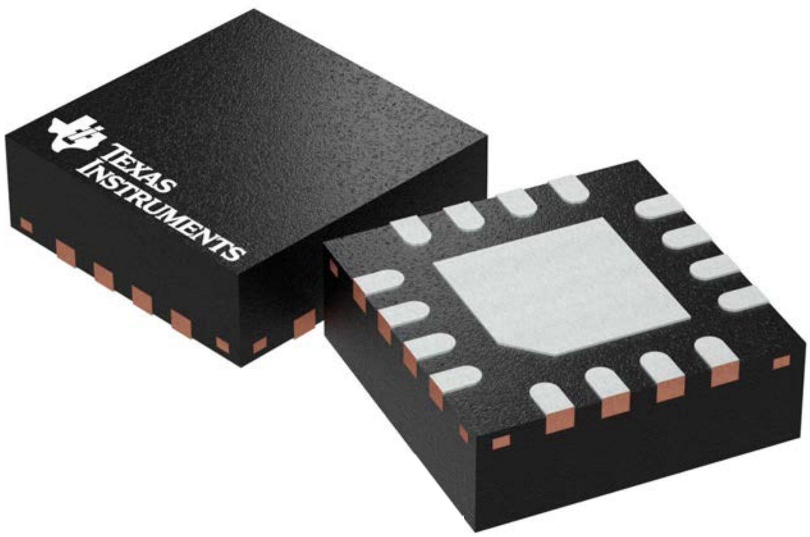
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD62RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
SN65HVD62RGTRG4	VQFN	RGT	16	3000	346.0	346.0	33.0
SN65HVD62RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

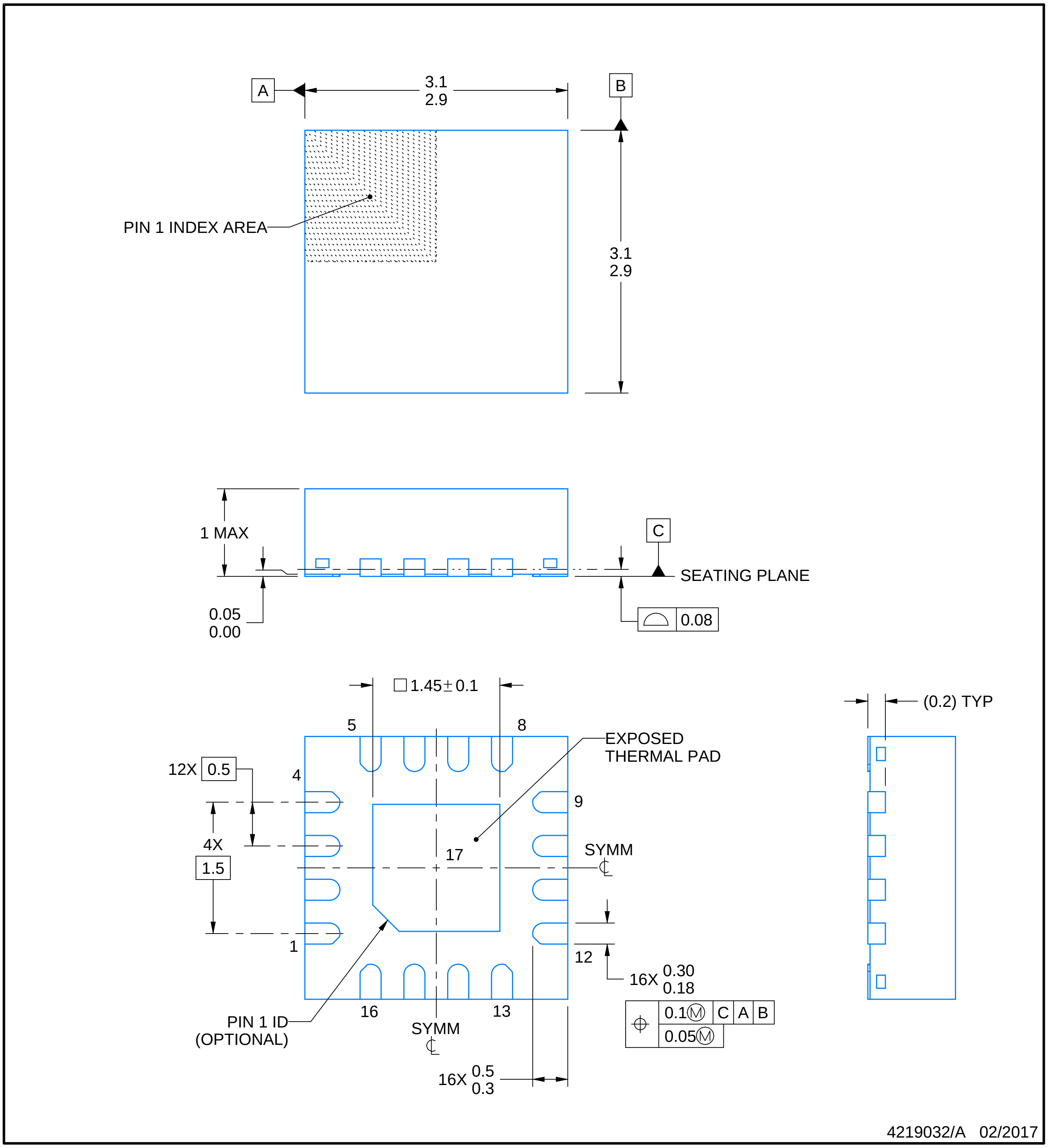
GENERIC PACKAGE VIEW

RGT 16 **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

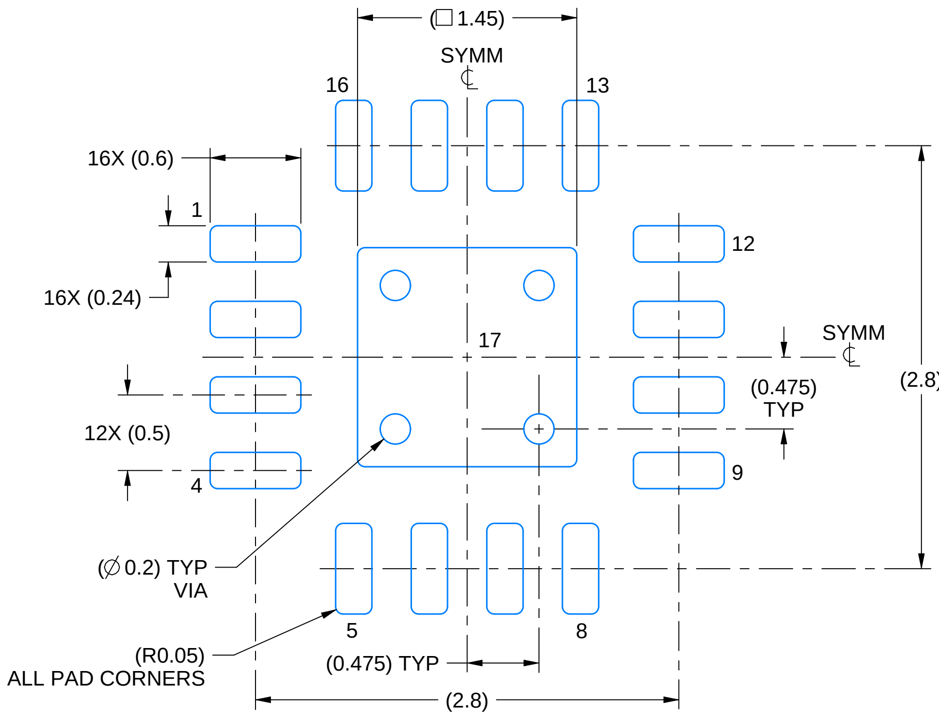


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

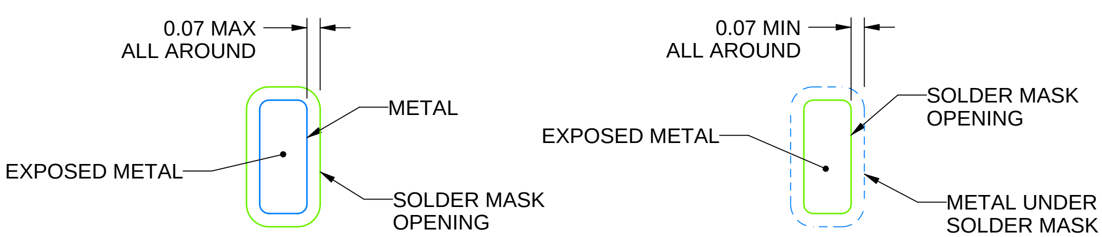


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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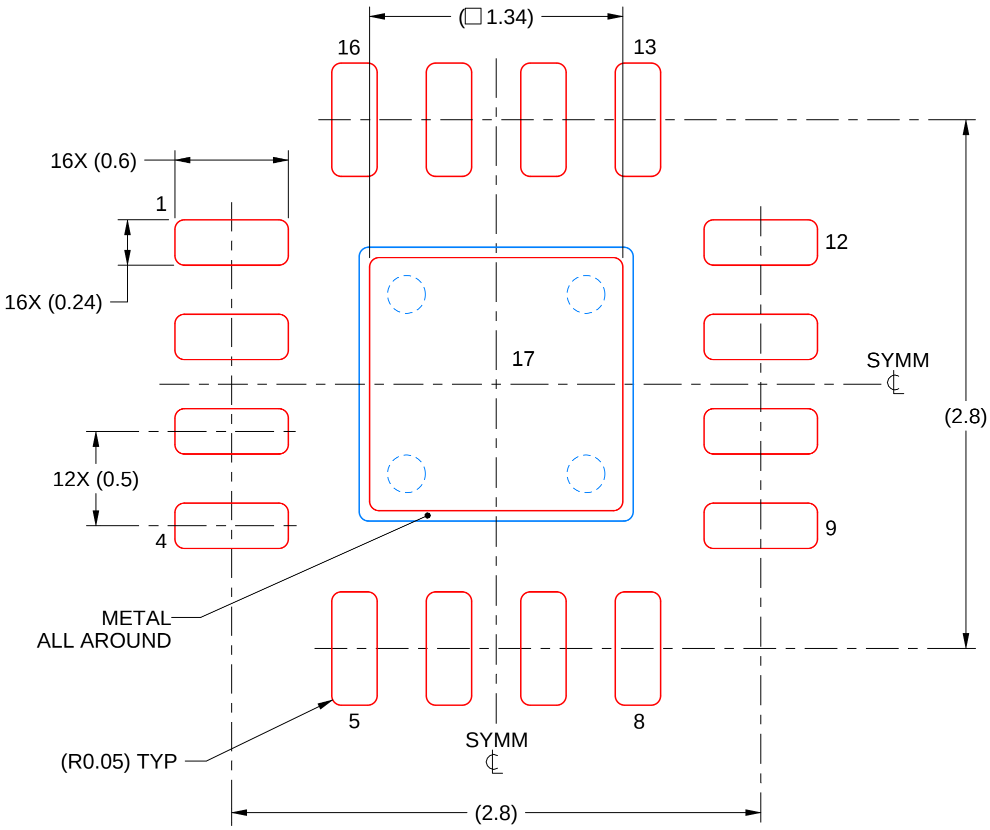
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.