

SN65LBC173A-EP Quadruple RS-485 Differential Line Receiver

1 Features

- Designed for TIA/EIA-485, TIA/EIA-422 and ISO 8482 Applications
- Signaling Rates ⁽¹⁾ up to 50 Mbps.
- Fail-Safe in Bus Short-Circuit, Open-Circuit, and Idle-Bus Conditions
- ESD Protection on Bus Inputs Exceeds 6 kV
- Common-Mode Bus Input Range –7 V to 12 V
- Propagation Delay Times < 18 ns
- Low-Standby Power Consumption < 32 μ A
- Pin-Compatible Upgrade for AM26LS32, DS96F173, LTC488, and SN75173

2 Applications

- Supports Defense, Aerospace, and Medical Applications
 - Controlled Baseline
 - One Assembly and Test Site
 - One Fabrication Site
 - Extended Product Life Cycle
 - Extended Product-Change Notification
 - Product Traceability

3 Description

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications.

This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS[®], facilitating low-power consumption and robustness.

The G and \overline{G} inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

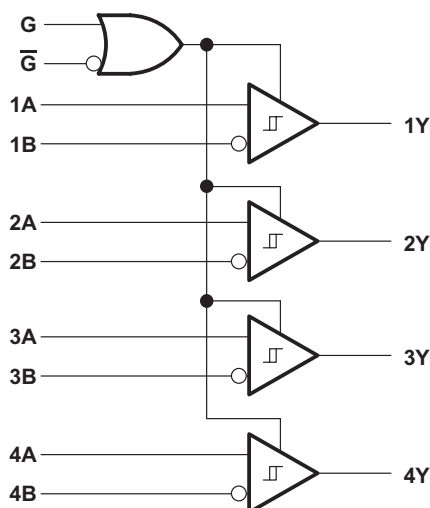
Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LBC173A-EP	SOIC (16)	9.90 mm × 3.90 mm

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram



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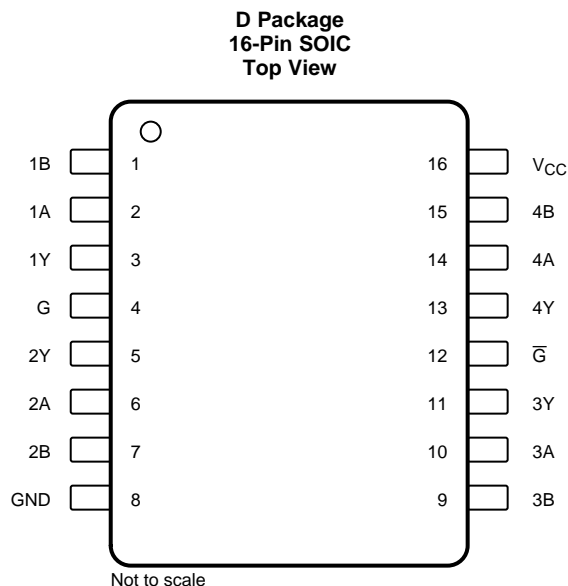
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4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	2	I	RS-485 differential input (noninverting).
1B	1	I	RS-485 differential input (inverting).
1Y	3	O	Logic level output.
2A	6	I	RS-485 differential input (noninverting).
2B	7	I	RS-485 differential input (inverting).
2Y	5	O	Logic level output.
3A	10	I	RS-485 differential input (noninverting).
3B	9	I	RS-485 differential input (inverting).
3Y	11	O	Logic level output.
4A	14	I	RS-485 differential input (noninverting).
4B	15	I	RS-485 differential input (inverting).
4Y	13	O	Logic level output.
\overline{G}	12	I	Active-low select.
G	4	I	Active-high select.
GND	8	—	Ground.
V _{CC}	16	—	Power supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC} ⁽²⁾	−0.3	6	V
Voltage at any bus input (DC)	−10	15	V
Voltage at any bus input (transient pulse through 100 Ω , see Figure 10)	−30	30	V
Input voltage at G and \overline{G} , V_I	−0.5	$V_{CC} + 0.5$	V
Receiver output current, I_O	−10	10	mA
Storage temperature, T_{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to GND.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	A and B to GND	±6000
		All pins	±5000
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	All pins	±2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
	Voltage at any bus terminal	A, B		12	V
V_{IH}	High-level input voltage	G, \overline{G}		V_{CC}	V
V_{IL}	Low-level input voltage			0.8	V
	Output current	Y		8	mA
T_J	Junction temperature			−55	125

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65LBC173A-EP	UNITS
		D (SOIC)	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	78	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	39.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	35.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going differential input voltage threshold		−7 V ≤ V _{CM} ≤ 12 V (V _{CM} = (V _A + V _B) / 2)			−80	−10	mV
V _{IT−}	Negative-going differential input voltage threshold				−200	−120		mV
V _{HYS}	Hysteresis voltage (V _{IT+} − V _{IT−})					40		mV
V _{IK}	Input clamp voltage		I _I = −18 mA		−1.5	−0.8		V
V _{OH}	High-level output voltage		V _{ID} = 200 mV, I _{OH} = −8 mA	See Figure 6	2.7	4.8		V
V _{OL}	Low-level output voltage		V _{ID} = −200 mV, I _{OL} = 8 mA			0.2	0.4	V
I _{OZ}	High-impedance-state output current		V _O = 0 V to V _{CC}		−1		1	μA
I _I	Line input current		Other input at 0 V, V _{CC} = 0 V or 5 V	V _I = 12 V			0.9	mA
				V _I = −7 V	−0.7			
I _{IH}	High-level input current	Enable inputs G, \overline{G}					110	μA
I _{IL}	Low-level input current				−100			μA
R _I	Input resistance	A, B inputs			12			kΩ
I _{CC}	Supply current		V _{ID} = 5 V	G at 0 V, \overline{G} at V _{CC}			32	μA
			No load	G at V _{CC} , \overline{G} at 0 V		11	16	mA

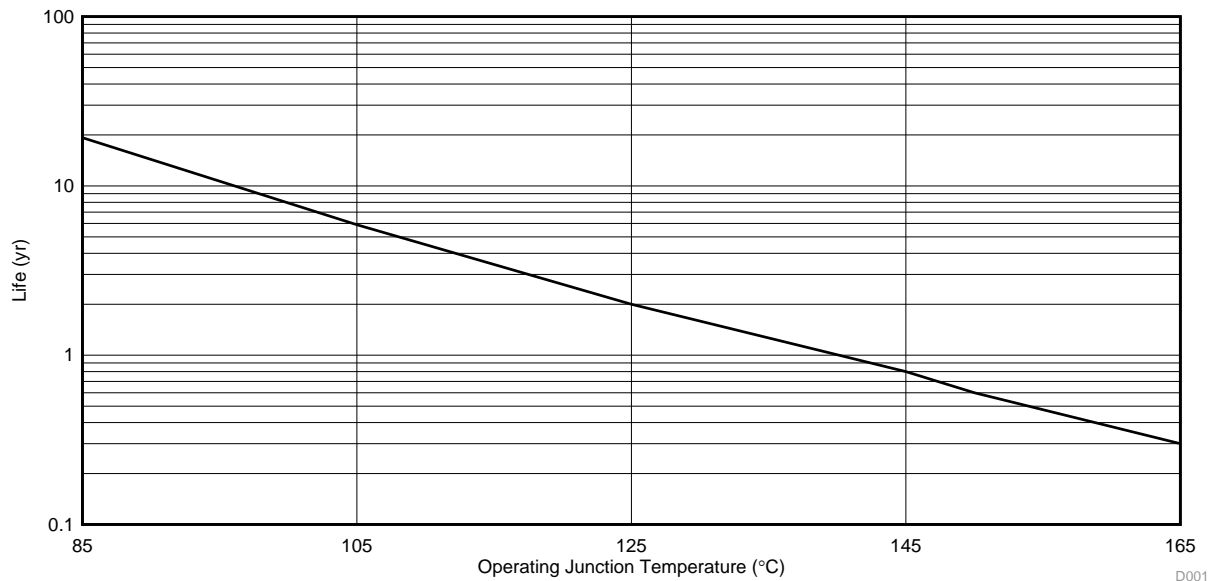
(1) All typical values are at V_{CC} = 5 V and 25°C.

6.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _r	Differential output voltage rise time	V _{ID} = –3 V to 3 V, See Figure 7		2	7	ns
t _f	Differential output voltage fall time			2	7	ns
t _{PLH}	Propagation delay time, low-to-high level output		8	12	18	ns
t _{PHL}	Propagation delay time, high-to-low level output		8	12	18	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 8		27	39	ns
t _{PHZ}	Propagation delay time, high-level-output-to-high impedance			7	24	ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 9		29	39	ns
t _{PLZ}	Propagation delay time, low-level-output-to-high impedance			12	18	ns
t _{sk(p)}	Pulse skew (t _{PLH} – t _{PHL})			0.2	2	ns
t _{sk(o)}	Output skew ⁽¹⁾				3	ns
t _{sk(pp)}	Part-to-part skew ⁽²⁾				3	ns

- (1) Output skew (t_{sk(o)}) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
- (2) Part-to-part skew (t_{sk(pp)}) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.



- (1) See data sheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

Figure 1. SN65LBC173A-EP Wirebond Life Derating Chart

6.7 Typical Characteristics

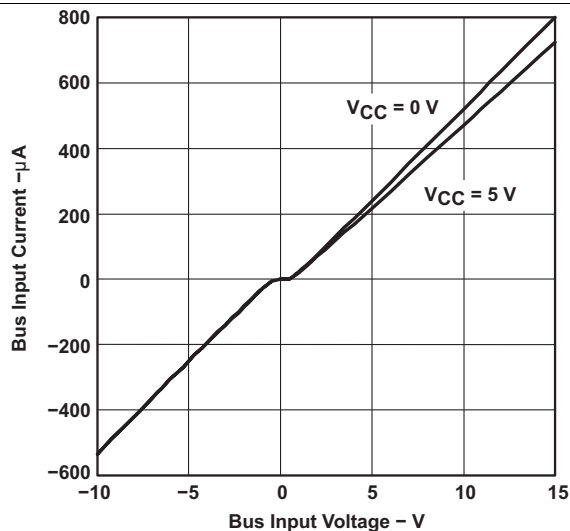


Figure 2. Bus Input Current vs Bus Input Voltage

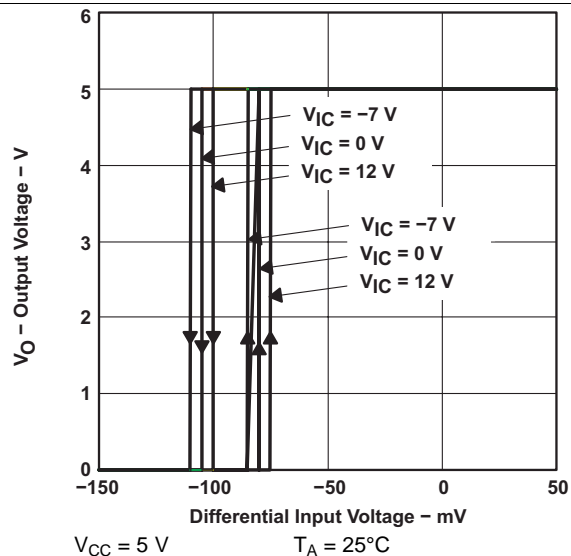


Figure 3. Output Voltage vs Differential Input Voltage

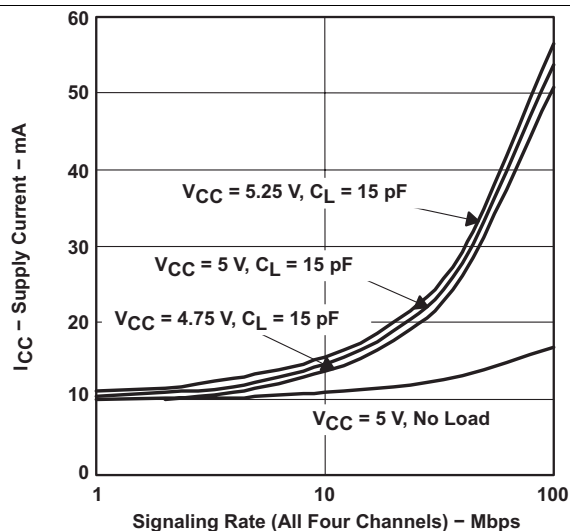


Figure 4. Supply Current vs Signaling Rate (All Four Channels)

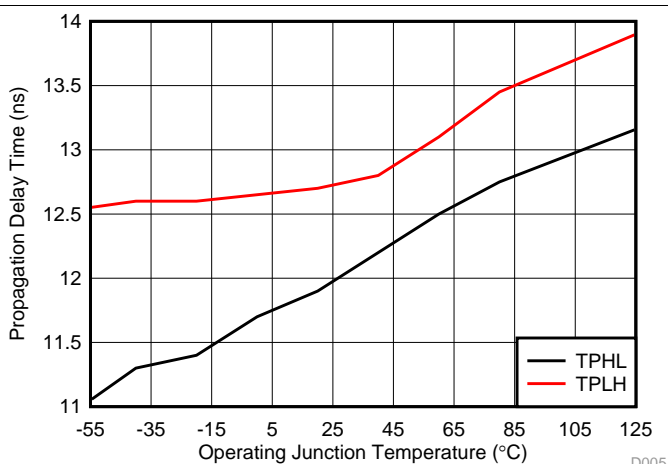


Figure 5. Propagation Delay Time vs Free-Air Temperature

7 Parameter Measurement Information

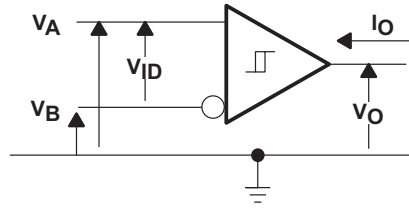
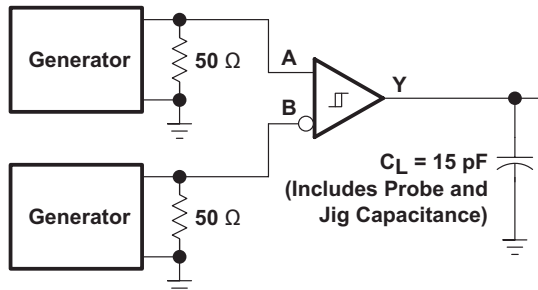
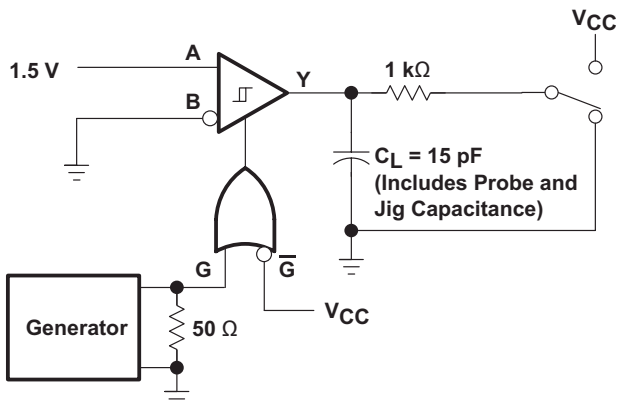


Figure 6. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
 $t_r < 6$ ns, $Z_O = 50 \Omega$

Figure 7. Switching Test Circuit and Waveforms



Generators: PRR = 1 MHz, 50% Duty Cycle,
 $t_r < 6$ ns, $Z_O = 50 \Omega$

Figure 8. Test Circuit Waveforms, t_{PZH} and t_{PHZ}

Parameter Measurement Information (continued)

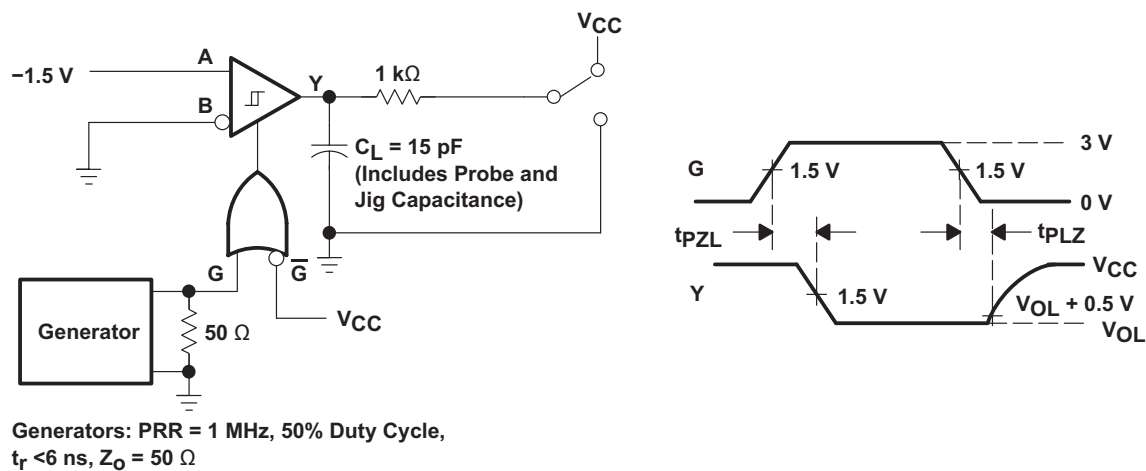


Figure 9. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

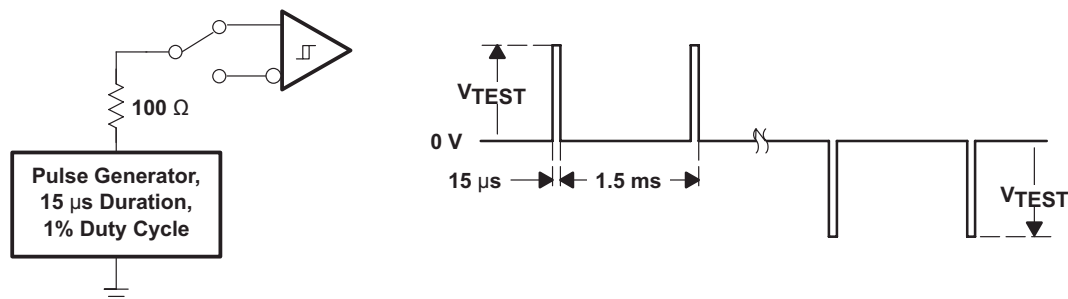


Figure 10. Test Circuit and Waveform, Transient Over-Voltage Test

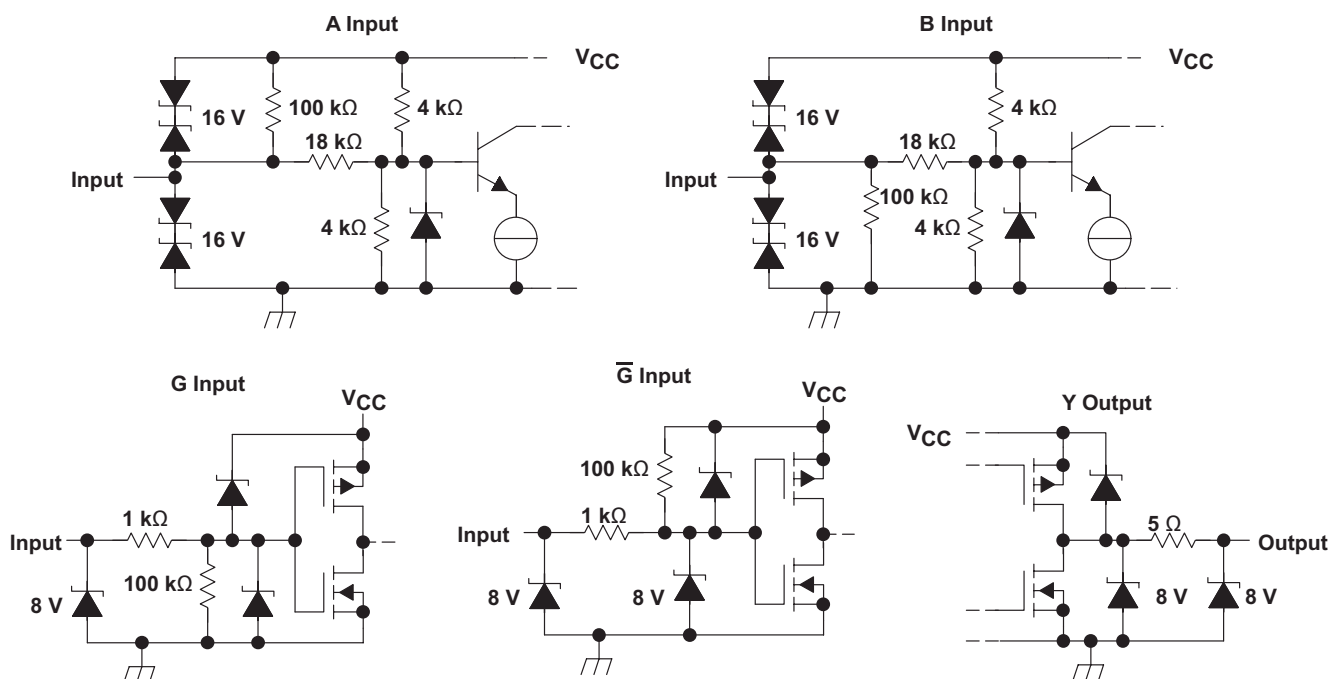


Figure 11. Equivalent Input and Output Schematic Diagrams

8 Detailed Description

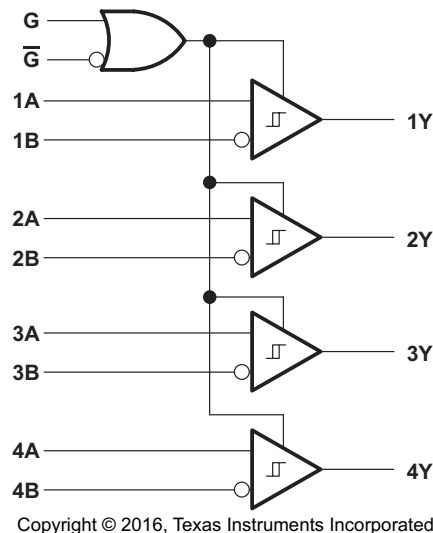
8.1 Overview

The SN65LBC173A is a quadruple differential line receiver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 50 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The receiver operates over a wide range of positive and negative common-mode input voltages, and features ESD protection to 6 kV, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS®, facilitating low-power consumption and robustness.

The G and \overline{G} inputs provide enable control logic for either positive- or negative-logic enabling all four drivers. When disabled or powered off, the receiver inputs present a high-impedance to the bus for reduced system loading.

8.2 Functional Block Diagram



8.3 Feature Description

The device can be configured using the G and \overline{G} logic inputs to select receiver output. The high voltage or logic 1 on the G pin allows the device to operate on an active-high, and having a low voltage or logic 0 on the \overline{G} enables active low operation. These are simple ways to configure the logic to match that of the receiving or transmitting controller or microprocessor.

8.4 Device Functional Modes

The receivers implemented in these RS-485 device can be configured using the G and \overline{G} logic pins to be enabled or disabled. This allows users to ignore or filter out transmissions as desired.

Table 1. Function Table⁽¹⁾

INPUT A - B (V_{ID})	ENABLES		OUTPUT Y
	G	\overline{G}	
$V_{ID} \leq -0.2 \text{ V}$	H	X	L
	X	L	
$-0.2 \text{ V} < V_{ID} < -0.01 \text{ V}$	H	X	?
	X	L	
$-0.01 \text{ V} \leq V_{ID}$	H	X	H
	X	L	
X	L	H	Z
	OPEN	OPEN	
Short circuit	H	X	H
	X	L	
Open circuit	H	X	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

9 Application and Implementation

NOTE

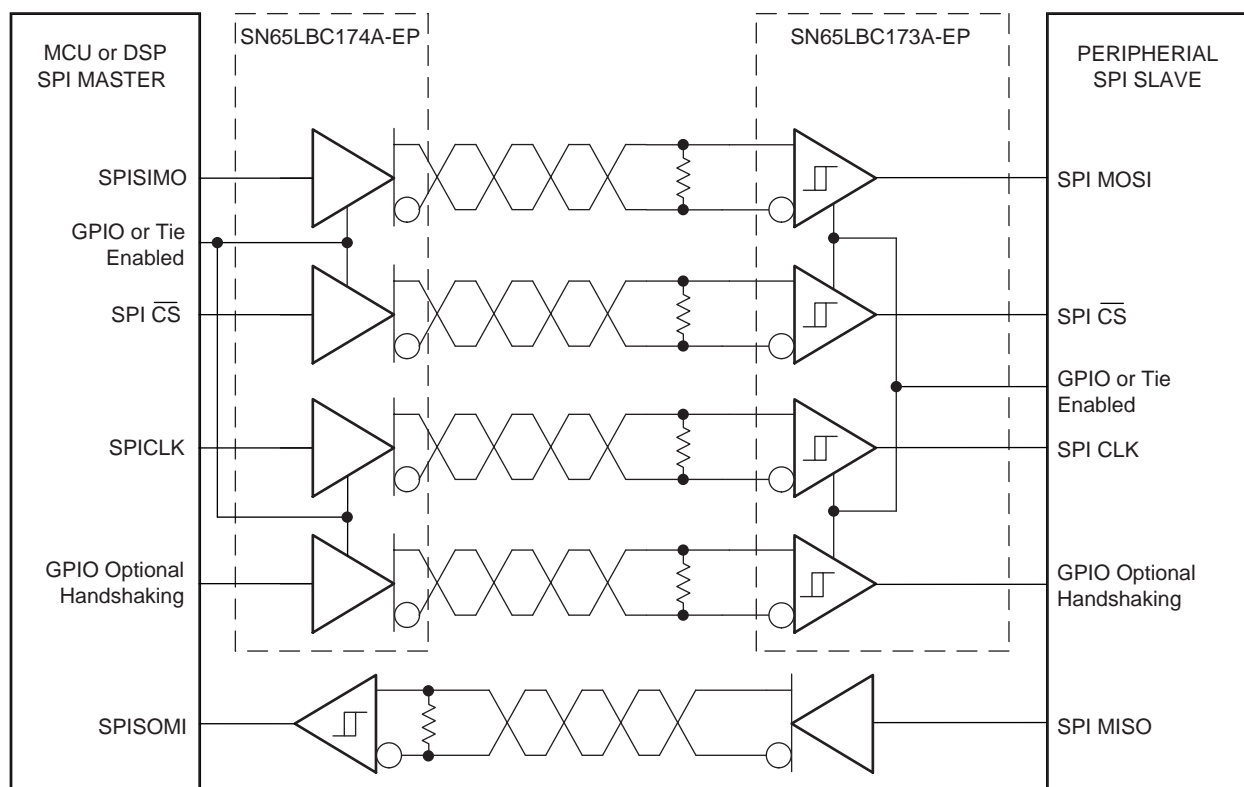
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Extending SPI operation over RS-485 link.

9.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.



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Figure 12. DSP-to-DSP Link via Serial Peripheral Interface

9.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

9.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled.

Typical Application (continued)

The link shown can operate at up to 50 Mbps, well within the capability of most SPI links.

9.2.3 Application Curves

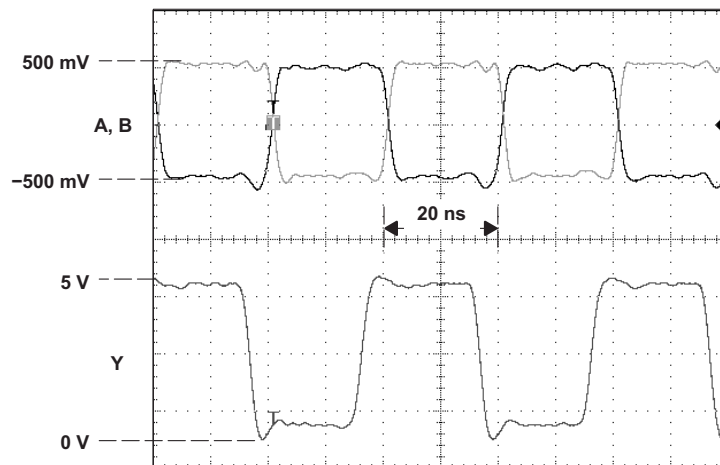


Figure 13. Receiver Inputs and Outputs, 50-Mbps Signaling Rate

10 Power Supply Recommendations

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to buss as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

11.2 Layout Example

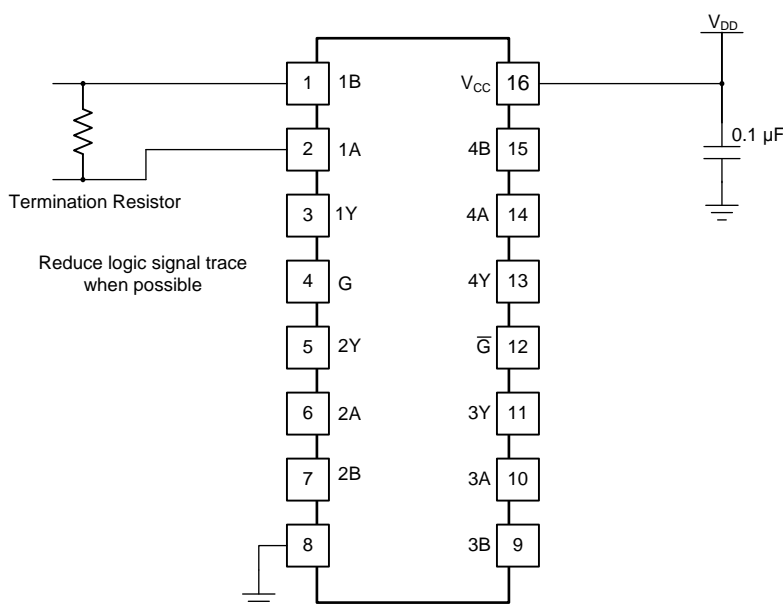


Figure 14. Layout with PCB Recommendations

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC173AMDREP	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP
SN65LBC173AMDREP.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP
V62/13623-02XE	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LBC173AEP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN65LBC173A-EP :

- Catalog : [SN65LBC173A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC173AMDREP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC173AMDREP	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

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