SN65LBC174A-EP Quadruple RS-485 Differential Line Driver

1 Features

- VID V62/07611
- Designed for TIA/EIA-485, TIA/EIA-422, and ISO 8482 applications
- Signaling rates up to 30 Mbps (1)
- Propagation delay times < 11 ns
- Low standby power consumption 1.5-mA max
- Driver positive- and negative-current limiting
- Power-up and power-down glitch free for line-insertion applications
- Thermal shutdown protection
- Industry standard pinout, compatible with SN75174, MC3487, DS96174, LTC487, and MAX3042
- Supports defense, aerospace, and medical applications
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Available in military (–55°C to 125°C) temperature range
  - Extended product life cycle
  - Extended product-change notification
  - Product traceability

(1) The signaling rate of a line is the number of voltage transitions that are made per second, expressed in the unit bits per second (bps).

2 Applications

- Transmission at signaling rates up to 30 Mbps
- Avionics, radar
- GPS navigation for missiles
- Industrial transportation
- High-speed multipoint data transmission applications in noisy environments

3 Description

The SN65LBC174A-EP is a quadruple differential line driver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

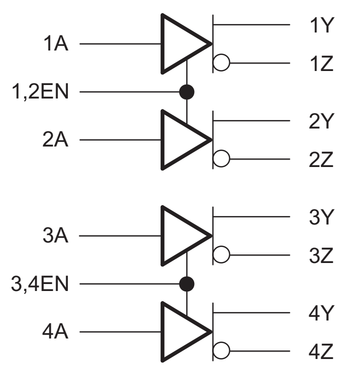
This device is optimized for balanced multipoint bus transmission at signaling rates up to 30-million bits per second (Mbps). The transmission media may be printed-circuit-board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LBC174A-EP	SOIC (20)	7.50 × 12.80
	SOIC (16)	7.50 × 10.30

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2006) to Revision A **Page**

- Updated data sheet to superior standards ... 1
- Added pinout drawing for 16-pin DW ... 3
- Added 16-pin DW and updated the Pin Functions table ... 4
- Added ESD value for 16-pin DW package ... 5
- Added updated thermal metrics ... 5

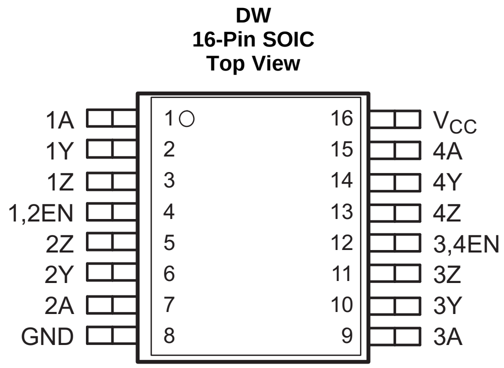
5 Description (continued)

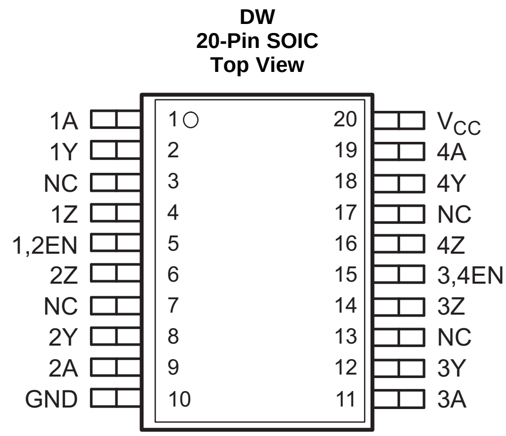
Each driver features current limiting and thermal-shutdown circuitry, making it suitable for high-speed multipoint applications in noisy environments. The device is designed using LinBiCMOS™ technology, facilitating low power consumption and robustness.

The two enable (EN) inputs provide pair-wise driver enabling, or can be externally tied together to provide enable control of all four drivers with one signal. When disabled or powered off, the driver outputs present a high impedance to the bus for reduced system loading.

The SN65LBC174A-EP is characterized for operation over the temperature range of –55°C to 125°C.

6 Pin Configuration and Functions





Pin Functions

PIN			I/O	DESCRIPTION
NAME	16 PINS	20 PINS		
1A	1	1	Digital input	Port 1 A data input
1Y	2	2	Bus output	Bus port 1 Y (complementary to 1 Z)
NC	—	3	No Connect	Physically not connected in package
1Z	3	4	Bus output	Bus port 1 Z (complementary to 1 Y)
1,2EN	4	5	Digital input	Bus output port 1 and 2 driver enable
2Z	5	6	Bus output	Bus port 2 Z (complementary to 2 Y)
NC	—	7	No Connect	Physically not connected in package
2Y	6	8	Bus output	Bus port 2 Y (complementary to 2 Z)
2A	7	9	Digital input	Port 2 A data input
GND	8	10	Ground	Device ground
3A	9	11	Digital input	Port 3 A data input
3Y	10	12	Bus output	Bus port 3 Y (complementary to 3 Z)
NC	—	13	No Connect	Physically not connected in package
3Z	11	14	Bus output	Bus port 3 Z (complementary to 3 Y)
3,4EN	12	15	Digital input	Bus output port 3 and 4 driver enable
4Z	13	16	Bus output	Bus port 4 Z (complementary to 4 Y)
NC	—	17	No Connect	Physically not connected in package
4Y	14	18	Bus output	Bus port 4 Y (complementary to 4 Z)
4A	15	19	Digital input	Port 4 A data input
V_{CC}	16	20	V_{CC}	Device power

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage[2]	–0.3	6	V
	Voltage at any bus (dc)	–10	15	V
	Voltage at any bus (transient pulse through 100 Ω, See Figure 14)	–30	30	V
V_I	Input voltage at any A or EN terminal	–0.5	V_{CC} + 0.5	V
T_{stg}	Storage temperature[3]	–65	150	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Y, Z (20-pin DW)	±13,000	V
			Y, Z (16-pin DW)	±10,000	
			All other pins	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	All pins	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at any bus terminal	Y, Z	–7		12	V
V_{IH}	High-level input voltage	A, EN	2		V_{CC}	V
V_{IL}	Low-level input voltage	A, EN	0		0.8	V
	Output current		–60		60	mA
T_A	Operating free-air temperature		–55		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		SN65LBC174A-EP DW (SOIC)		UNIT
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.3	60.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.2	24.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.8	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

7.5 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude[2]	No load (open circuit)		3		V_{CC}	V
		R_L = 54 Ω, See Figure 7		0.8	1.6	2.5	
		With common-mode loading, See Figure 8		0.8	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See Figure 7		–0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 9		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 9		–0.04		0.04	V
I_I	Input current	A, G, $\overline{G}$		–70		70	µA
I_{OS}	Short-circuit output current	V_{TEST} = –7 V to 12 V, See Figure 13	V_I = 0 V	–200		200	mA
			$V_I = V_{CC}$				
I_{OZ}	High-impedance-state output current		EN at 0 V	–50		50	µA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0 V	–10		10	µA
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load	All drivers enabled			25	mA
			All drivers disabled			1.5	

(1) All typical values are at V_{CC} = 5 V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibility of lower output signal into account in determining the maximum signal transmission distance.

7.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 10	T_A= 25°C	4.0	8	11	ns
			T_A= –55°C to 125°C	4.0		16	
t_{PHL}	Propagation delay time, high- to low-level output		T_A= 25°C	4.0	8	11	ns
			T_A= –55°C to 125°C	4.0		16	
t_r	Differential output voltage rise time		T_A= 25°C	3	7.5	11	ns
			T_A= –55°C to 125°C	3		24	
t_f	Differential output voltage fall time		T_A= 25°C	3	7.5	11	ns
			T_A= –55°C to 125°C	3		24	
$t_{sk(p)}$	Pulse skew $\|t_{PLH} - t_{PHL}\|$				0.6		ns
$t_{sk(o)}$	Output skew(1)				2		ns
$t_{sk(pp)}$	Part-to-part skew(2)				3		ns
t_{PZH}	Propagation delay time, high impedance to high-level output	See Figure 11				25	ns
t_{PHZ}	Propagation delay time, high-level output to high impedance					25	ns
t_{PZL}	Propagation delay time, high impedance to low-level output	See Figure 12				30	ns
t_{PLZ}	Propagation delay time, low-level output to high impedance					20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.7 Typical Characteristics

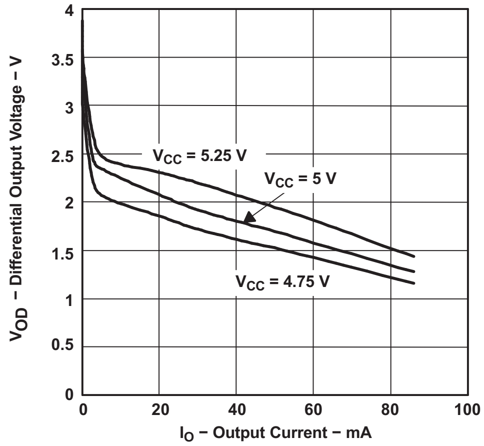


Figure 1. Differential Output Voltage vs Output Current

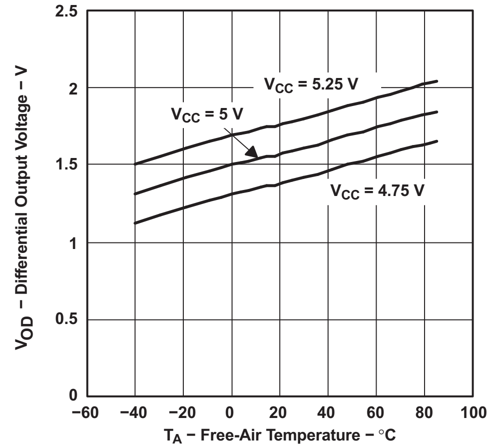


Figure 2. Differential Output Voltage vs Free-Air Temperature

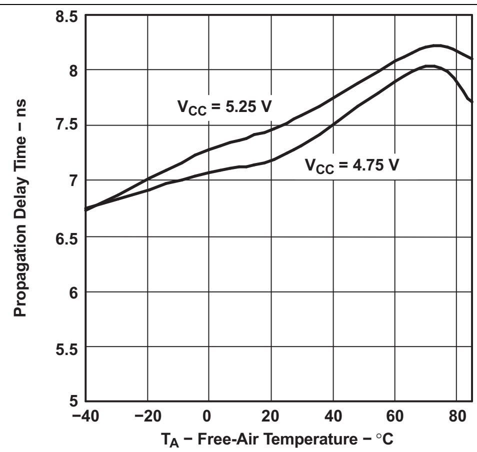
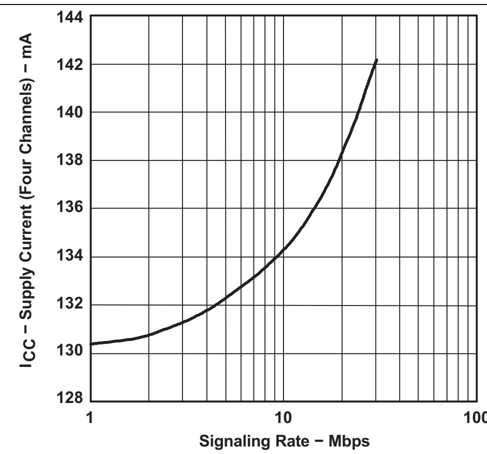
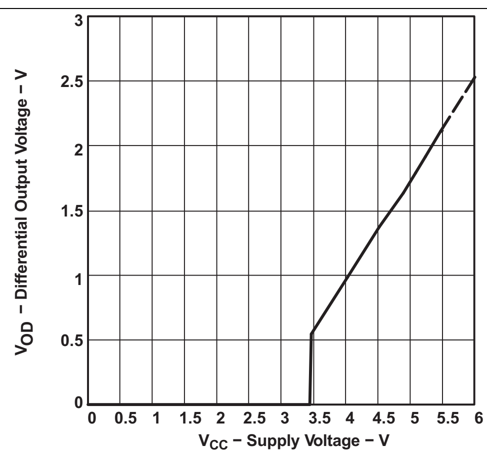


Figure 3. Propagation Delay Time vs Free-Air Temperature



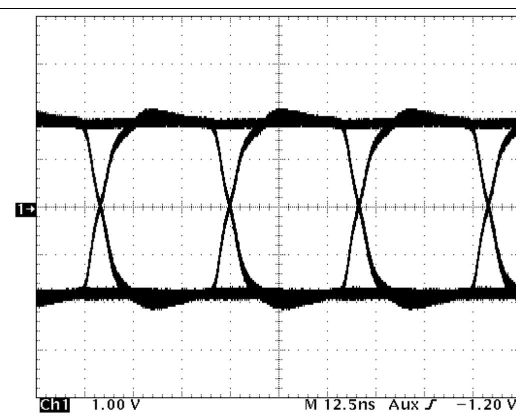
R_L = 54 Ω C_L = 50 pF (Each Channel)

Figure 4. Supply Current (Four Channels) vs Signaling Rate



R_L = 54 Ω

Figure 5. Differential Output Voltage vs Supply Voltage



R_L = 54 Ω C_L = 50 pF

Figure 6. Eye Pattern, Pseudo-Random Data at 30 Mbps

8 Parameter Measurement Information

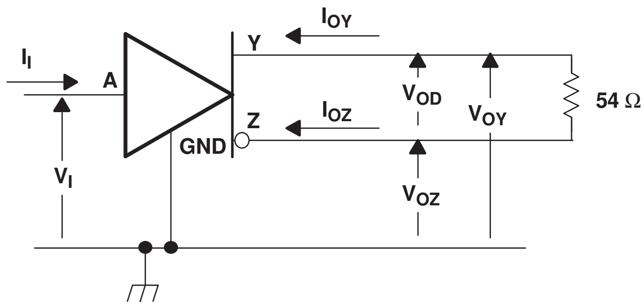


Figure 7. Test Circuit, V_{OD} Without Common-Mode Loading

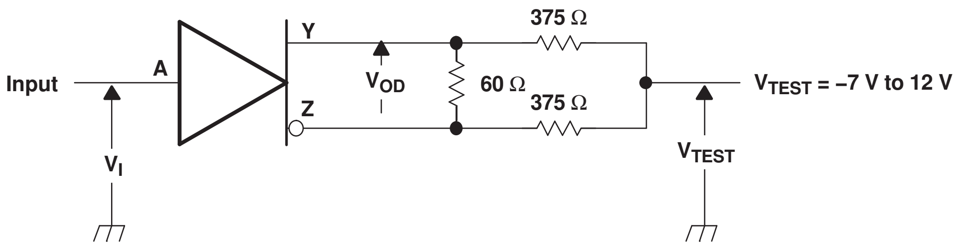
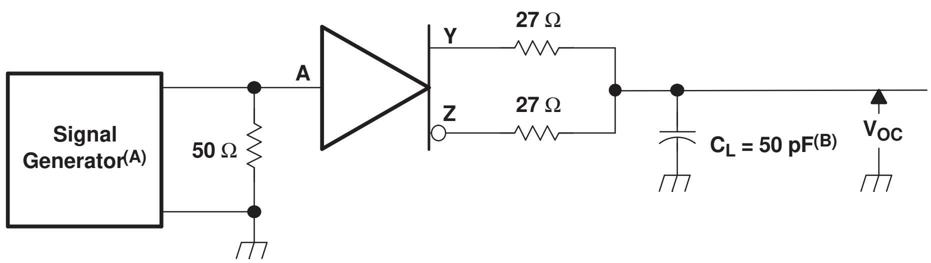


Figure 8. Test Circuit, V_{OD} With Common-Mode Loading

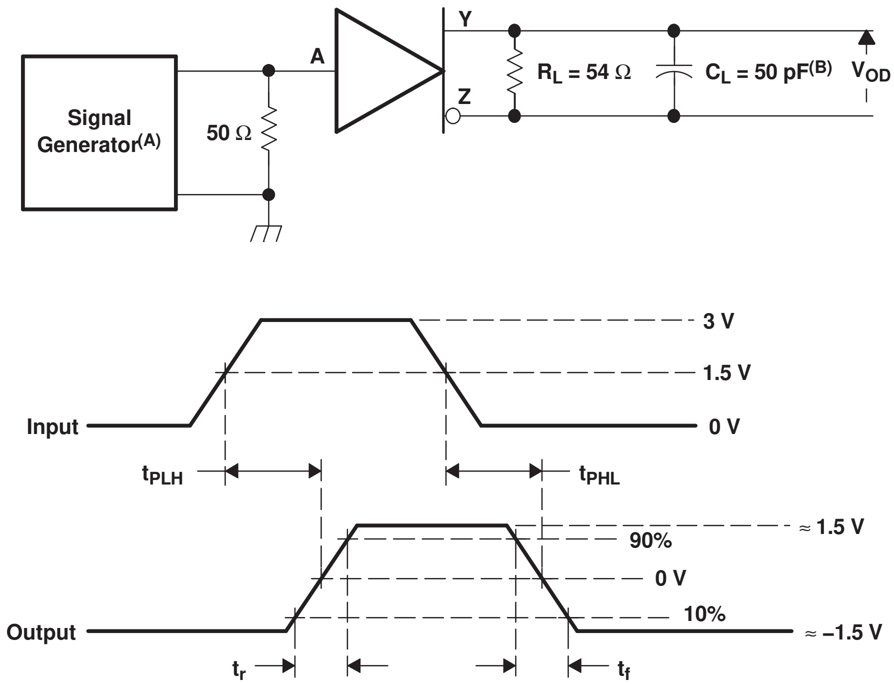


PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Includes probe and jig capacitance.

Figure 9. V_{OC} Test Circuit

Parameter Measurement Information (continued)

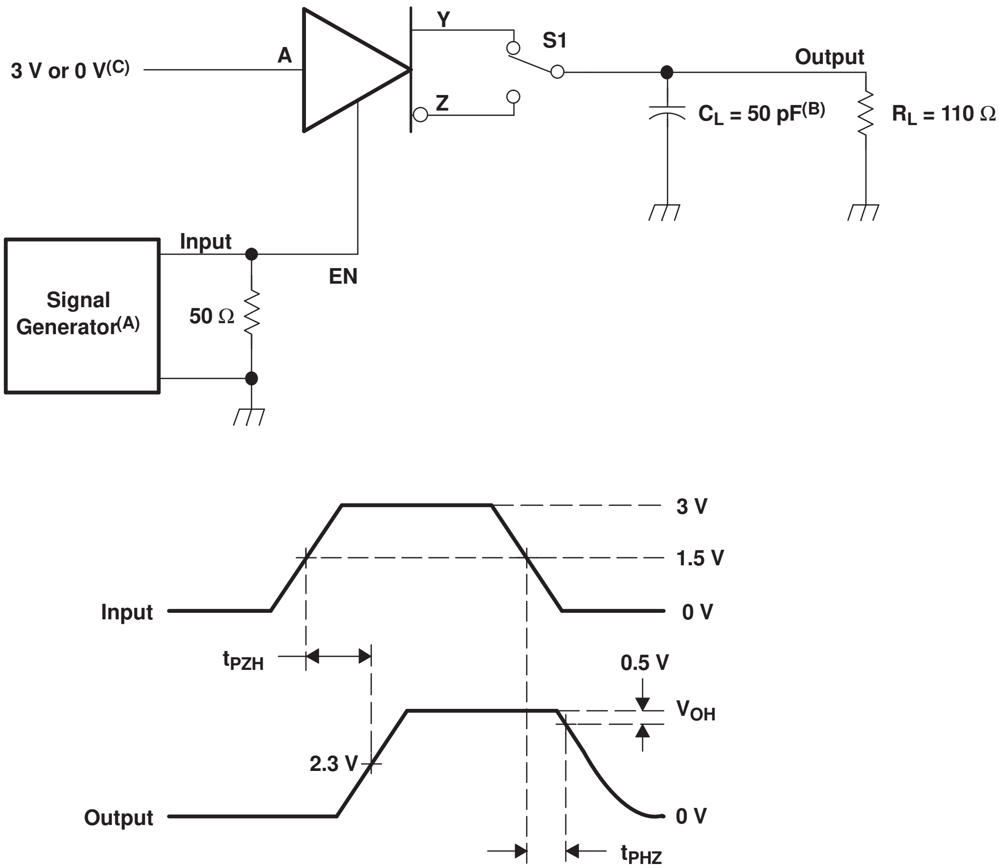


PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Includes probe and jig capacitance.

Figure 10. Output Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)



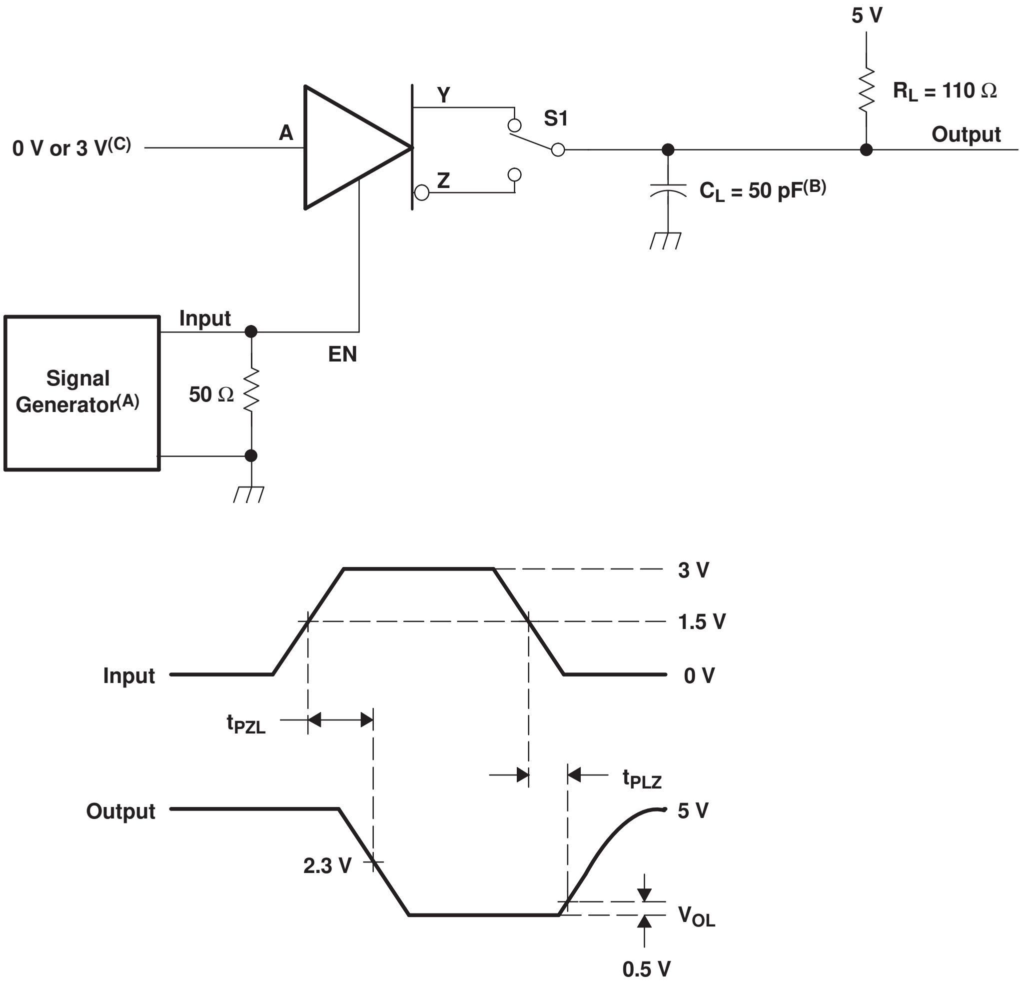
PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Includes probe and jig capacitance.

3 V if testing Y output, 0 V if testing Z output.

Figure 11. Enable Timing Test Circuit and Waveforms, T_{PZH} and T_{PHZ}

Parameter Measurement Information (continued)



PRR = 1 MHz, 50% duty cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω

Includes probe and jig capacitance.

3 V if testing Y output, 0 V if testing Z output.

Figure 12. Enable Timing Test Circuit and Waveforms, T_{PZL} and T_{PLZ}

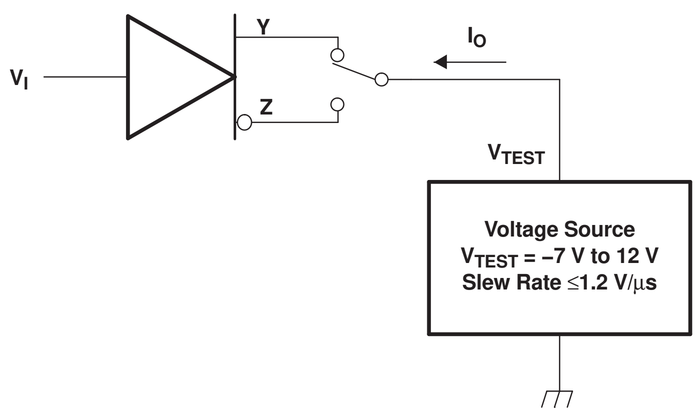


Figure 13. Test Circuit, Short-Circuit Output Current

Parameter Measurement Information (continued)

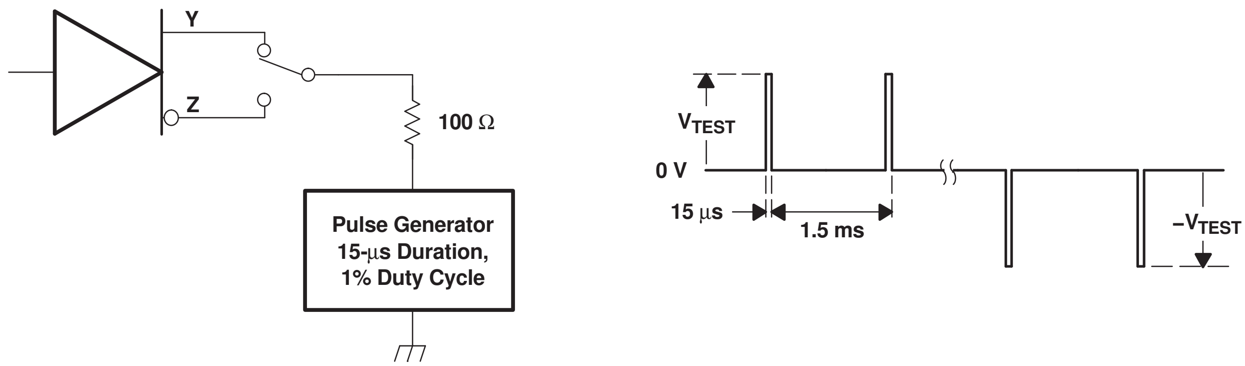


Figure 14. Test Circuit Waveform, Transient Overvoltage Test

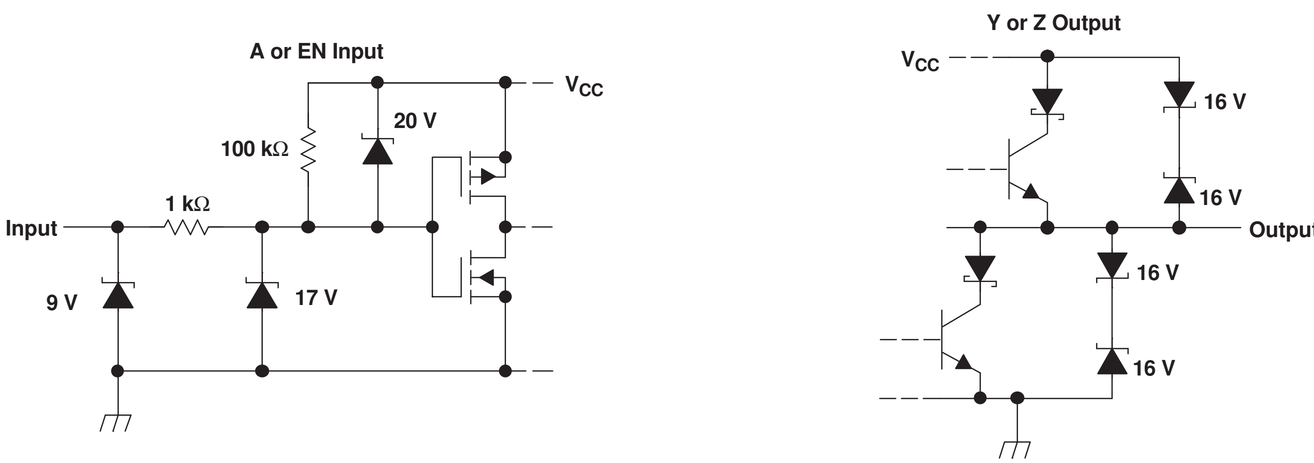


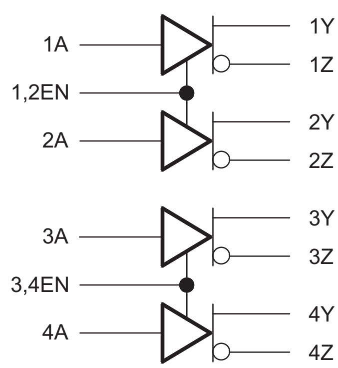
Figure 15. Equivalent Input and Output Schematic Diagrams

9 Detailed Description

9.1 Overview

The SN65LBC174A-EP is a quadruple differential line driver with tri-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 (Euro RS-485) applications. This device is optimized for balanced multipoint bus communication at data rates up to and exceeding 30 million bits per second. The transmission media may be twisted-pair cables, printed-circuit board traces, or backplanes. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment. The transmitter features ESD protection to 12 kV on driver outputs, making it suitable for high-speed multipoint data transmission applications in harsh environments. These devices are designed using LinBiCMOS, facilitating low-power consumption and robustness. Two EN inputs provide pair-wise enable control, or these can be tied together externally to enable all four drivers with the same signal.

9.2 Functional Block Diagram



9.3 Feature Description

The device can be configured using the enable inputs to enable driver pairs 1 and 2, and/or 3 and 4. The high voltage or logic 1 on the EN pin enables the devices differential outputs.

9.4 Device Functional Modes

The drivers implemented in the RS-485 device can be configured using the EN logic pins set to enabled or disabled. This allows users to transmit or idle the bus as desired.

Table 1. Function Table(1) (Each Driver)

INPUT A	ENABLE G	OUTPUTS Y	OUTPUTS Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Extending SPI operation over RS-485 link.

10.2 Typical Application

The following block diagram shows an MCU host connected via RS-485 to a SPI slave device. This device can be an ADC, DAC, MCU, or other SPI slave peripheral.

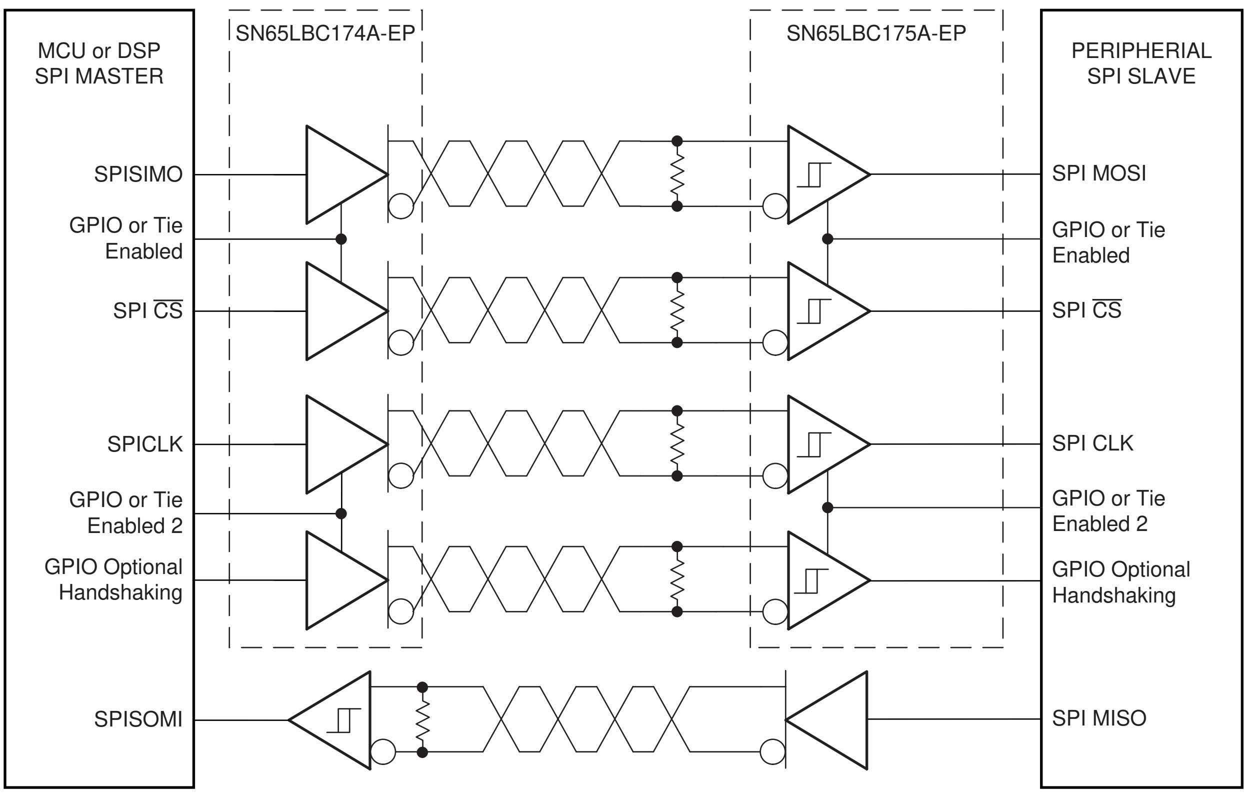


Figure 16. Typical Application Circuit, MCU Master to Slave Link Via Serial Peripheral Interface

10.2.1 Design Requirements

This application can be implemented using standard SPI protocol on DSP or MCU devices. The interface is independent of the specific frame or data requirements of the host or slave device. An additional but not required handshake bit is provided that can be used for customer purposes.

Typical Application (continued)

10.2.2 Detailed Design Procedure

The interface design requirements are fairly straight forward in this single source/destination scenario. Trace lengths and cable lengths need to be matched to maximize SPI timing. If there is a benefit to put the interface to sleep, GPIOs can be used to control the enable signals of the transmitter and receiver. If GPIOs are not available, or constant uptime needed, both the enables on transmit and receive can be hard tied enabled. The link shown can operate at up to 30 Mbps, well within the capability of most SPI links.

10.2.3 Application Curve

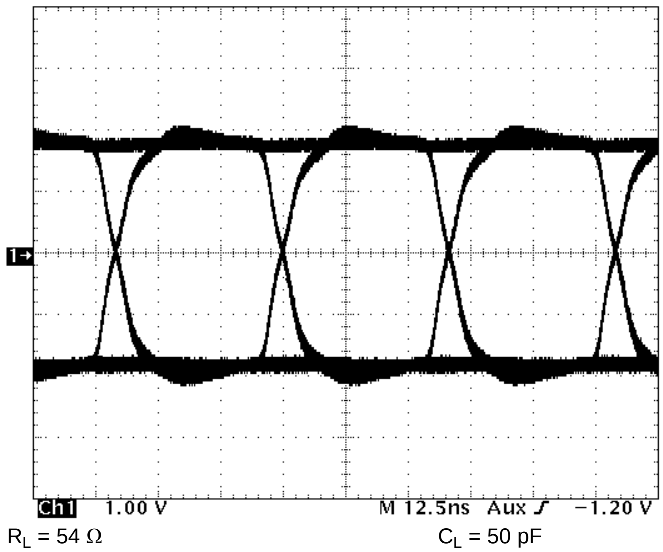


Figure 17. Eye Pattern, Pseudo-Random Data at 30 Mbps

11 Power Supply Recommendations

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies.

12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible.
- Place termination resistor as close as possible to the input pins (if end point node).
- Keep trace lengths from input pins to bus as short as possible to reduce stub lengths and reflections on any nodes that are not end points of bus.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.

12.2 Layout Example

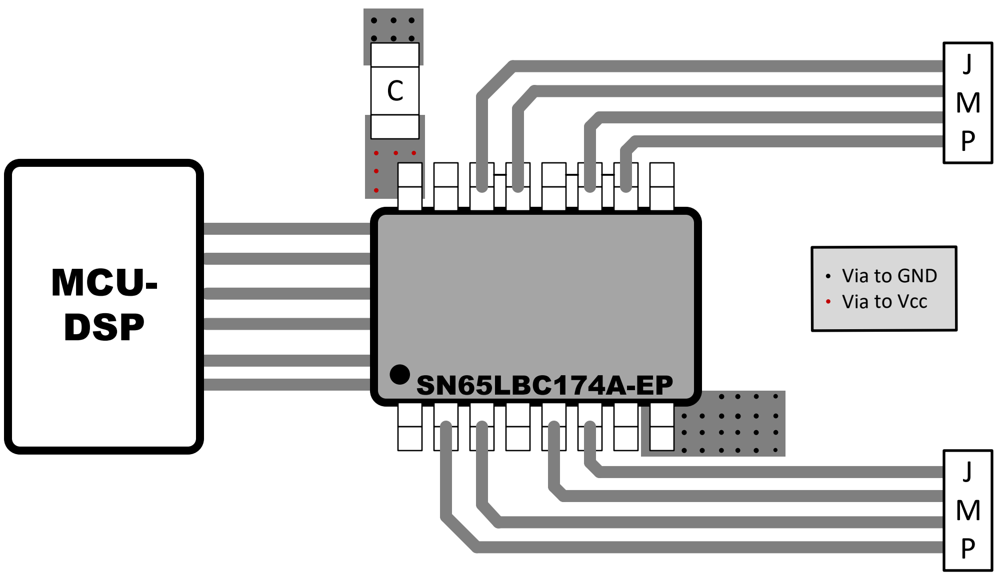


Figure 18. Layout With PCB Recommendations

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.3 Trademarks

LinBiCMOS, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
65LBC174AM16DWREP	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	65LBC174EP
65LBC174AM16DWREP.A	Active	Production	SOIC (DW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	65LBC174EP
SN65LBC174AMDWREP	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP
SN65LBC174AMDWREP.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP
V62/07611-01XE	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	65LBC174EP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LBC174A-EP :

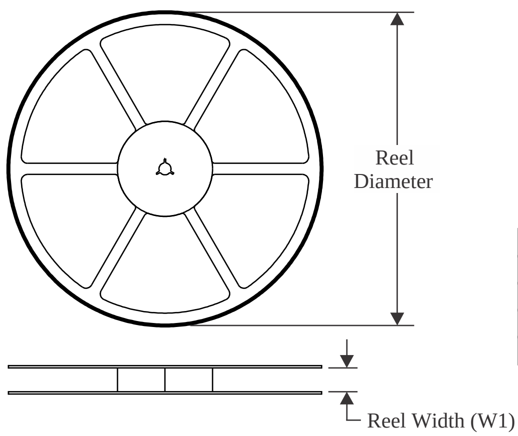
- Catalog : SN65LBC174A

NOTE: Qualified Version Definitions:

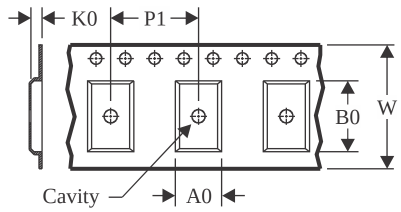
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

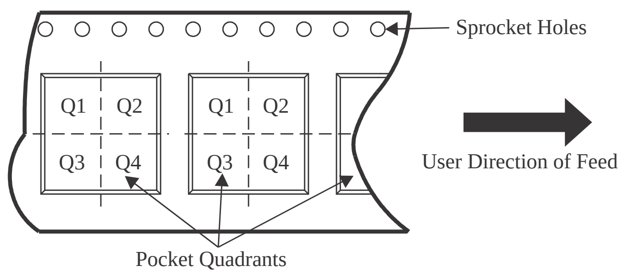


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

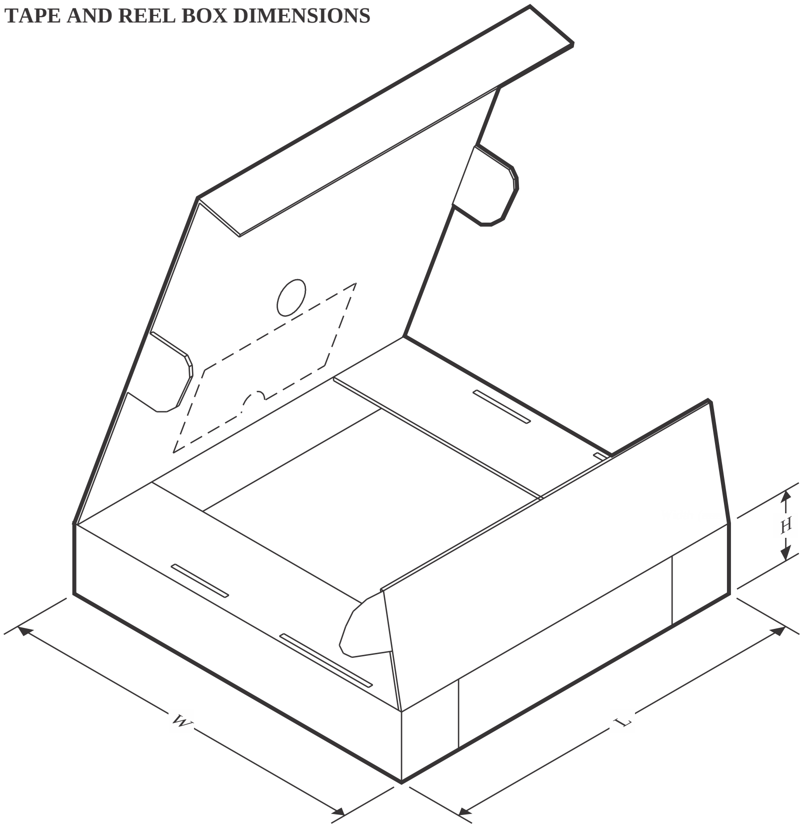
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
65LBC174AM16DWREP	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC174AMDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

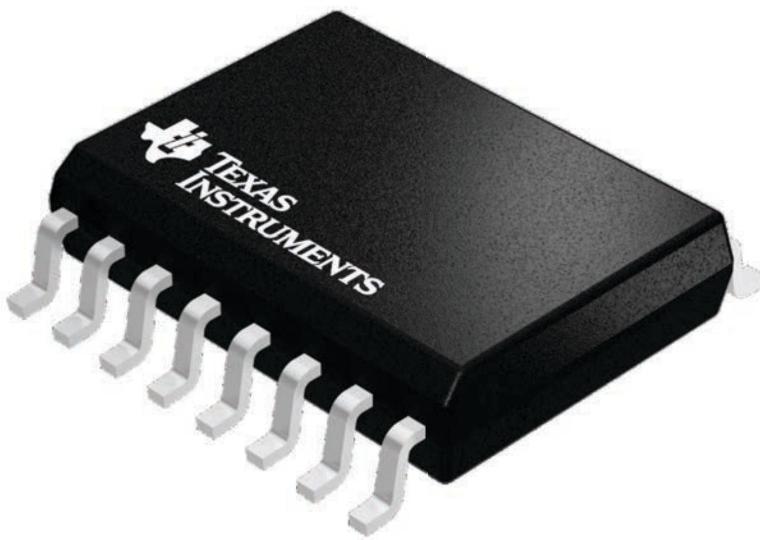
TAPE AND REEL BOX DIMENSIONS



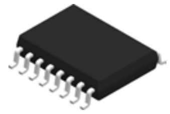
*All dimensions are nominal

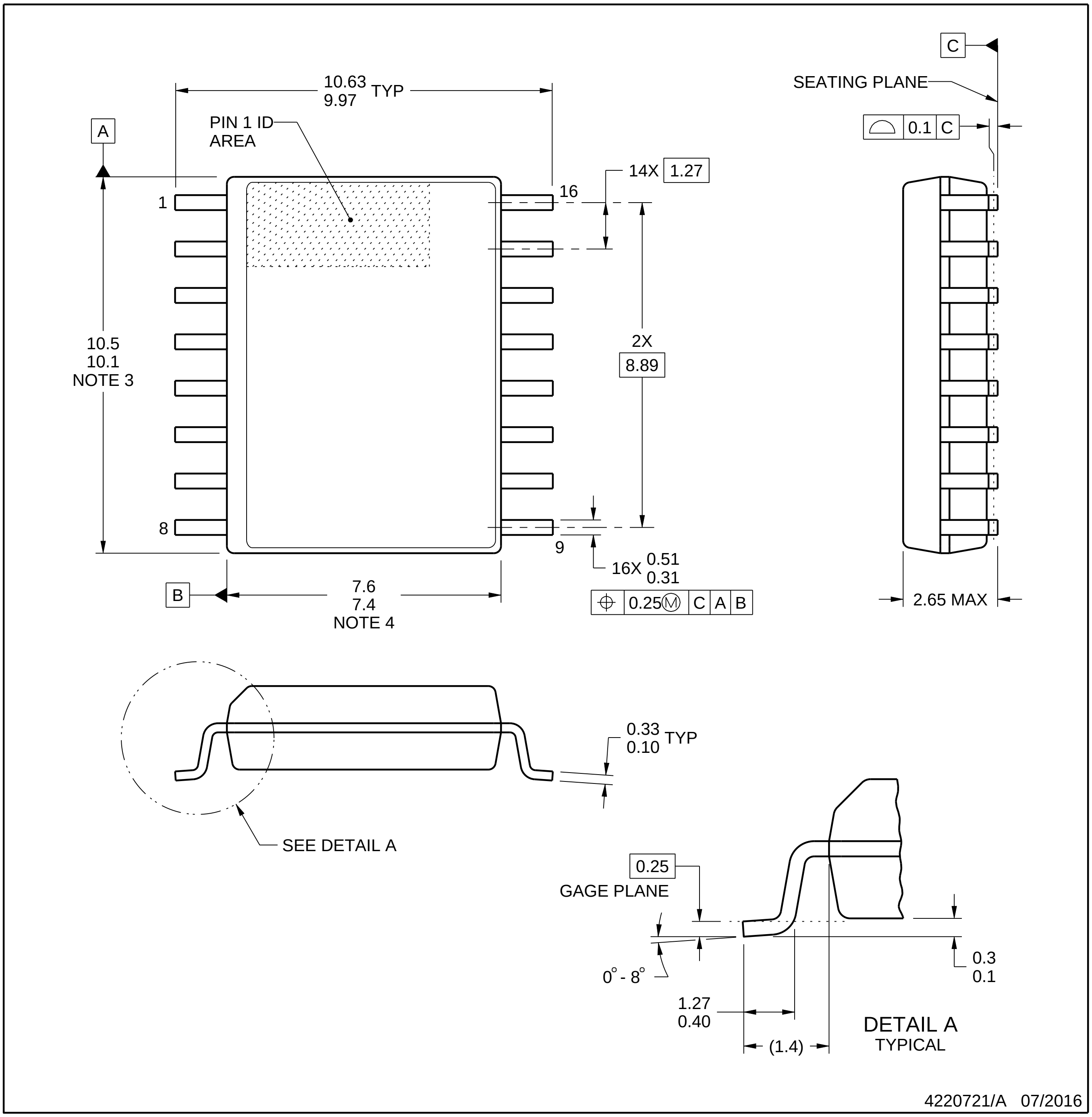
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
65LBC174AM16DWREP	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC174AMDWREP	SOIC	DW	20	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



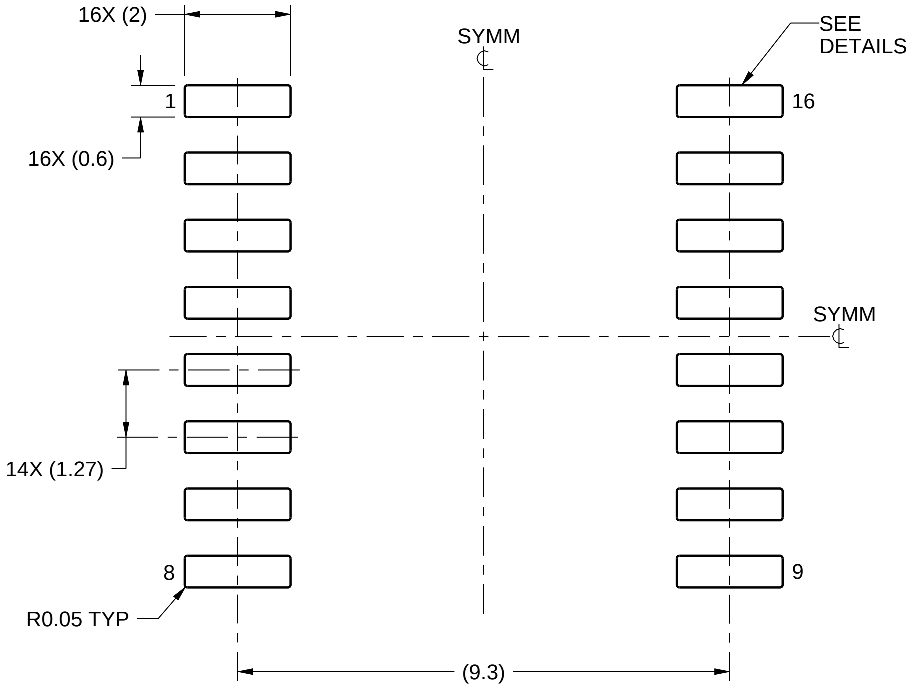
4224780/A



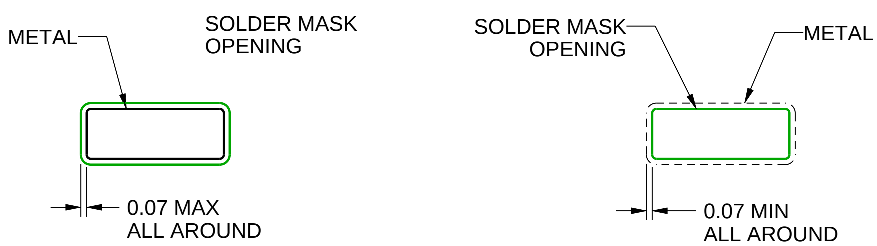


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

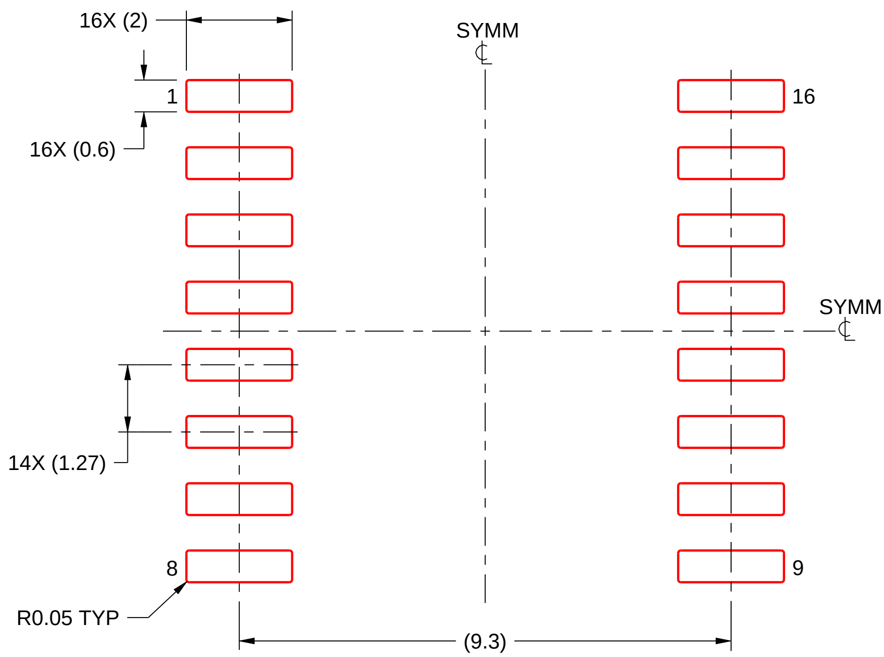
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

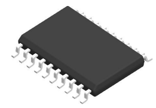


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

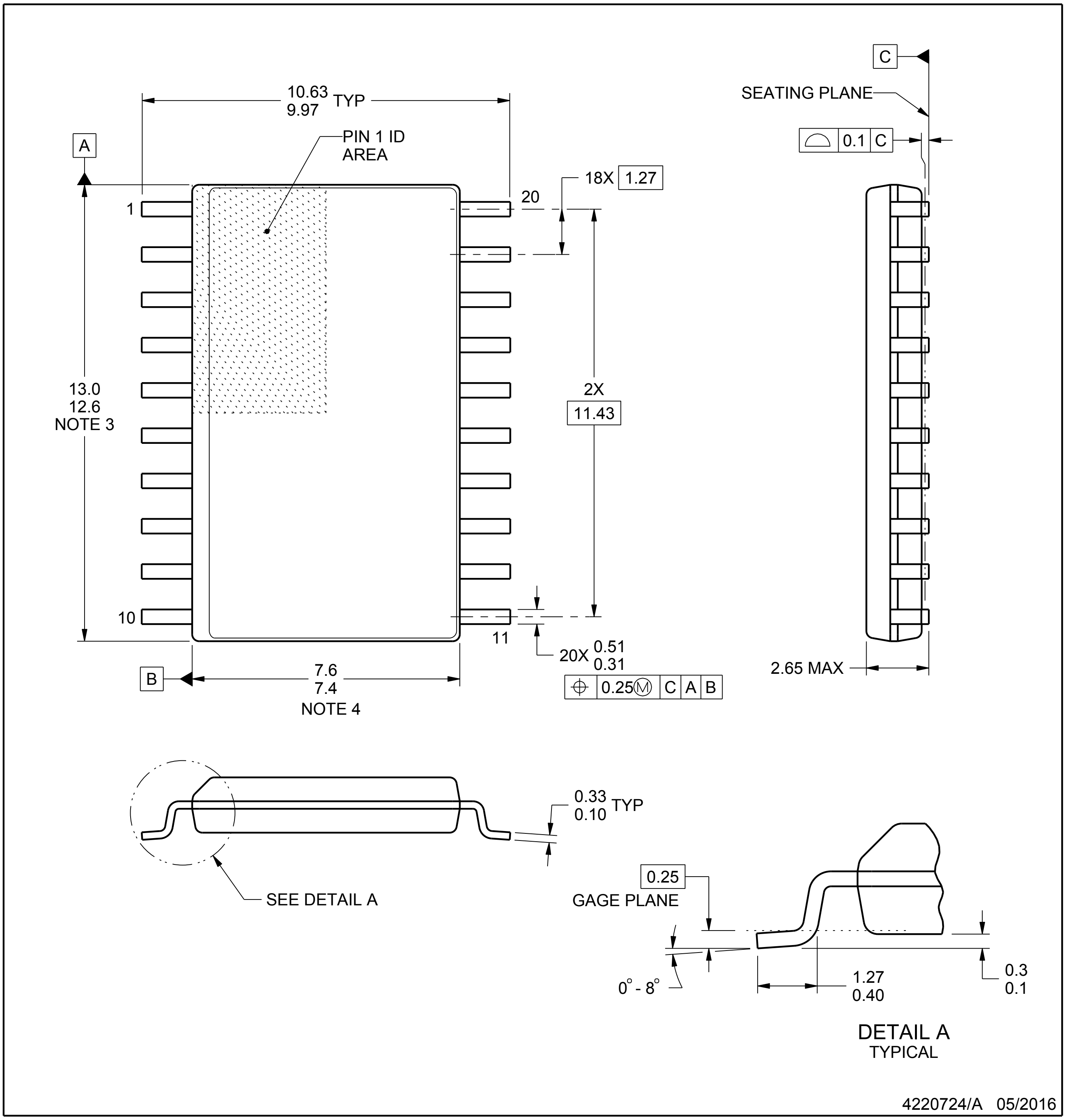
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

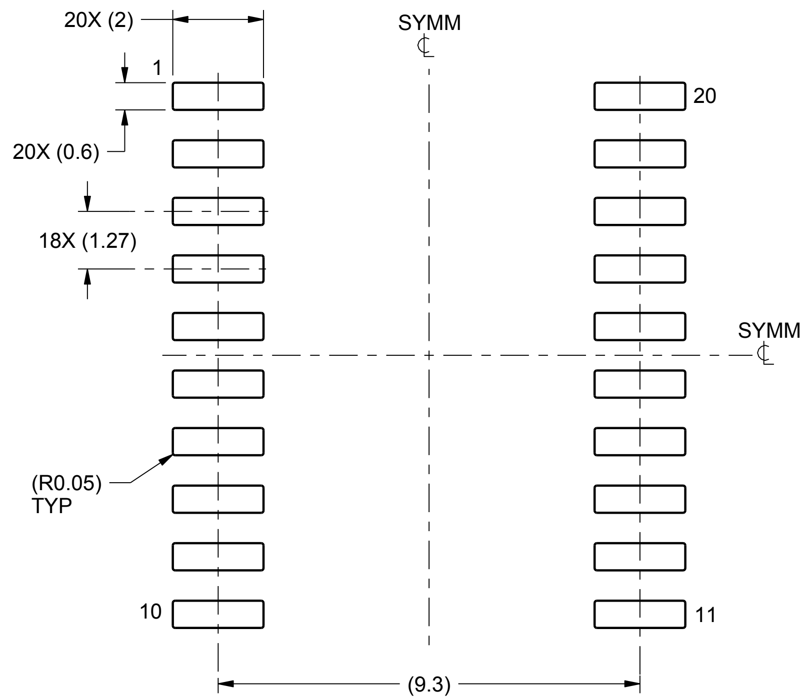
SOIC - 2.65 mm max height

SOIC

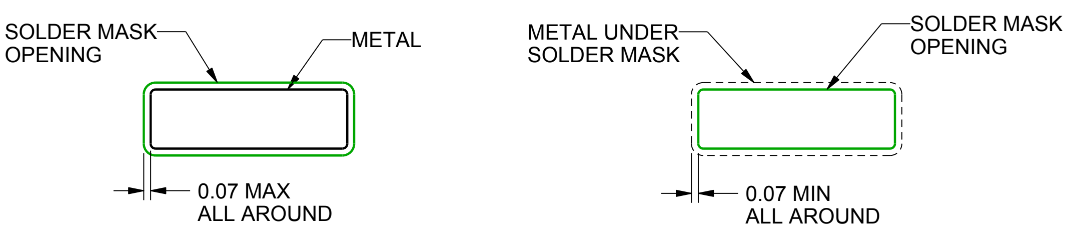


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

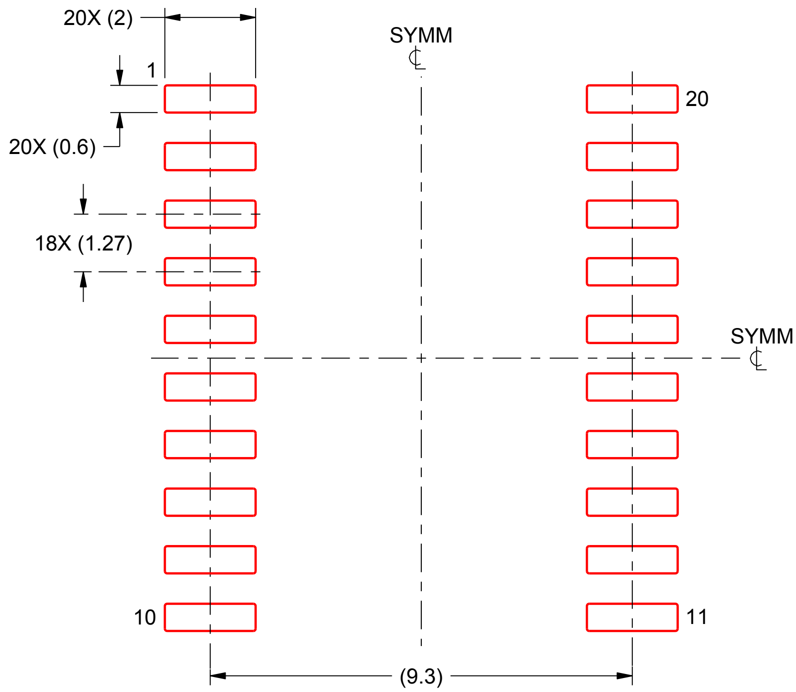
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.