SNx5LBC180A Low-Power Differential Line Driver and Receiver Pairs

1 Features

- High-speed low-power LinBICMOS™ circuitry designed for signaling rates(1) of up to 30 Mbps
- Bus-Pin ESD protection 15 kV HBM
- Low disabled supply-current requirements: 700 µA maximum
- Designed for high-speed multipoint data transmission over long cables
- Common-mode voltage range of –7 V to 12 V
- Low supply current: 15 mA Max
- Compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E)
- Positive and negative output current limiting
- Driver thermal shutdown protection [1]

2 Description

The SN65LBC180A and SN75LBC180A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

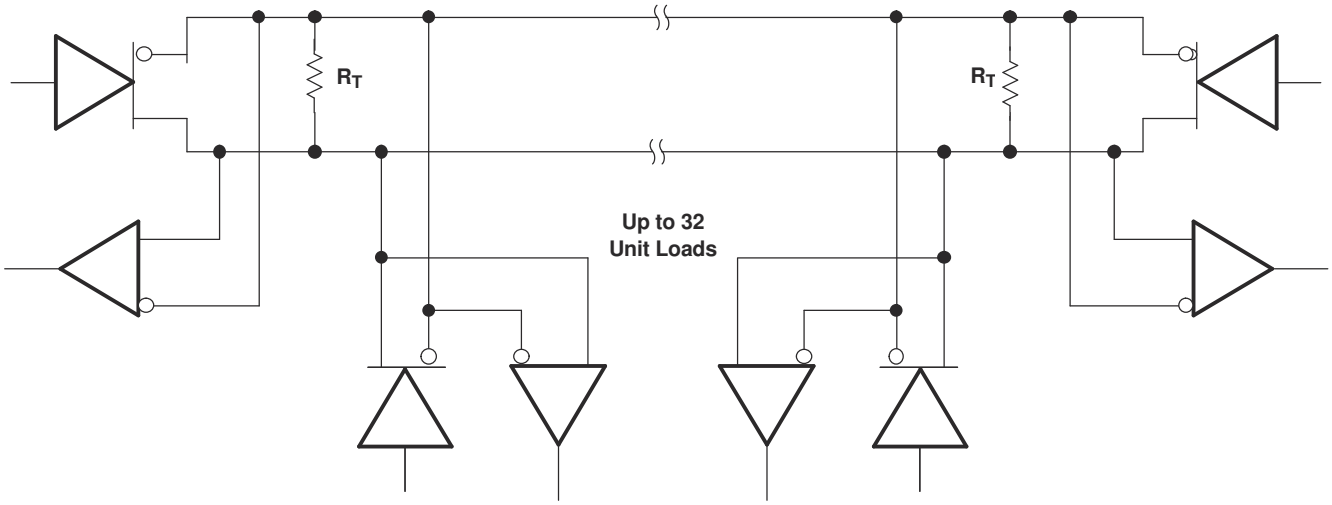
These devices combine a differential line driver and differential input line receiver and operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off (V_{CC} = 0). These parts feature wide positive and negative common-mode voltage ranges, making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive and negative current limiting for protection from line fault conditions. The SN65LBC180A is characterized for operation from –40°C to 85°C, and the SN75LBC180A is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN65LBC180ASN75 LBC180A	D (SOIC)	4.9 mm x 3.91 mm
	N (PDIP)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN65LBC180A
SN75LBC180A



Typical Application

[1] Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved without this requirement as displayed in the *Typical Characteristics* of this device.

3 Revision History

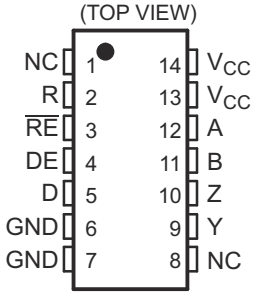
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2009) to Revision E (January 2023)	Page
• Changed the document to the latest TI format	1
• Added the *Pin Configuration and Functions*	3
• Added the *Thermal Information* table	5
• Changed the Typical Characteristics graphs	7

Changes from Revision C (June 2002) to Revision D (April 2009)	Page
• Deleted exceeds from features, and changed 12 kV To 15 kV	1
• Deleted storage temperature and lead temperature from the absolute maximum ratings table	4
• Added receiver output current to the absolute maximum ratings table	4
• Changed the ESD rows in the absolute maximum ratings table	4

4 Pin Configuration and Functions

SN65LBC180AD (Marked as BL180A)
SN65LBC180AN (Marked as 65LBC180A)
SN75LBC180AD (Marked as LB180A)
SN75LBC180AN (Marked as 75LBC180A)
(TOP VIEW)



NC – No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1, 8	No Connect	Not electrically connected
R	2	Digital Output	Logic output RS485 data
$\overline{RE}$	3	Digital Input	Receiver enable, active low
DE	4	Digital Input	Driver enable, active high
D	5	Digital Input	Driver data input
GND	6, 7	Ground	Device ground
Y	9	Bus Output	Bus Output Y (Complementary to Z)
Z	10	Bus Output	Bus Output Z (Complementary to Y)
B	11	Bus Input	Bus Input B (Complementary to A)
A	12	Bus Input	Bus Input A (Complementary to B)
V_{CC}	13, 14	Power	5 V Supply

5 Reference

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			UNIT
V_{CC}	Supply voltage range(2)		–0.3 V to 6 V
V_I	Input voltage range	A, B	–10 V to 15 V
	Voltage range	D, R, DE, $\overline{RE}$	–0.3 V to V_{CC} + 0.5 V
I_O	Receiver output current		±10 mA
	Continuous total power dissipation(3)		Internally limited
	Total power dissipation		See Dissipation Rating Table
ESD	Bus terminals and GND	HBM (Human Body Model) EIA/JESD22-A114(4)	±15 kV
	All pins	HBM (Human Body Model) EIA/JESD22-A114(4)	±3 kV
		MM (Machine Model) EIA/JESD22-A115	±400 V
		CDM (Charge Device Model) EIA/JESD22-C101	±1.5 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND except for differential input or output voltages.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(4) Tested in accordance with MIL-STD-883C, Method 3015.7.

5.2 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$	0		0.8	V
V_{ID}	Differential input voltage(1)		–12(2)		12	V
V_O, V_I, V_{IC}	Voltage at any bus terminal (separately or common mode)	A, B, Y, or Z	–7		12	V
I_{OH}	High-level output current	Y or Z	–60			mA
		R	–8			
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_A	Operating free-air temperature	SN65LBC180A	–40		85	°C
		SN75LBC180A	0		70	

(1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
(2) The algebraic convention, where the least positive (more negative) limit is designated minimum, is used in this data sheet.

5.4 Thermal Information

THERMAL METRIC[1]		N (PDIP)	D (SOIC) SN75 Devices	D (SOIC) SN65 Devices	UNIT
		14-Pins	14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.2	88.6	93.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	49.12	49.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.0	14.17	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.1	48.6	48.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 54 Ω, See Figure 6-1	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
		R_L = 60 Ω, See Figure 6-2	SN65LBC180A	1	1.5	3	V
			SN75LBC180A	1.1	1.5	3	
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage[2]	See Figure 6-1 and Figure 6-2		–0.2		0.2	V
$V_{OC(ss)}$	Steady-state common-mode output voltage	See Figure 6-1		1.8	2.4	2.8	V
ΔV_{OC}	Change in steady-state common-mode output voltage[2]			–0.1		0.1	V
I_O	Output current with power off	V_{CC} = 0 ,	V_O = –7 V to 12 V	–10		10	µA
I_{IH}	High-level input current	V_I = 2 V		–100			µA
I_{IL}	Low-level input current	V_I = 0.8 V		–100			µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V		–250	±70	250	mA
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled		5.5	9	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) Δ | V_{OD} | and Δ | V_{OC} | are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 6-3	2	6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		2	6	12	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			0.3	1	ns
t_r	Differential output signal rise time		4	7.5	11	ns
t_f	Differential output signal fall time		4	7.5	11	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, See Figure 6-4		12	22	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, See Figure 6-5		12	22	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	R_L = 110 Ω, See Figure 6-4		12	22	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	R_L = 110 Ω, See Figure 6-5		12	22	ns

5.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} - V_{IT-}$)				50		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		–1.5	–0.8		V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA		4	4.9		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA			0.1	0.8	V
I_{OZ}	High-impedance-state output current	V_O = 0 V to V_{CC}		–1		1	µA
I_{IH}	High-level enable-input current	V_{IH} = 2.4 V		–100			µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V		–100			µA
I_I	Bus input current	V_I = 12 V, V_{CC} = 5 V	Other input at 0 V		0.4	1	mA
		V_I = 12 V, V_{CC} = 0			0.5	1	
		V_I = –7 V, V_{CC} = 5 V		–0.8	–0.4		
		V_I = –7 V, V_{CC} = 0		–0.8	–0.3		
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled		4.5	7.5	mA
			Receiver disabled and driver disabled		0.5	1	
			Receiver enabled and driver enabled		8.5	15	

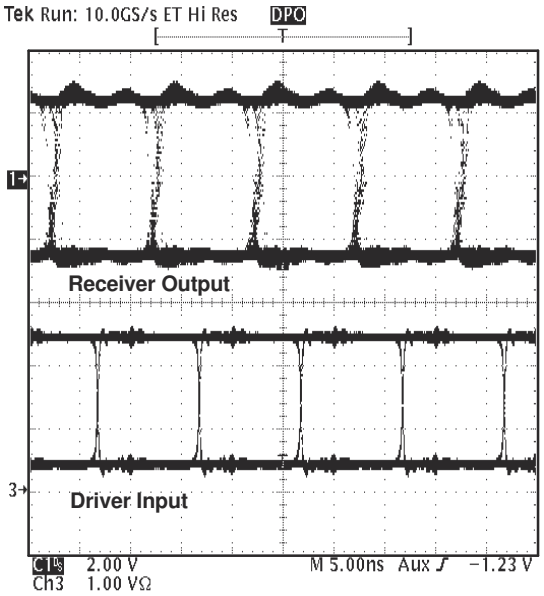
(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 6-7	7	13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output		7	13	20	ns
$t_{sk(p)}$	Pulse skew (| t_{PHL} – t_{PLH} |)			0.5	1.5	ns
t_r	Output signal rise time			2.1	3.3	ns
t_f	Output signal fall time	See Figure 6-7		2.1	3.3	ns
t_{PZH}	Output enable time to high level	C_L = 10 pF, See Figure 6-8		30	45	ns
t_{PZL}	Output enable time to low level			30	45	ns
t_{PHZ}	Output disable time from high level			20	40	ns
t_{PLZ}	Output disable time from low level			20	40	ns

Typical Characteristics



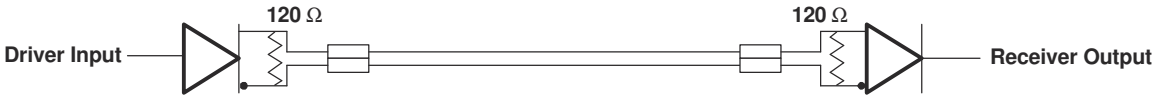


Figure 5-1. Typical Waveform of Nonreturn-to-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

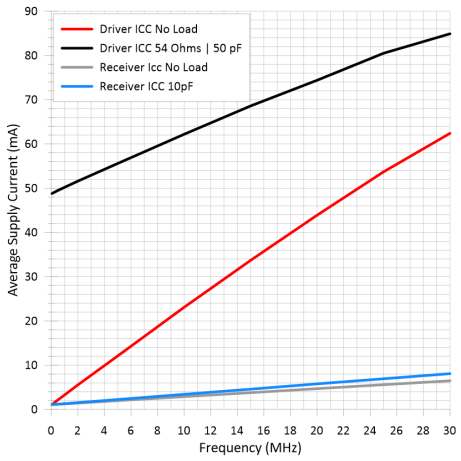


Figure 5-2. Average Supply Current vs Frequency

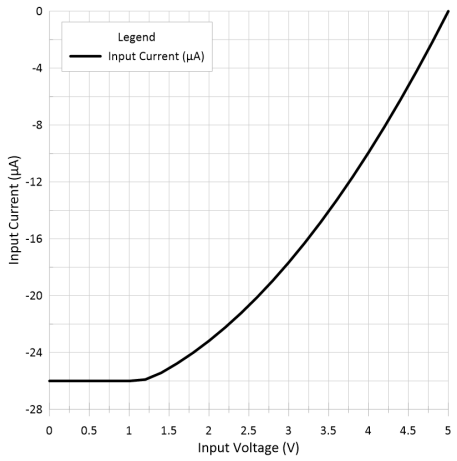


Figure 5-3. Logic Input Current vs Input Voltage

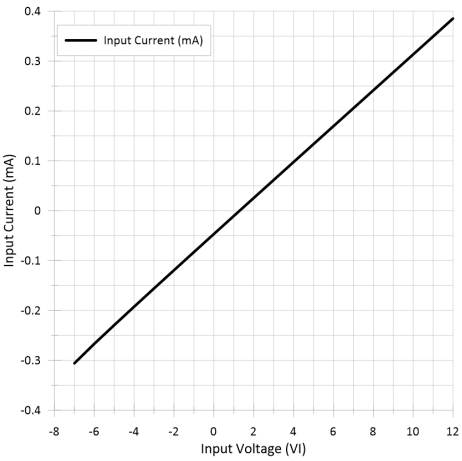


Figure 5-4. Bus Input Current vs Input Voltage

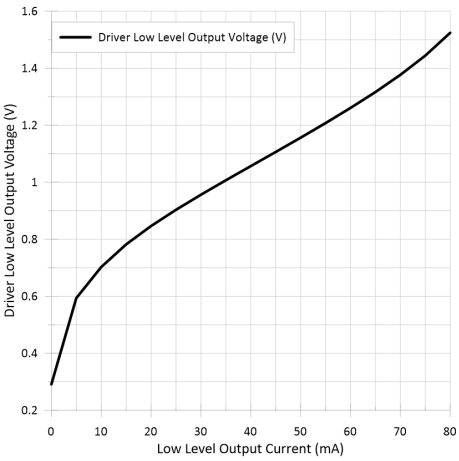


Figure 5-5. Driver Low-Level Output Voltage vs Low-Level Output Current

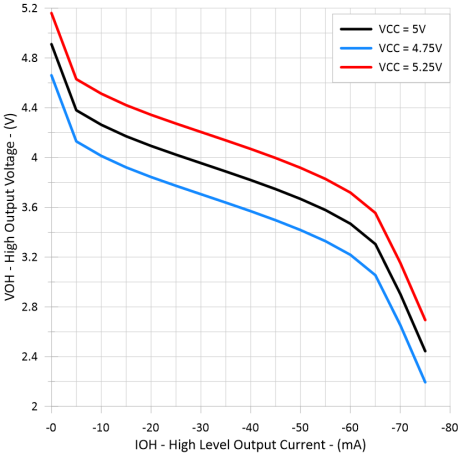


Figure 5-6. Driver High-Level Output Voltage vs High-Level Output Current

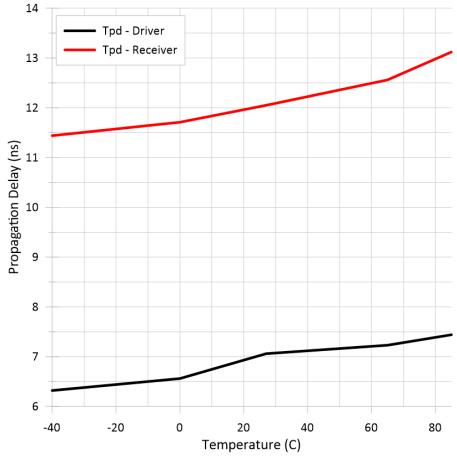


Figure 5-7. Propagation Delay Time vs Case Temperature

Parameter Measurement Information

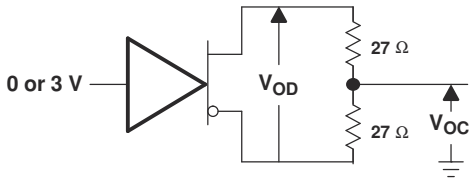


Figure 6-1. Driver V_{OD} and V_{OC}

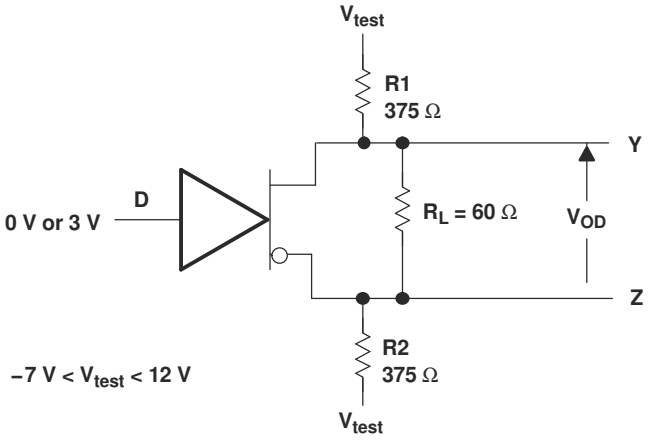
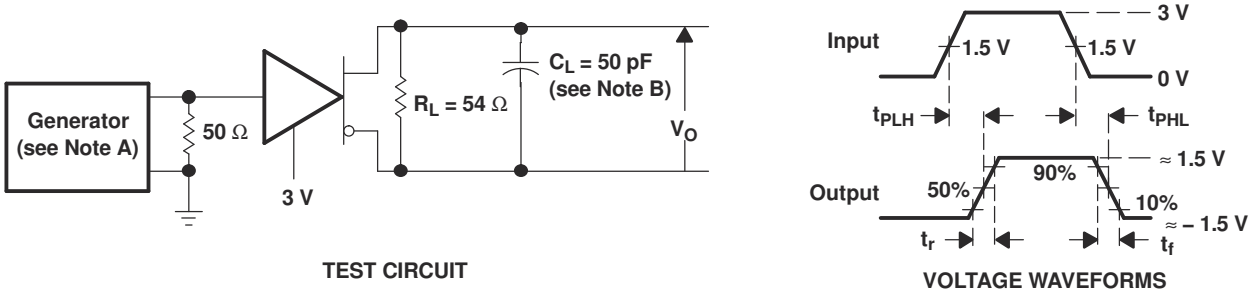


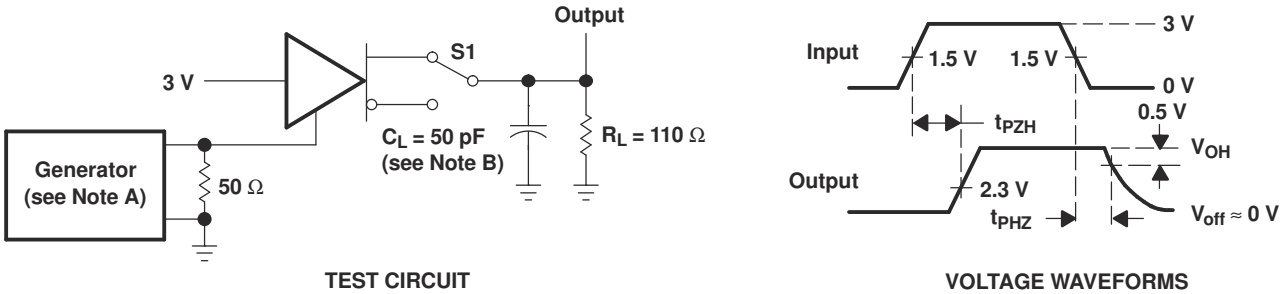
Figure 6-2. Driver V_{OD}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

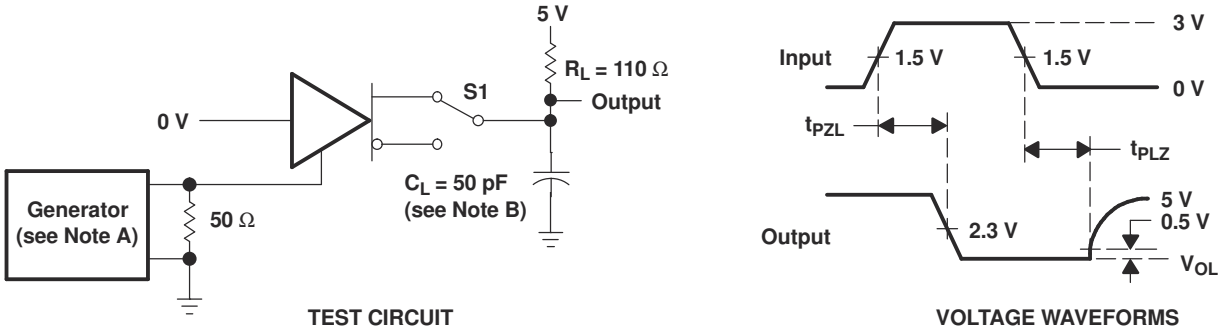
Figure 6-3. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-4. Driver Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-5. Driver Test Circuit and Voltage Waveforms

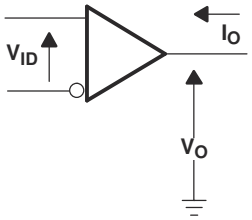
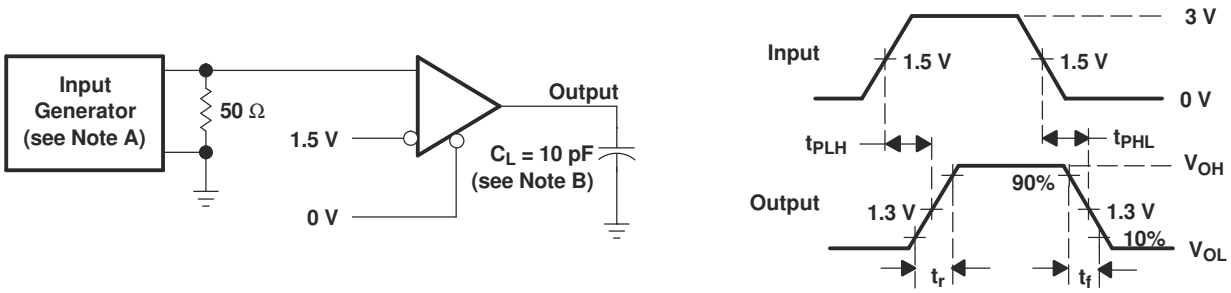


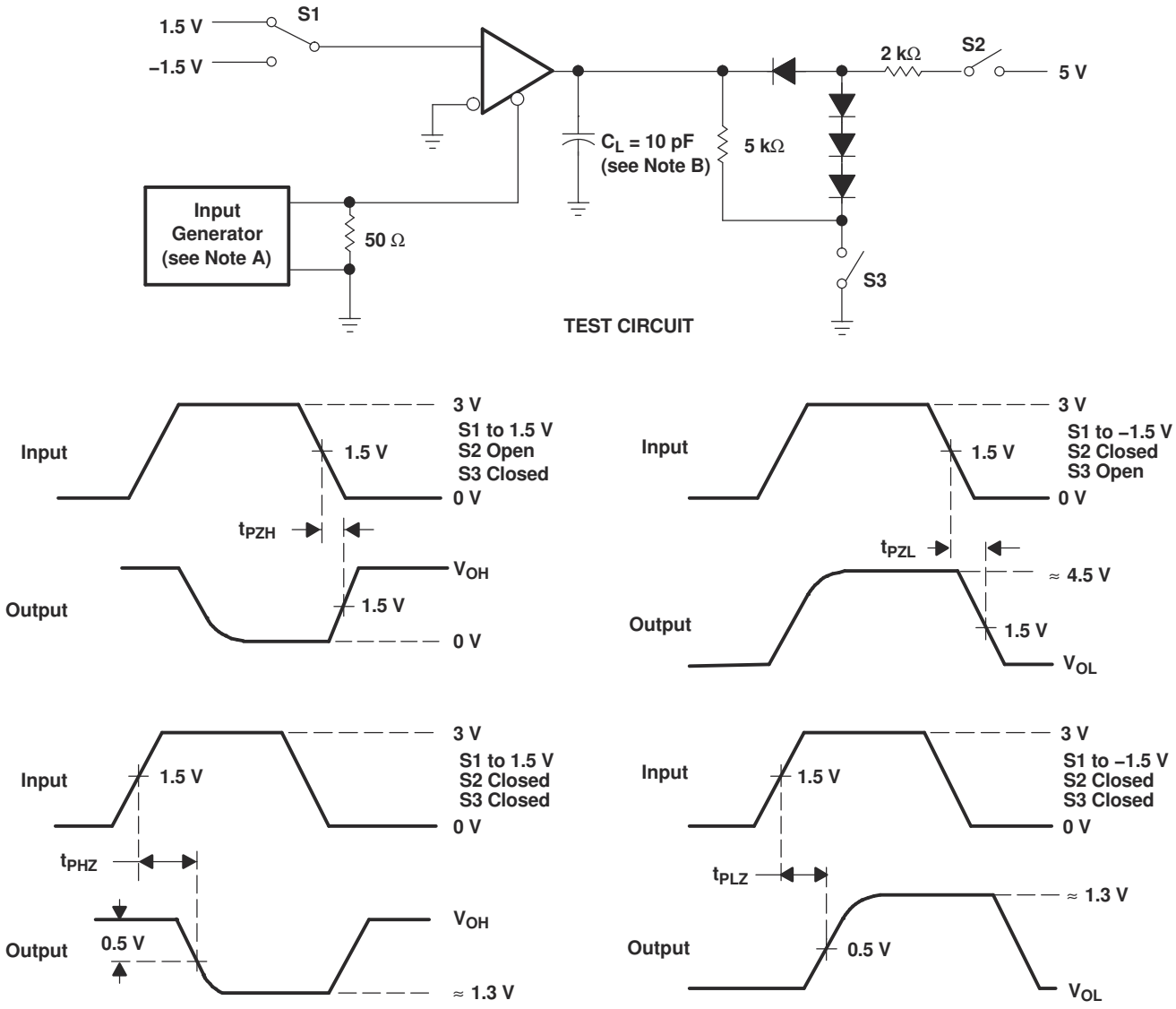
Figure 6-6. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-7. Receiver Test Circuit and Voltage Waveforms



VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-8. Receiver Output Enable and Disable Times

6 Detailed Description

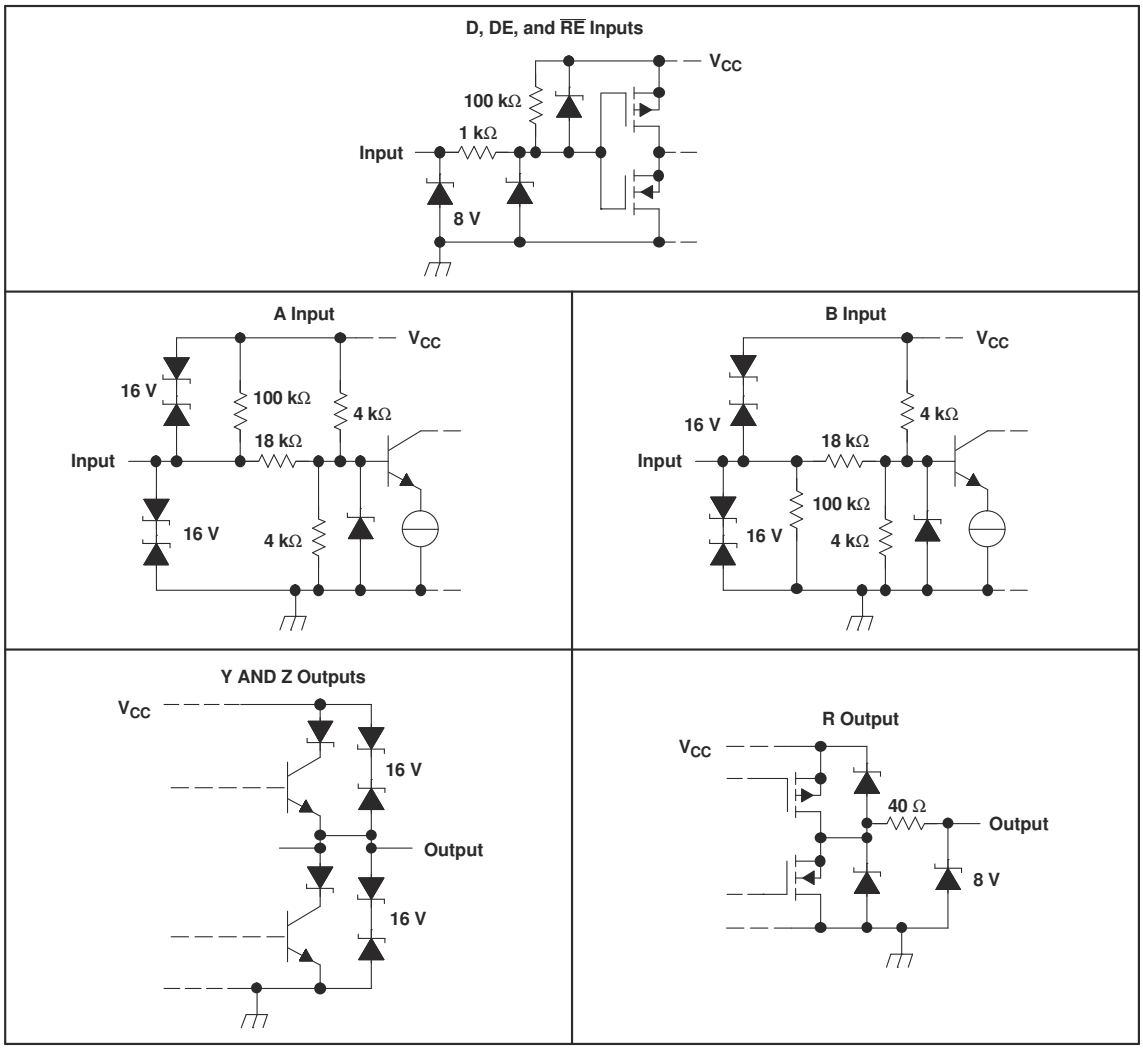
6.1 Device Functional Modes

6.1.1 Functional Tables

DRIVER[1]				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS		DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
		Y	Z			
H	H	H	L	$V_{ID} \geq 0.2$ V	L	H
L	H	L	H	-0.2 V < V_{ID} < 0.2 V	L	?
X	L	Z	Z	$V_{ID} \leq -0.2$ V	L	L
OPEN	H	H	L	X	H	Z
				Open circuit	L	H

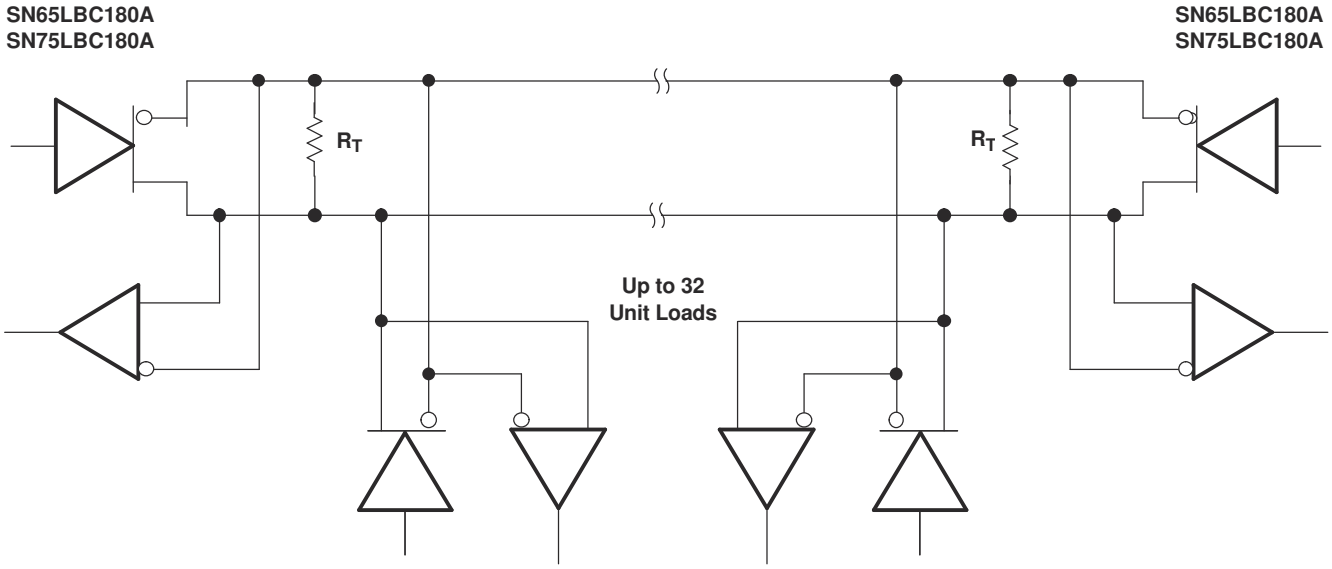
(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

6.1.2 Schematics of Inputs and Outputs



7 Application Information

7.1 Typical Application Circuit



A. The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible. One SN65LBC180A typically represents less than one unit load.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

LinBICMOS™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC180AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	BL180A
SN65LBC180ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180A
SN65LBC180ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180A
SN65LBC180ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180A
SN65LBC180ADRG4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL180A
SN65LBC180AN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC180A
SN65LBC180AN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65LBC180A
SN75LBC180AD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	LB180A
SN75LBC180AN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC180A
SN75LBC180AN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75LBC180A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

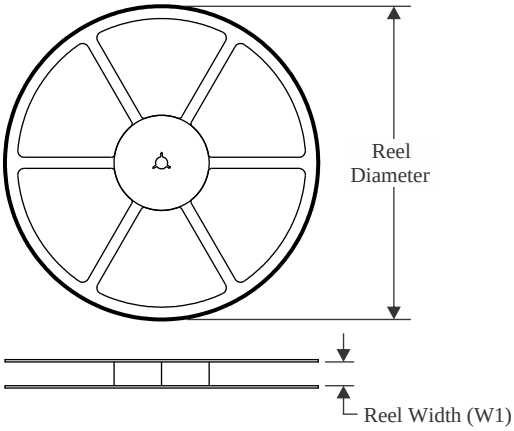
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

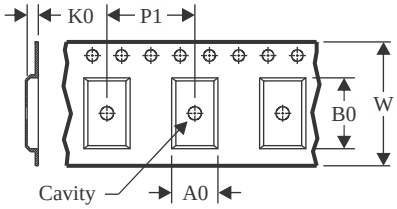
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

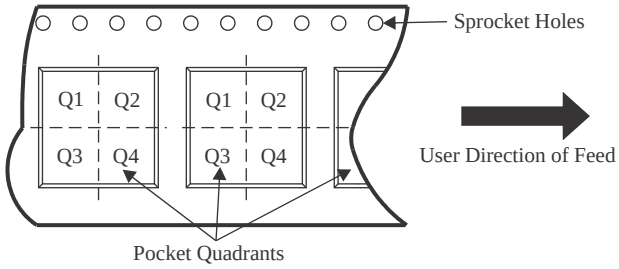


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

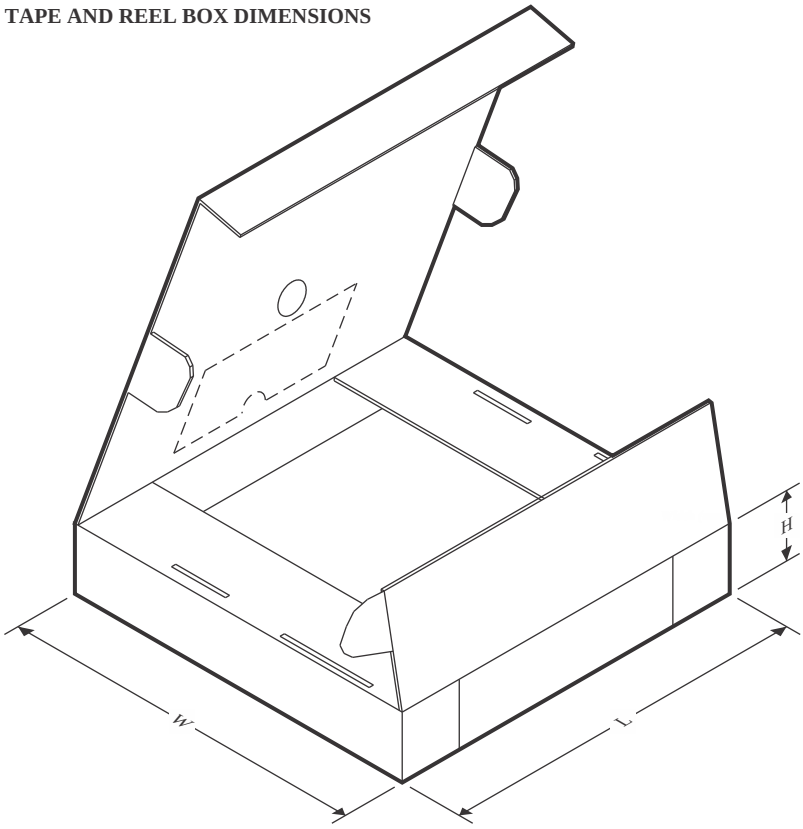
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC180ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LBC180ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

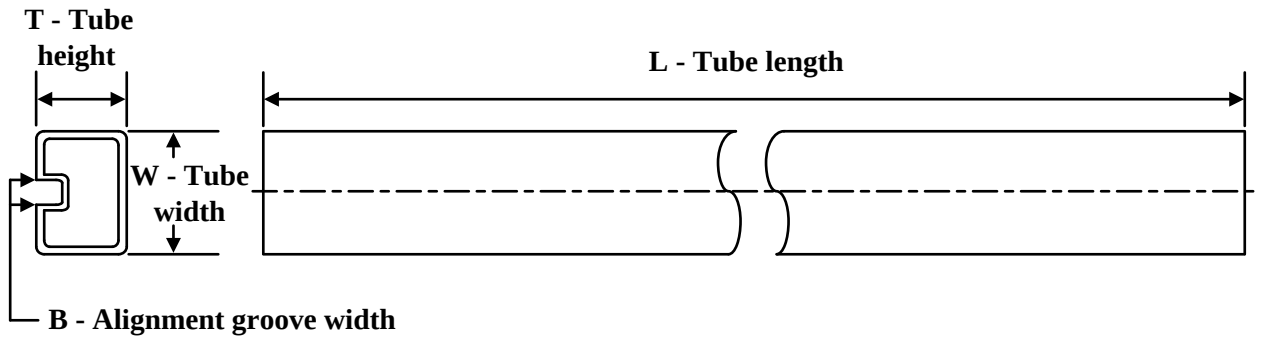
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

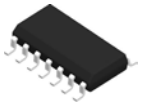
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC180ADR	SOIC	D	14	2500	340.5	336.1	32.0
SN65LBC180ADRG4	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC180AN	N	PDIP	14	25	506	13.97	11230	4.32
SN65LBC180AN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180AN	N	PDIP	14	25	506	13.97	11230	4.32
SN75LBC180AN.A	N	PDIP	14	25	506	13.97	11230	4.32

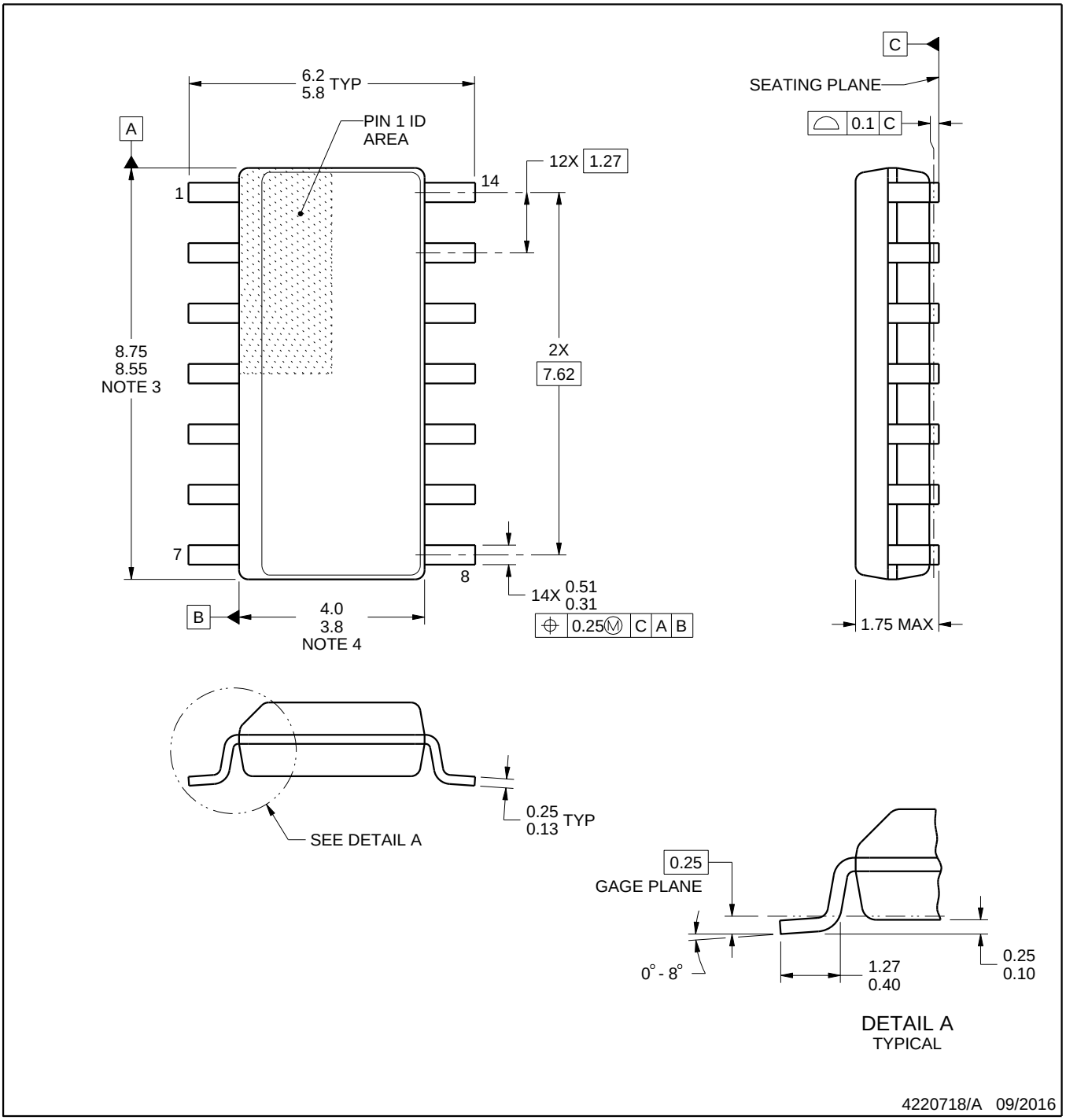


PACKAGE OUTLINE

D0014A

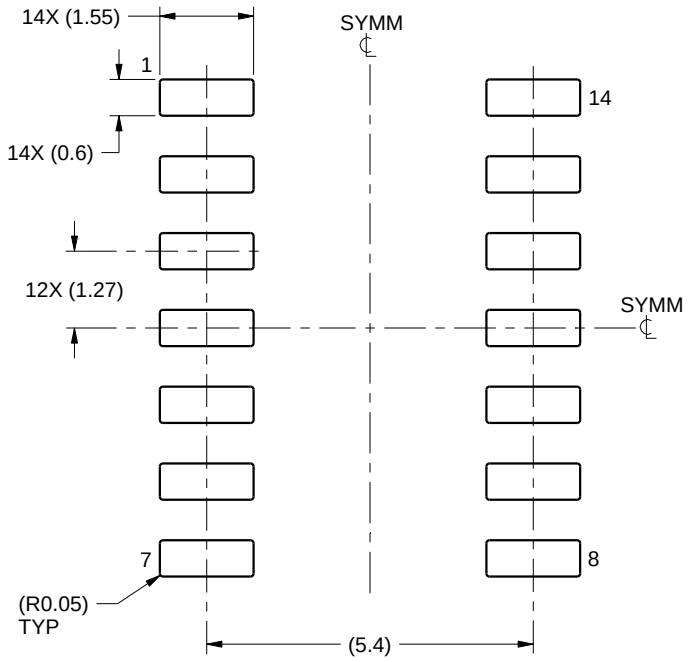
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

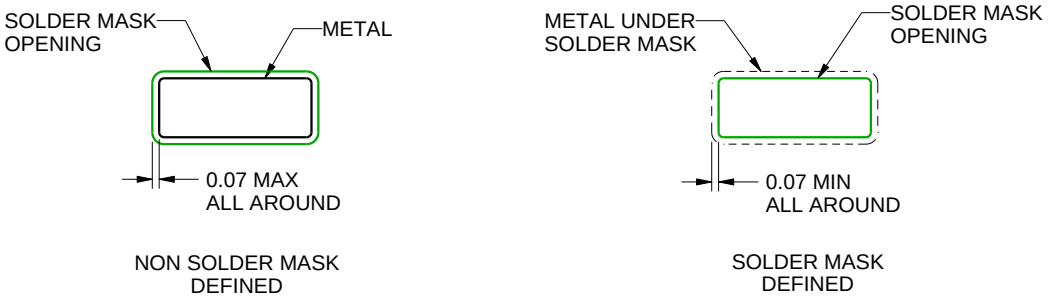


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

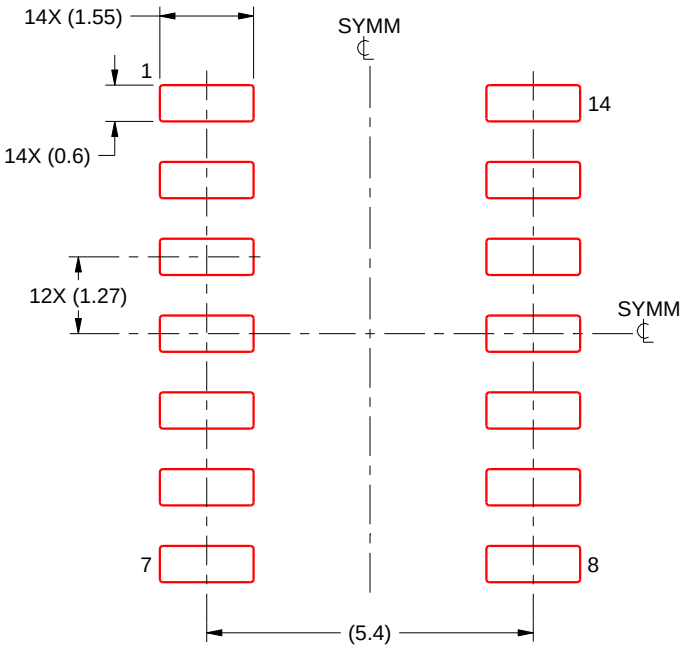
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

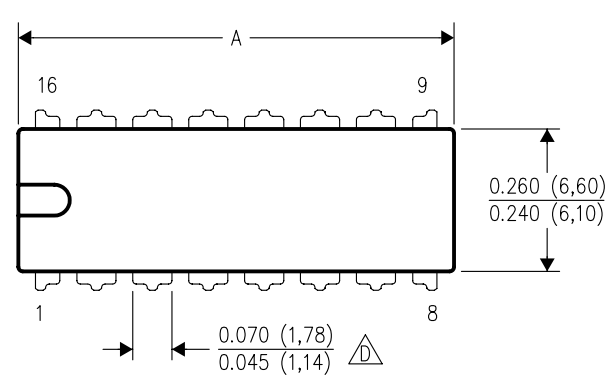
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

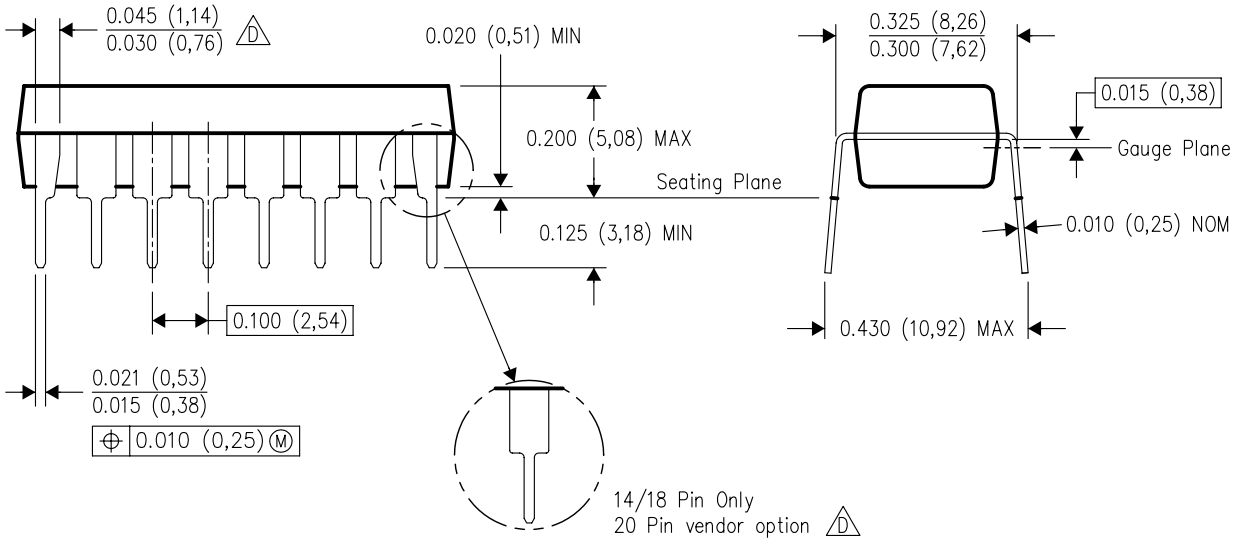
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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