Gigabit 4 × 4 CROSSPOINT SWITCH

FEATURES

- **Up to 2.5-Gbps Operation**
- **Non-Blocking Architecture Allows Each Output to Be Connected to Any Input**
- **30 ps of Deterministic Jitter**
- **Selectable Transmit Preemphasis Per Lane**
- **Selectable Receive Equalization**
- **Available Packaging: 48-Pin QFN**
- **Propagation Delay Times: 500 ps Typical**
- **Inputs Electrically Compatible With CML Signal Levels**
- **Operates From a Single 3.3-V Supply**
- **Ability to Place Ouputs in High-Impedance State**
- **Low Power: 560 mW**
- **Integrated Termination Resistors**

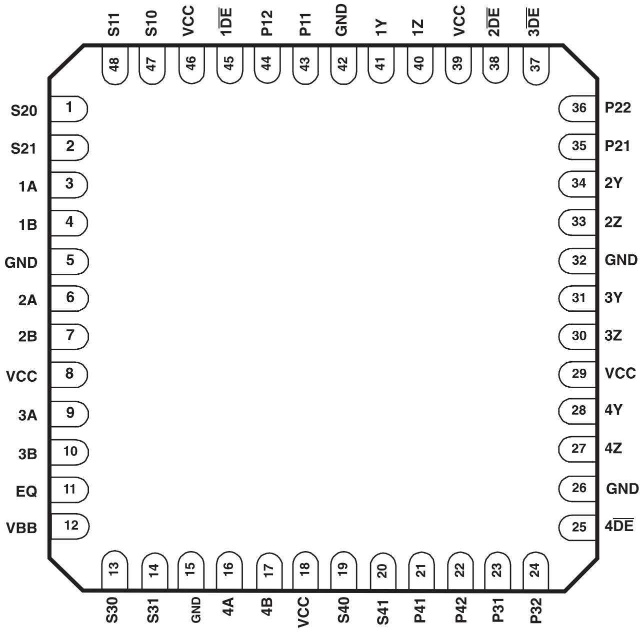
APPLICATIONS

- **Clock Buffering/Clock MUXing**
- **Wireless Base Stations**
- **High-Speed Network Routing**
- **Telecom/Datacom**

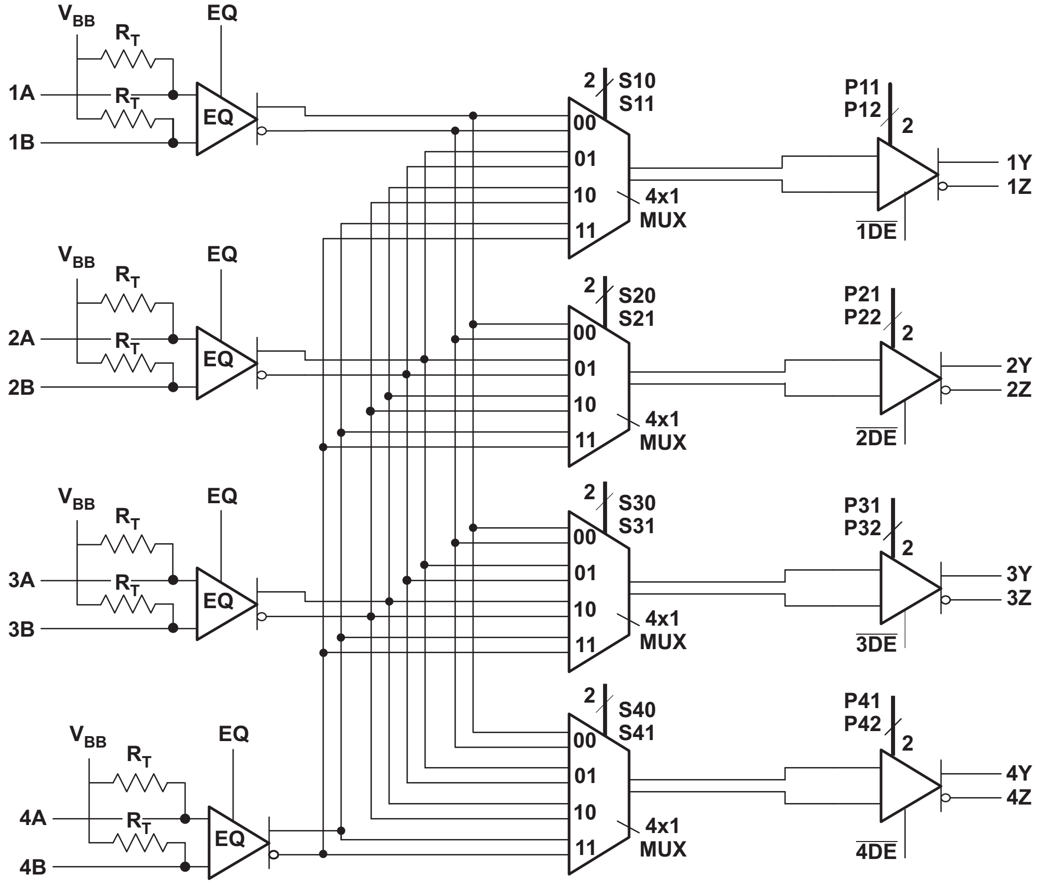
DESCRIPTION

The SN65LVCP204 is a 4×4 non-blocking crosspoint switch in a flow-through pinout that allows for ease in PCB layout. VML signaling is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve high signaling speeds while maintaining low signal skews. The SN65LVCP204 incorporates 100-Ω termination resistors for those applications where board space is at a premium. Transmit preemphasis and receive equalization are built in for superior signal integrity performance.

The SN65LVCP204 is characterized for operation from –40°C to 85°C.



LOGIC DIAGRAM



Note:

V_{BB}: Receiver input internal biasing voltage (allows ac coupling)

EQ: Input equalizer (compensates for frequency dependent transmission line loss of backplanes)

R_T: Internal 50-Ω receiver termination (100-Ω differential)

Preemphasis: Output precompensation for transmission line losses

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
High Speed I/O			
xA xB	3, 6, 9, 16 4, 7, 10, 17	Differential inputs (with 50-Ω termination to V_{BB}) xA = P; xB = N	Line-side differential inputs, CML compatible
xY xZ	41, 34, 31, 28 40, 33, 30, 27	Differential output xY = P; xZ = N	Switch-side differential outputs, VML
Control Signals			
x$\overline{\text{DE}}$	45, 38, 37, 25	Input	Data enable; active low; LVTTL; when not enabled, the ouput is in the high-impedance state for power savings.
S10–S41	47, 48, 1, 2, 13, 14, 19, 20	Input; S1x = channel 1, bit x	Switching selection; LVTTL

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	**NO.**		
P11–P42	43, 44, 35, 36, 23, 24, 21, 22	Input; P1x = channel 1, bit x	Output preemphasis control; LVTTL
EQ	11	Input; selection for receive equalization setting	EQ = 1 (default) is for the 5-dB setting, EQ = 0 is for the 12-dB setting
Power Supply			
VCC	8, 18, 29, 39, 46	Power	Power supply 3.3 V ±5%
GND	5, 15, 26, 32, 42		Ground
Thermal pad			The ground center pad of the package must be connected to GND plane.
V_{BB}	12	Input	Receiver input biasing voltage

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

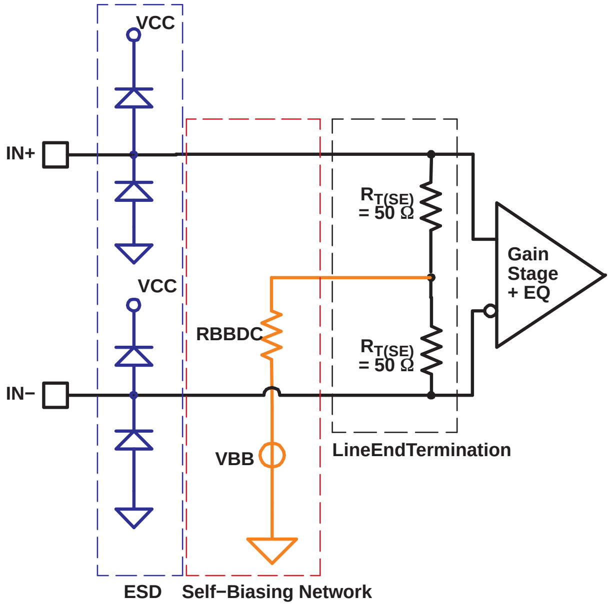


Figure 1. Equivalent Input Circuit Design

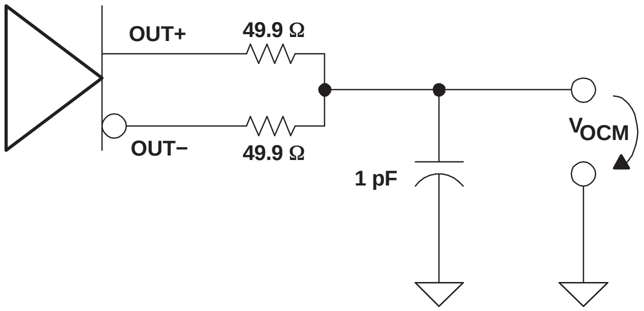


Figure 2. Common-Mode Output Voltage Test Circuit

Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	**S11**	**1Y/1Z**	**S20**	**S21**	**2Y/2Z**	**S30**	**S31**	**3Y/3Z**	**S40**	**S41**	**4Y/4Z**
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGED DEVICE(1)
		RGZ (48-Pin) (Orderable)
–40°C to 85°C	Serial multiplexer	SN65LVCP204RGZ

(1) The package is available taped and reeled. Add an R suffix to device types (e.g., SN65LVCP204RGZR).

PACKAGE THERMAL CHARACTERISTICS

PACKAGE THERMAL CHARACTERISTICS(1)		NOM	UNIT
θ_{JA} (junction-to-ambient)	Four-layer JEDEC board (JESD51-7) using eight GND-vias of 0.3-mm diameter on the center pad as shown in the section: *Recommended PCB footprint* with boundary and environment conditions of JEDEC board (JESD51-2)	33	°C/W
θ_{JB} (junction-to-board)		20	°C/W
θ_{JC} (junction-to-case)		23.6	°C/W
Ψ-jt (junction-to-top pseudo)		0.6	°C/W
Ψ-jb (junction-to-board pseudo)		19.4	°C/W
θ_{JP} (junction-to-pad)		5.4	°C/W

(1) See the *IC Package Thermal Metrics* application report SPRA953 for a detailed explanation of thermal parameters.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

				UNIT
V_{CC}	Supply-voltage range(2)			–0.5 V to 6 V
	Voltage range		Control inputs, all outputs	–0.5 V to (V_{CC} + 0.5 V)
			Receiver inputs	–0.5 V to 4 V
	ESD	Human-body model(3)	All pins	3 kV
		Charged-device model(4)	All pins	500 V
T_J	Maximum junction temperature			See *Package Thermal Characteristics* table
	Moisture sensitivity level			2
	Reflow temperature package soldering, 4 seconds			260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to the ground terminals.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
dR	Operating data rate				2.5	Gbps
V_{CC}	Supply voltage		3.135	3.3	3.465	V
$V_{CC(N)}$	Supply-voltage noise amplitude	10 Hz to 1.25 GHz			20	mV
T_J	Junction temperature				125	°C
T_A	Operating free-air temperature (1)		–40		85	°C
DIFFERENTIAL INPUTS						
V_{ID}	Receiver peak-to-peak differential input voltage (2)	$dR_{(in)} \leq 1.25$ Gbps	100		1750	mV_{PP}
		$1.25\text{ Gbps} < dR_{(in)} \leq 2.5$ Gbps	100		1560	mV_{PP}
		$dR_{(in)} > 2.5$ Gbps	100		1000	mV_{PP}
V_{ICM}	Receiver common-mode input voltage	Note: for best jitter performance, ac coupling is recommended.	1.5	1.6	$V_{CC} - \frac{\|V_{ID}\|}{2}$	V
CONTROL INPUTS						
V_{IH}	High-level input voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
DIFFERENTIAL OUTPUTS						
R_L	Differential load resistance		80	100	120	Ω

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.
(2) Differential input voltage V_{ID} is defined as | IN+ – IN– |.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DIFFERENTIAL INPUTS						
V_{IT+}	Positive-going differential input, high threshold				50	mV
V_{IT-}	Negative-going differential input, low threshold		–50			mV
$A_{(EQ)}$	Equalizer gain	at 1.25 GHz (EQ = 0)		12		dB
$R_{T(D)}$	Termination resistance, differential		80	100	120	Ω
V_{BB}	Open-circuit input voltage (input self-bias voltage)	AC-coupled inputs		1.6		V
$R_{(BBDC)}$	Biasing network dc impedance			30		kΩ
$R_{(BBAC)}$	Biasing network ac impedance	375 MHz		42		Ω
DIFFERENTIAL OUTPUTS						
V_{ODH}	High-level output voltage	$R_L = 100\ \Omega \pm 1\%$, Px2 = Px1 = 0; 2.5 Gbps alternating 1010-pattern; Figure 3		650		mV_{PP}
V_{ODL}	Low-level output voltage			–650		mV_{PP}
$V_{ODB(PP)}$	Output differential voltage without preemphasis (2)		1000	1300	1500	mV_{PP}
V_{OCM}	Output common-mode voltage	See Figure 2		1.65		V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			1		mV

(1) All typical values are at $T_A = 25°C$ and $V_{CC} = 3.3$-V supply unless otherwise noted. They are for reference purposes and are not production tested.
(2) Differential output voltage $V_{(ODB)}$ is defined as | OUT+ – OUT– |.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
$V_{(PE)}$	Output preemphasis voltage ratio, $\frac{V_{ODB(PP)}}{V_{ODPE(PP)}}$	R_L = 100 Ω±1%; x = L or S; See Figure 3	Px2:Px1 = 00		0		dB
			Px2:Px1 = 01		3		
			Px2:Px1 = 10		6		
			Px2:Px1 = 11		9		
$t_{(PRE)}$	Preemphasis duration measurement	Output preemphasis is set to 9 dB during test; Pxx = 1; Measured with a 100-MHz clock signal; R_L = 100 Ω ±1%, See Figure 4			175		ps
R_O	Output resistance	Differential on-chip termination between OUT+ and OUT–			100		Ω
CONTROL INPUTS							
I_{IH}	High-level input current	V_{IN} = VCC				5	µA
I_{IL}	Low-level input current	V_{IN} = GND		–125	–90		µA
$R_{(PU)}$	Pullup resistance				35		kΩ
POWER CONSUMPTION							
P_D	Device power dissipation	All outputs terminated 100 Ω			560	750	mW
P_Z	Device power dissipation in high-impedance state	All outputs in high-impedance state				600	mW
I_{CC}	Device current consumption	All outputs terminated 100 Ω PRBS 2^7 – 1 pattern at 2.5 Gbps				220	mA

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
MULTIPLEXER						
$t_{(SM)}$	Multiplexer switch time	Multiplexer to valid output		3	6	ns
DIFFERENTIAL OUTPUTS						
t_{PLH}	Low-to-high propagation delay	Propagation delay, input to output See Figure 6		0.5	0.7	ns
t_{PHL}	High-to-low propagation delay			0.5	0.7	ns
t_r	Rise time	20% to 80% of $V_{O(DB)}$; test pattern: 100-MHz clock signal; see Figure 5 and Figure 8		110		ps
t_f	Fall time			110		ps
$t_{sk(p)}$	Pulse skew, $\mid t_{PHL} - t_{PLH} \mid$(2)				20	ps
$t_{sk(o)}$	Output skew(3)	All outputs terminated with 100 Ω		25	100	ps
$t_{sk(pp)}$	Part-to-part skew(4)				300	ps
t_{zd}	Switch time, hi-Z state to disable	50 Ω to Vcm and 150-pF load on each output			20	ns
t_{ze}	Switch time, hi-Z state to enable	50 Ω to Vcm and 150-pF load on each output			10	ns
RJ	Device random jitter, rms	See Figure 8 for test circuit. BERT setting 10^{-15} Alternating 10-pattern.		0.8	2	ps-rms

(1) All typical values are at 25°C and with 3.3-V supply, unless otherwise noted.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any two outputs of a single device.
(4) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

SWITCHING CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
DJ	Intrinsic deterministic device jitter [5][6], peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS $2^7 - 1$ pattern	2.5 Gbps			30	ps
	Absolute deterministic output jitter[7], peak-to-peak	0 dB preemphasis (PREx_x = 0); See Figure 8 for the test circuit.	PRBS $2^7 - 1$ pattern	1.25 Gbps; EQ = 1 Over 25-inch (63,5-cm) FR4 trace		7		ps

(5) Intrinsic deterministic device jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation ($DJ_{(OUT)} - DJ_{(IN)}$), where $DJ_{(OUT)}$ is the total peak-to-peak deterministic jitter measured at the output of the device in PSPP. $DJ_{(IN)}$ is the peak-to-peak deterministic jitter of the pattern generator driving the device.

(6) The SN65LVCP204 built-in passive input equalizer compensates for ISI. For a 25-inch (63,5-cm) FR4 transmission line with 8-mil (0,2-mm) trace width, the SN65LVCP204 typically reduces jitter by 60 ps from the device input to the device output.

(7) Absolute deterministic output jitter reflects the deterministic jitter measured at the SN65LVCP204 output. The value is a real value measured with a bit-error tester as described in Figure 8. The absolute DJ reflects the sum of all deterministic jitter components accumulated over the link: $DJ_{(absolute)} = DJ_{(Signal\ generator)} + DJ_{(transmission\ line)} + DJ_{(intrinsic(LVCP204))}$.

Table 2. Preemphasis Controls PL2, PL1, PS2, and PS1

Px2[1]	Px1[1]	OUTPUT PREEMPHASIS LEVEL IN dB	OUTPUT LEVEL IN mVpp		TYPICAL FR4 TRACE LENGTH
			DE-EMPHASIZED	PREEMPHASIZED	
0	0	0 dB	1200	1200	10 inches (25,4 cm) of FR4 trace
0	1	3 dB	850	1200	20 inches (50,8 cm) of FR4 trace
1	0	6 dB	600	1200	30 inches (76,2 cm) of FR4 trace
1	1	9 dB	425	1200	40 inches (101,6 cm) of FR4 trace

(1) x = L or S

Table 3. Receive Equalization Settings

EQ	EQUALIZATION	TYPICAL TRACE
1	5 dB	25 inches (63,5 cm) of FR4
0	12 dB	43 inches (109,2 cm) of FR4

PARAMETER MEASUREMENT INFORMATION

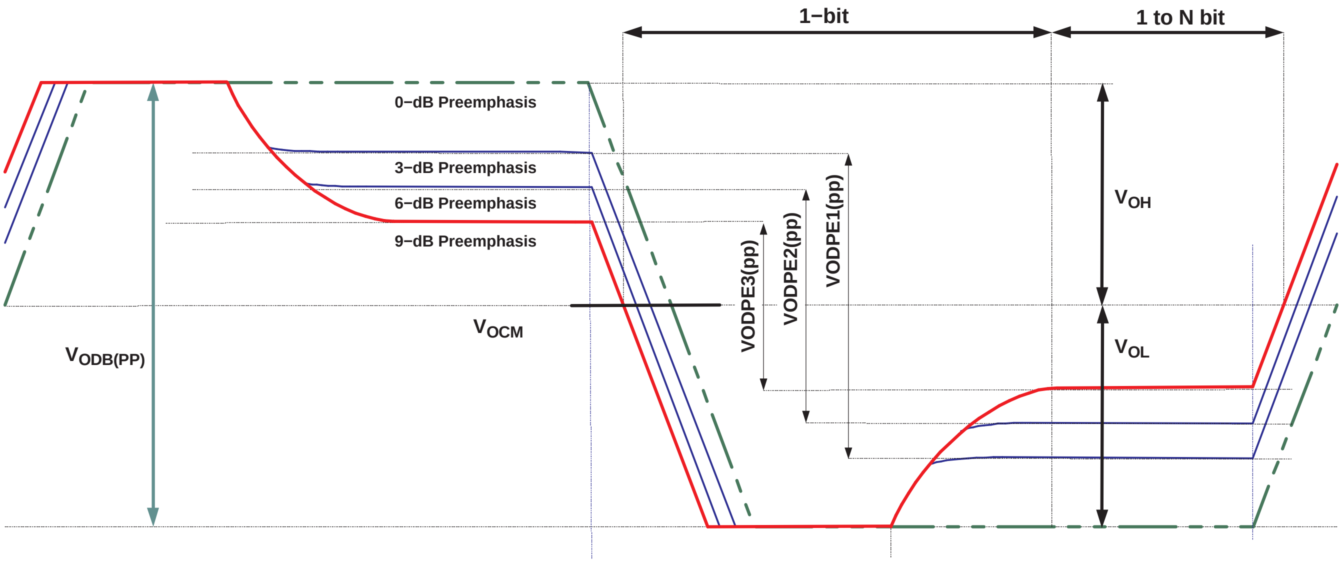


Figure 3. Preemphasis and Output Voltage Waveforms and Definitions

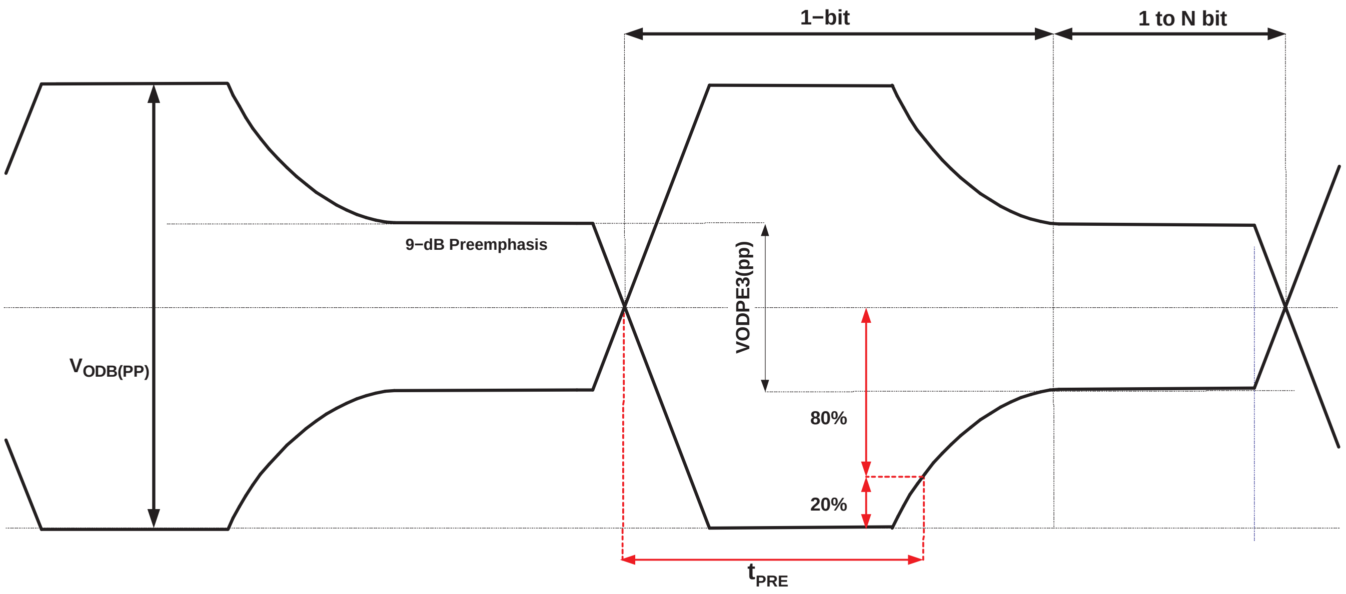


Figure 4. $t_{(PRE)}$) Preemphasis Duration Measurement

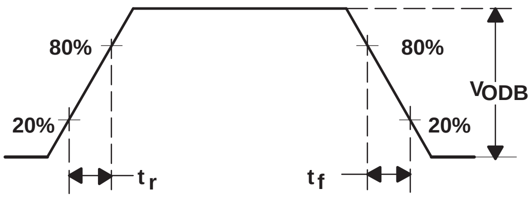


Figure 5. Driver Output Transition Time

PARAMETER MEASUREMENT INFORMATION (continued)

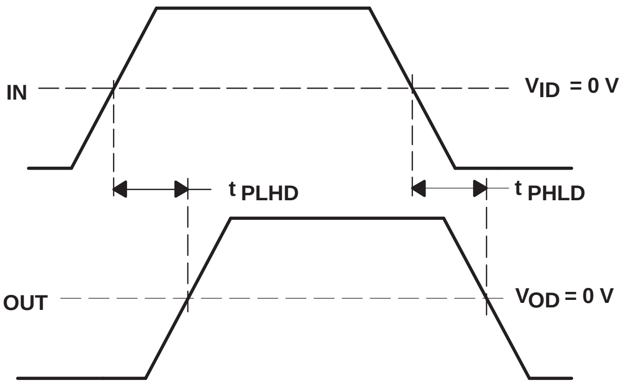
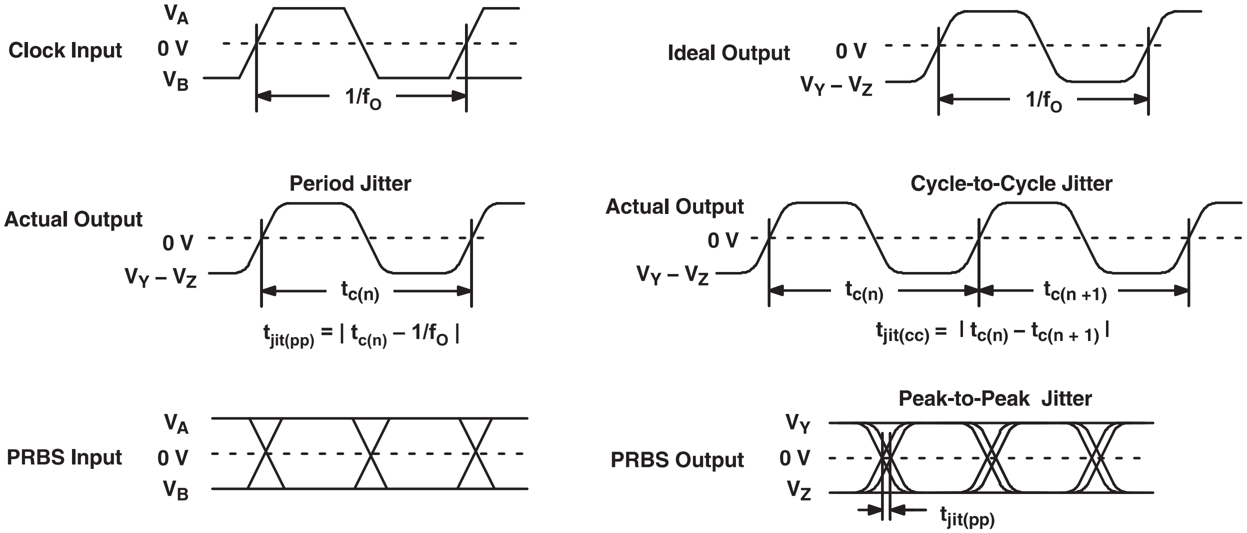


Figure 6. Propagation Delay Input to Output



A. All input pulses are supplied by an Agilent 81250 Stimulus System.

B. The measurement is made with the AgilentParBert measurement software.

Figure 7. Driver Jitter Measurement Waveforms

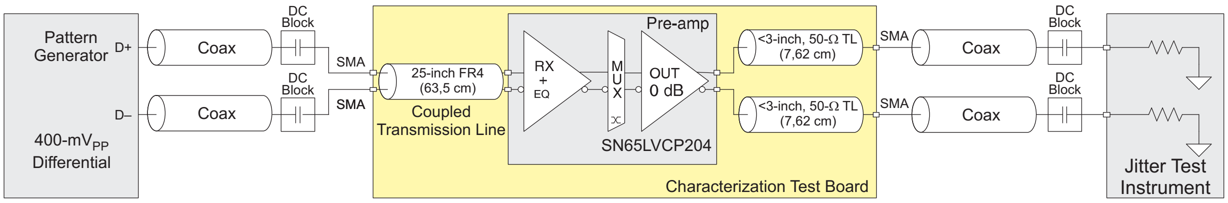
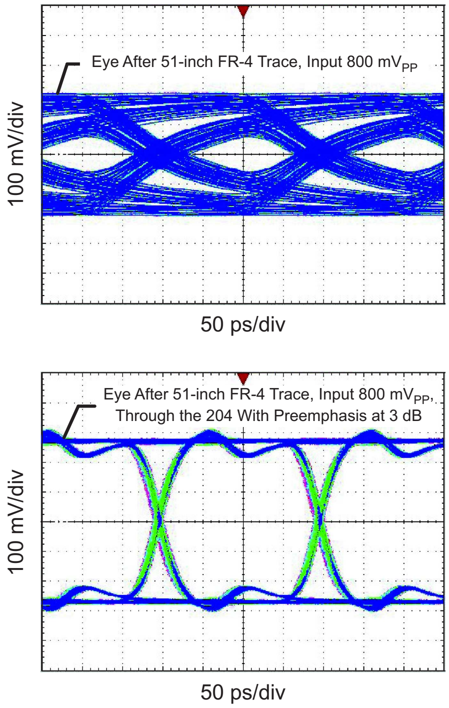


Figure 8. AC Test Circuit — Jitter and Output Rise Time Test Circuit

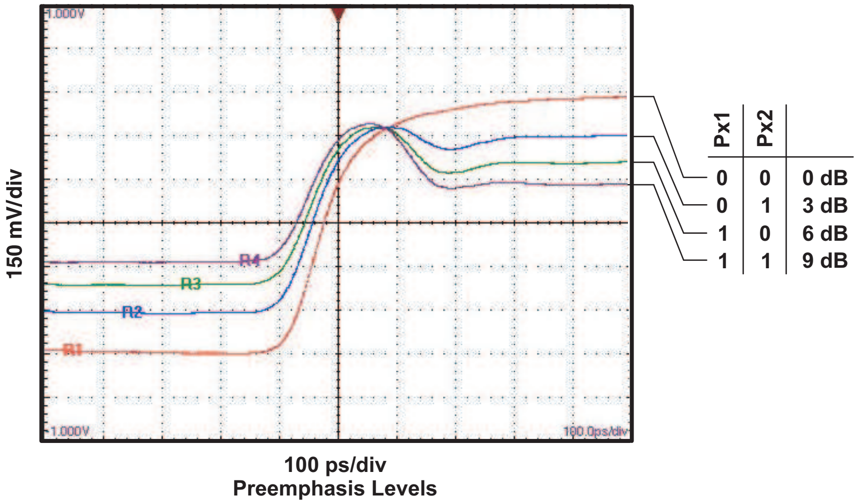
The SN65LVCP204 input equalizer provides 5-dB frequency gain to compensate for the frequency loss of a shorter backplane transmission line. For characterization purposes, a 25-inch (63,5 cm) FR-4 coupled transmission line is used in place of the backplane trace. The 25-inch trace provides roughly 5 dB of attenuation between 375 MHz and 2.125 GHz, representing closely the characteristics of a short backplane trace. The loss tangent of the FR4 in the test board is 0.018 with an effective ε(r) of 4.1.

TYPICAL DEVICE BEHAVIOR



NOTE: 51-Inch (129,54-cm) input trace, dR = 2.5 Gbps; $2^7 - 1$ PRBS

Figure 9. Data Input and Output Pattern



Px1	Px2	
0	0	0 dB
0	1	3 dB
1	0	6 dB
1	1	9 dB

Figure 10. Preemphasis Signal Shape

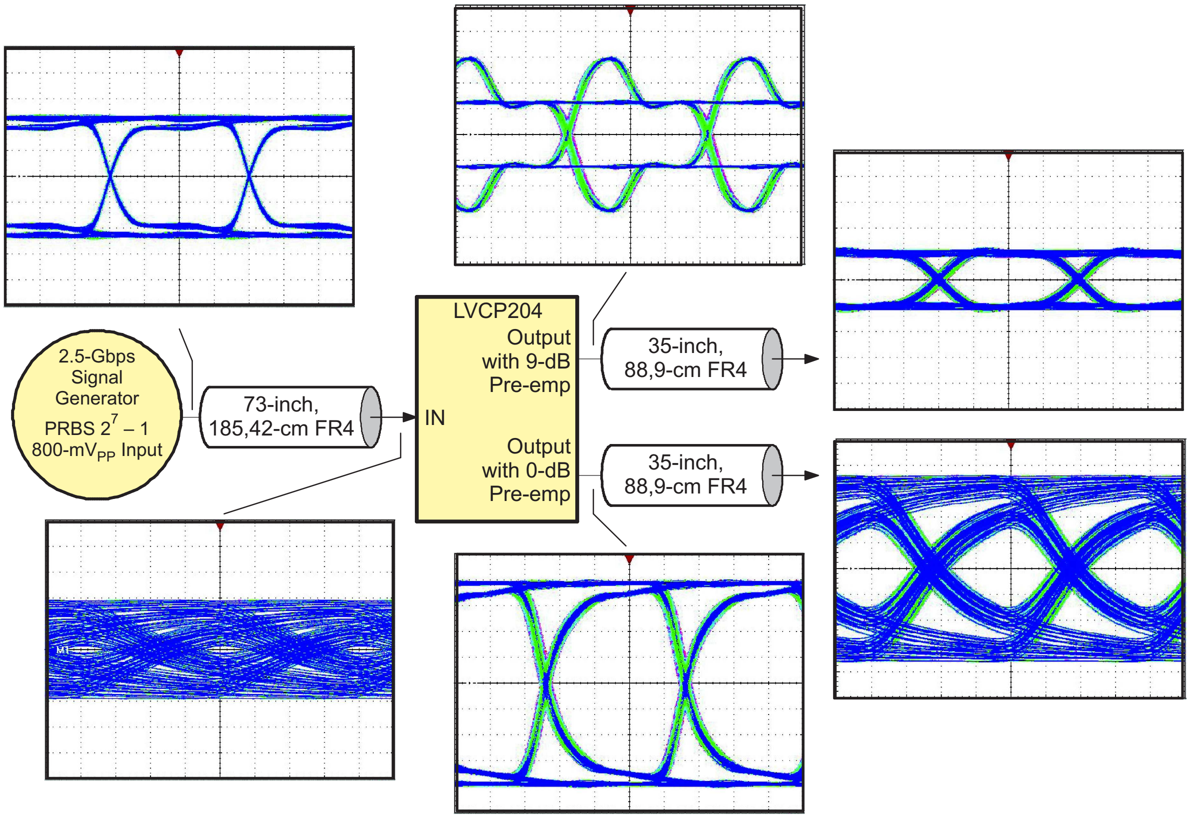


Figure 11. Data Output Pattern

TYPICAL CHARACTERISTICS

DETERMINISTIC OUTPUT JITTER vs DATA RATE

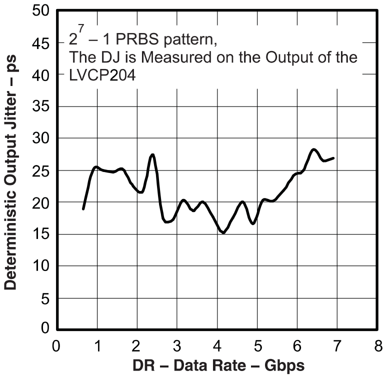


Figure 12.

DETERMINISTIC OUTPUT JITTER vs DIFFERENTIAL INPUT AMPLITUDE

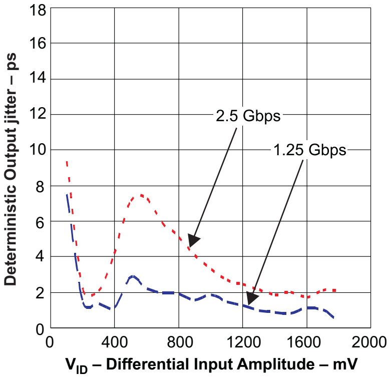


Figure 13.

DIFFERENTIAL OUTPUT VOLTAGE vs DATA RATE

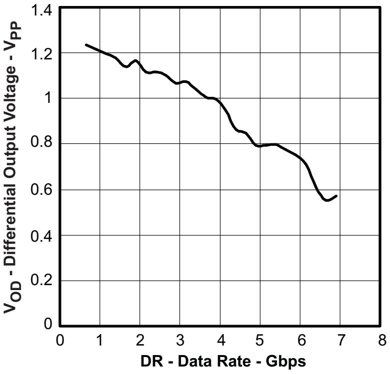


Figure 14.

DETERMINISTIC OUTPUT JITTER vs DATA RATE (SUPPLY NOISE IMPACT)

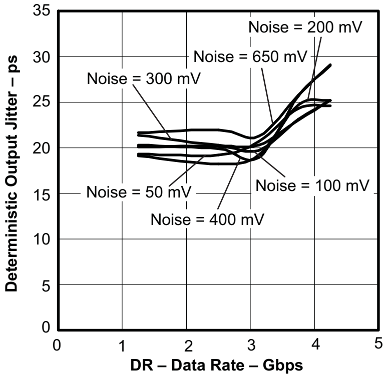


Figure 15.

DETERMINISTIC OUTPUT JITTER vs COMMON-MODE INPUT VOLTAGE

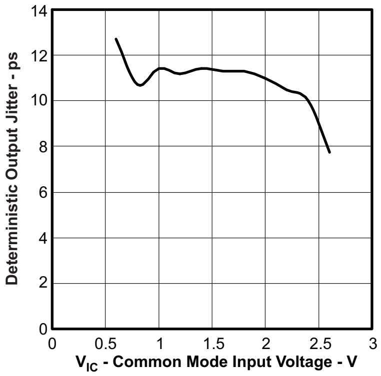
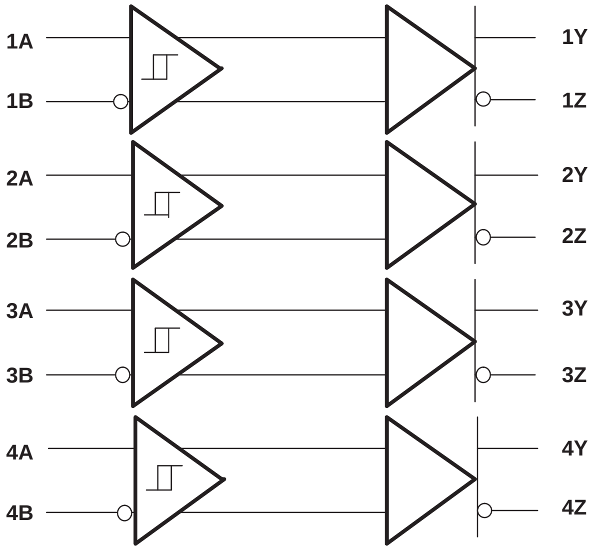


Figure 16.

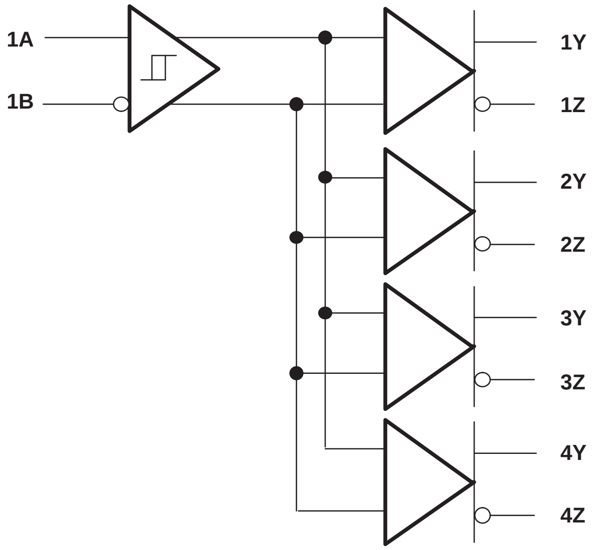
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

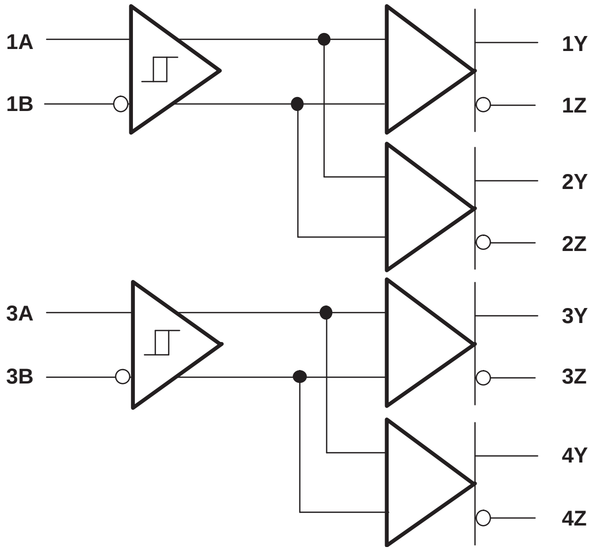
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



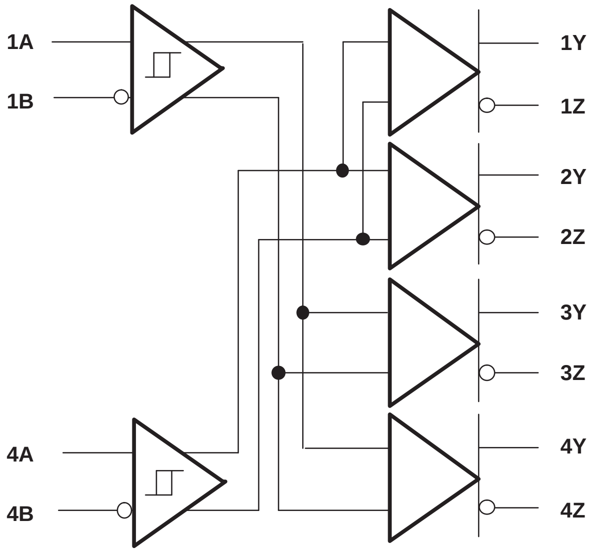
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



EXPLANATION OF EQUALIZATION

Backplane designs differ widely in size, layer stackup, and connector placement. In addition, the performance is impacted by trace architecture (trace width, coupling method) and isolation from adjacent signals. Common to most commercial backplanes is the use of FR4 as board material, with its related high-frequency signal attenuation. Within a backplane, the shortest to longest trace lengths differ substantially, often ranging from 8 inches (20,3 cm) up to 40 inches (101,6 cm). Increased loss is associated with longer signal traces. In addition, the backplane connector often contributes a good amount of signal attenuation. As a result, the signal attenuation for a 300-MHz signal might range from 1 dB to 4 dB, whereas the corresponding attenuation for a 2-GHz signal might span 6 dB to 24 dB. This frequency-dependent loss causes distortion jitter on the transmitted signal. Each SN65LVCP204 receiver input incorporates an equalizer and compensates for such frequency loss. The SN65LVCP204 equalizer provides 5 dB or 12 dB of frequency gain between 375 MHz and 1.875 GHz, compensating roughly for 20 inches (50,8 cm) of FR4 material with 8-mil (0,2-mm) trace width. Distortion jitter improvement is substantial, often providing more than 30-ps jitter reduction. The 5-dB compensation is sufficient for most short backplane traces. For longer trace lengths, it is recommended to enable transmit preemphasis in addition.

SETTING THE PREEMPHASIS LEVEL

The receive equalization compensates for ISI. This reduces jitter and opens the data eye. In order to find the best preemphasis setting for each link, calibration of every link is recommended. Assuming each link consists of a transmitter (with adjustable preemphasis, such as the SN65LVCP204) and the SN65LVCP204 receiver, the following steps are necessary:

1. Set the transmitter and receiver to 0-dB preemphasis; record the data eye on the SN65LVCP204 receiver output.
2. Increase the transmitter preemphasis until the data eye on the SN65LVCP204 receiver output looks the cleanest.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVCP204RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204
SN65LVCP204RGZR.B	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204
SN65LVCP204RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204
SN65LVCP204RGZT.B	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	LVCP204

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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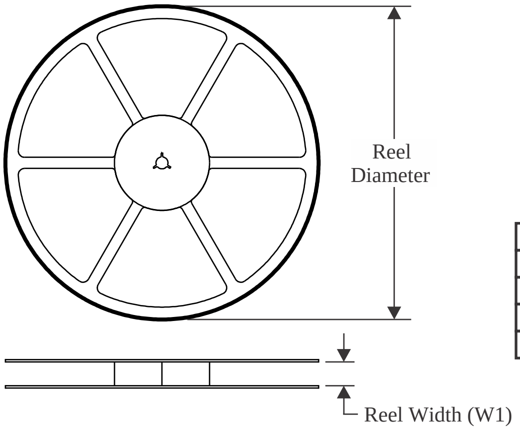
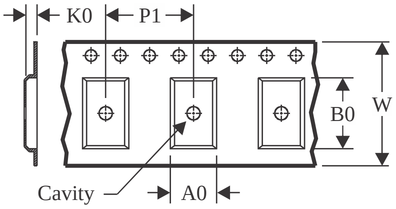
TAPE AND REEL INFORMATION

REEL DIMENSIONS

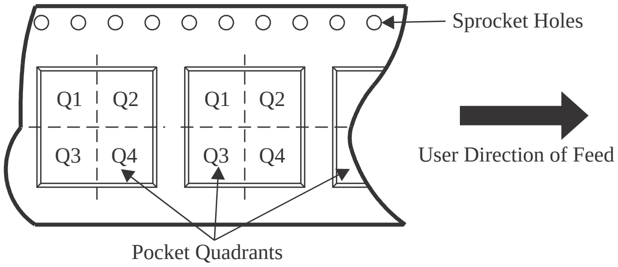


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

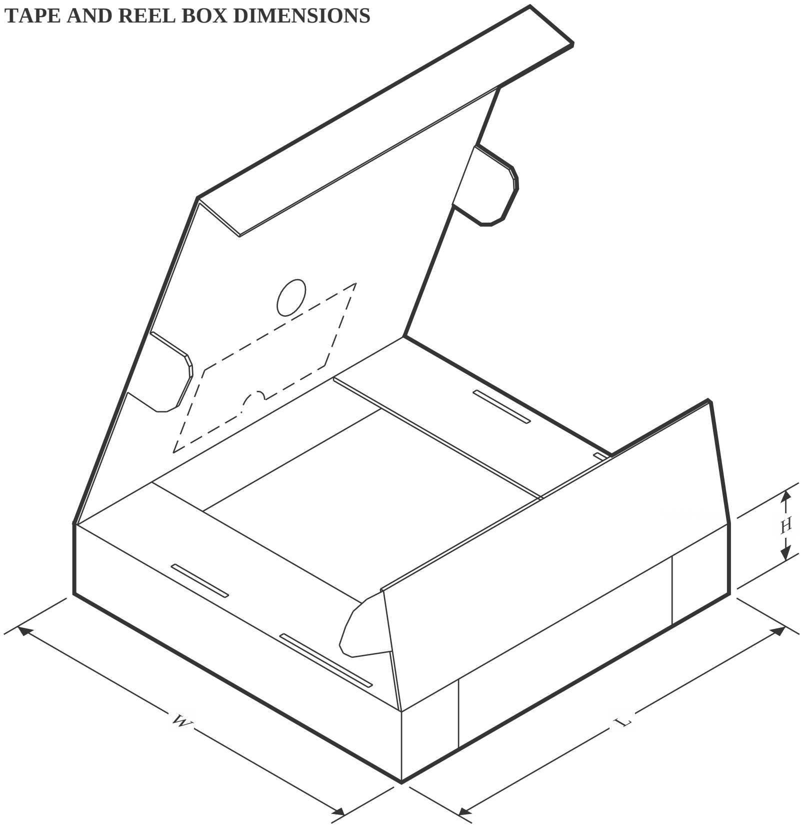
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVCP204RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN65LVCP204RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVCP204RGZR	VQFN	RGZ	48	2500	353.0	353.0	32.0
SN65LVCP204RGZT	VQFN	RGZ	48	250	213.0	191.0	35.0

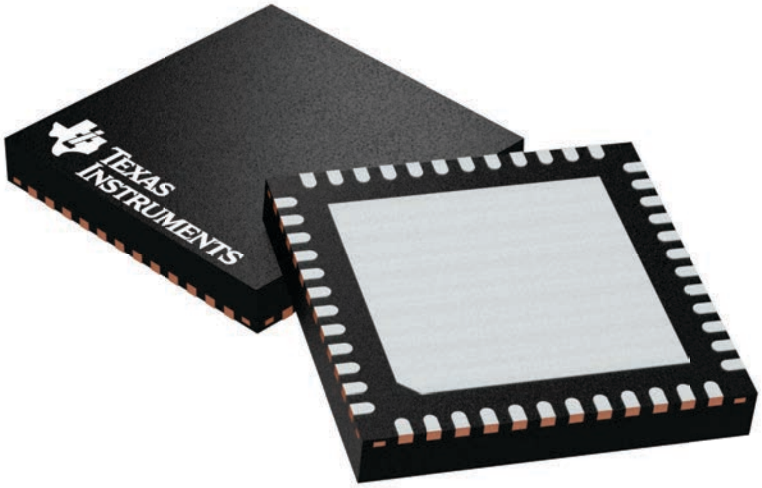
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

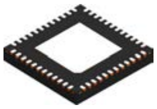


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

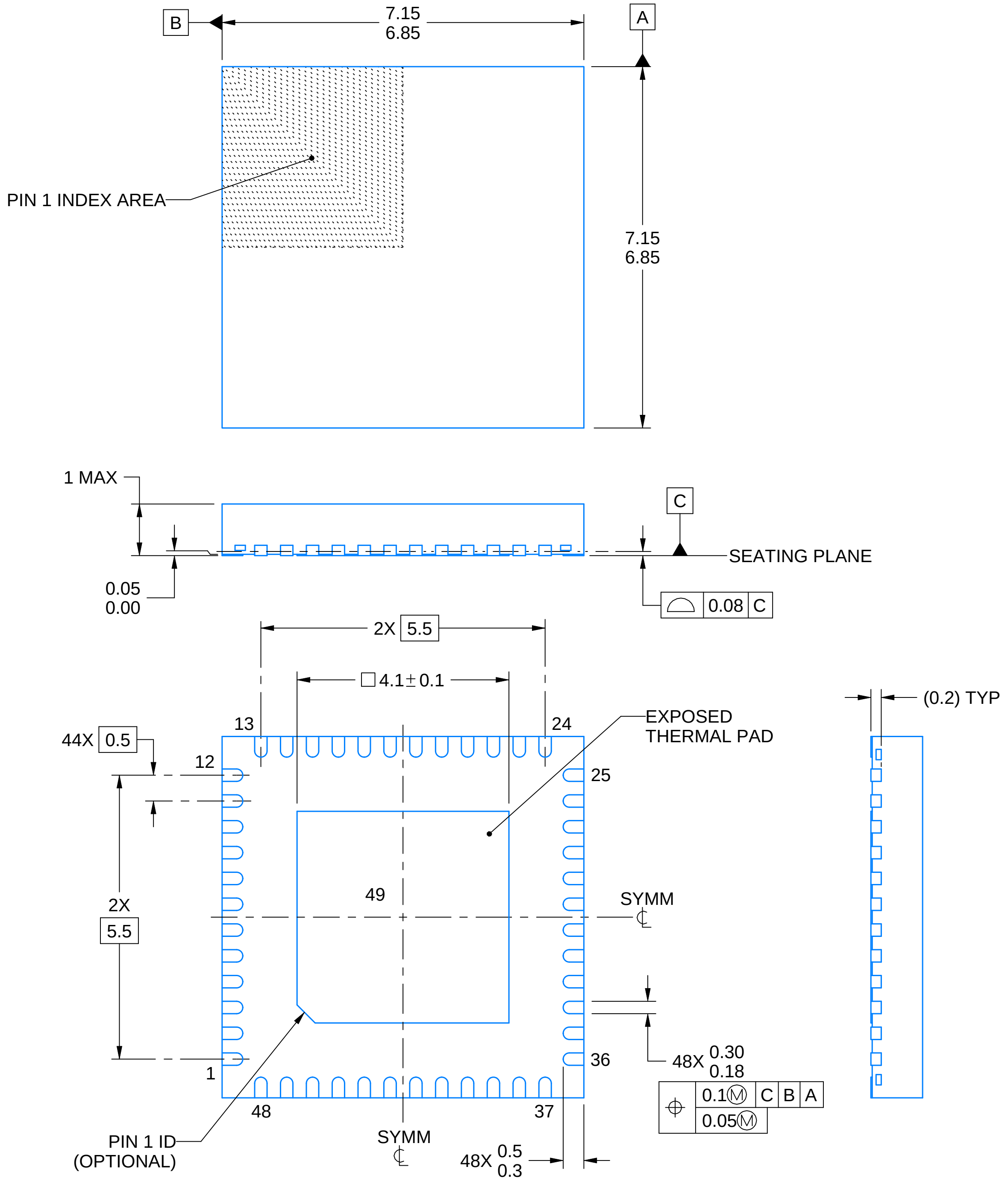
PACKAGE OUTLINE

RGZ0048B



VQFN - 1 mm max height

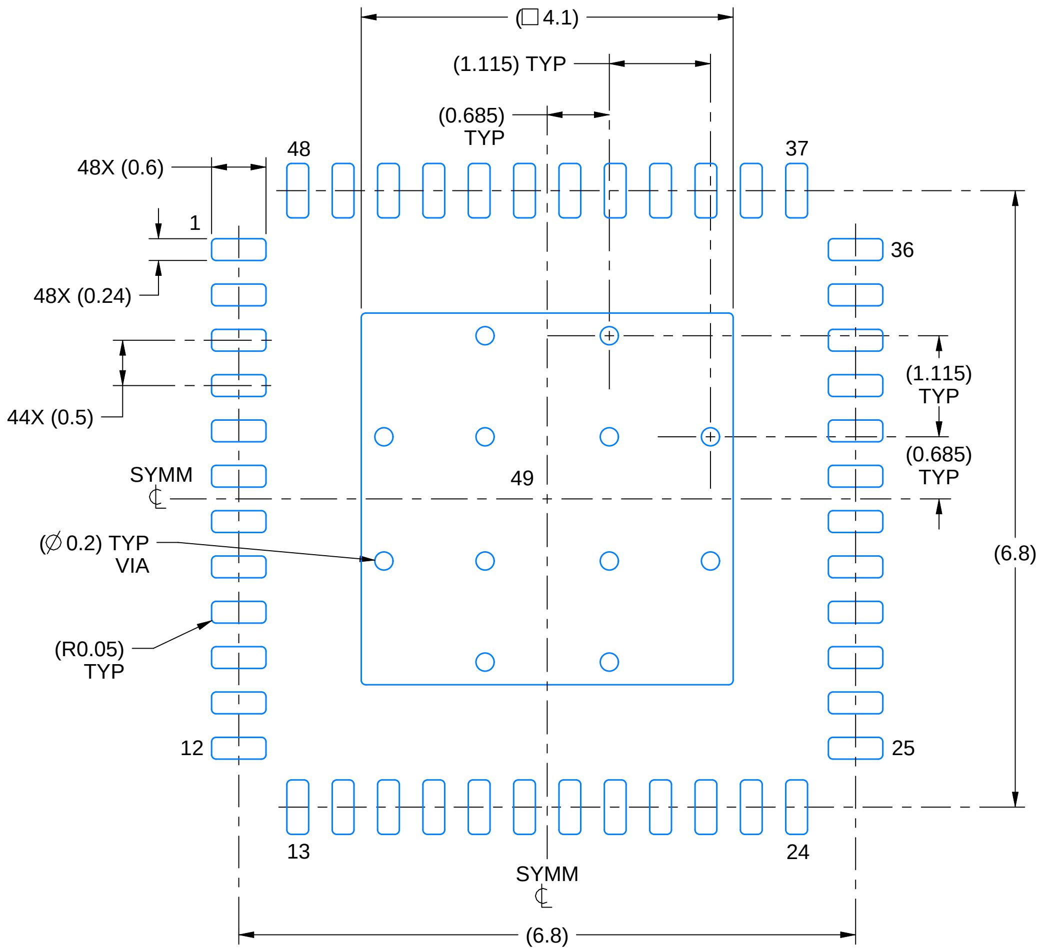
PLASTIC QUAD FLATPACK - NO LEAD



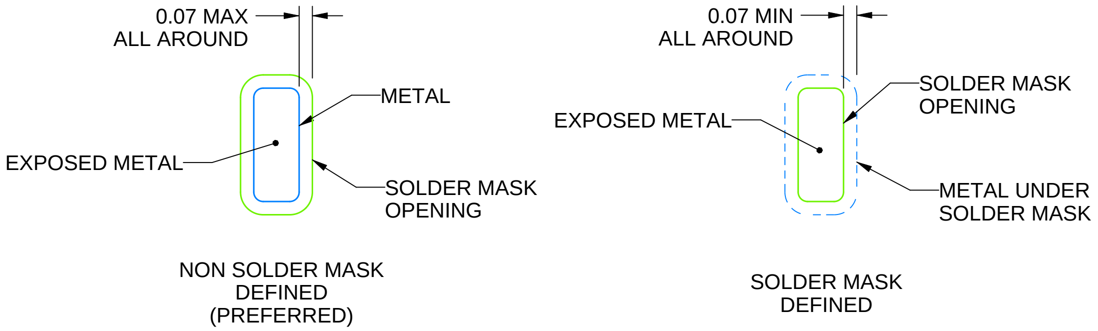
4218795/B 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



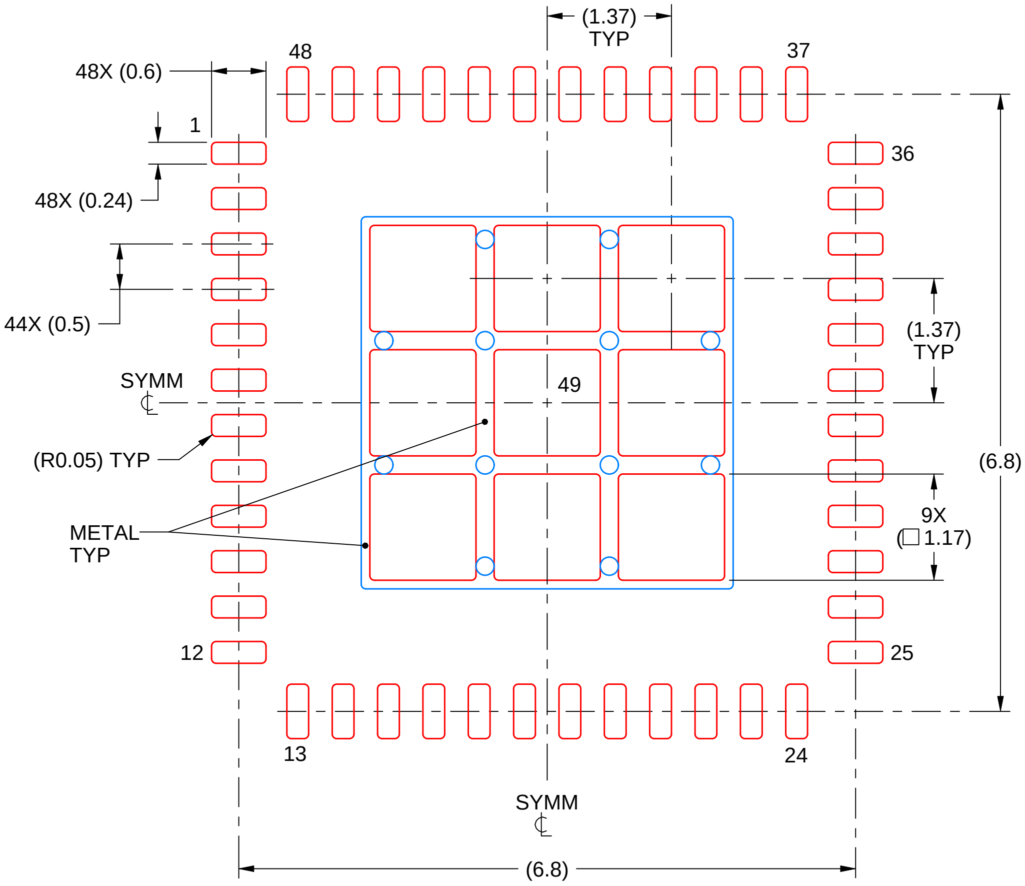
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025