

Quad Channel (Half X4 Lane) PCIe Redriver/Equalizer

Check for Samples: [SN65LVPE504](#)

FEATURES

- 4 Identical Channel PCIe Equalizer/Redriver
- Support for Both PCIe Gen I (2.5Gbps) and Gen II (5.0 Gbps) Speed
- Selectable Equalization, De-emphasis, and Output Swing
- Per Channel Receive Detect (Lane Detection)
- Selectable Receiver Electrical Idle Threshold Control
- Low Operating Power Modes
 - Supports Three Low-Power Modes to Enable up to 80% Lower Operating Power
- Excellent Jitter and Loss Compensation Capability to 50" of 4-mil SL on FR4
- Small Foot Print – 42 Pin 9 × 3.5 TQFN Package
- High Protection Against ESD Transient
 - HBM: 6,000 V
 - CDM: 1,000 V
 - MM: 200 V

DESCRIPTION

The SN65LVPE504 is a quad channel, half four lane PCIe redriver and signal conditioner supporting data rates of up to 5.0Gbps. The device complies with PCIe spec revision 2.1, supporting electrical idle and power management modes.

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE504 is designed to minimize the signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion PCIe signal will experience. Both equalization and de-emphasis levels for all 4 channels are controlled by the setting of signal control pins EQ, DE and OS.

See [Table 1](#) for EQ, DE and OS setting details.

APPLICATIONS

- PC MB, Docking Station, Server, Communication Platform, Backplane and Cabled Application

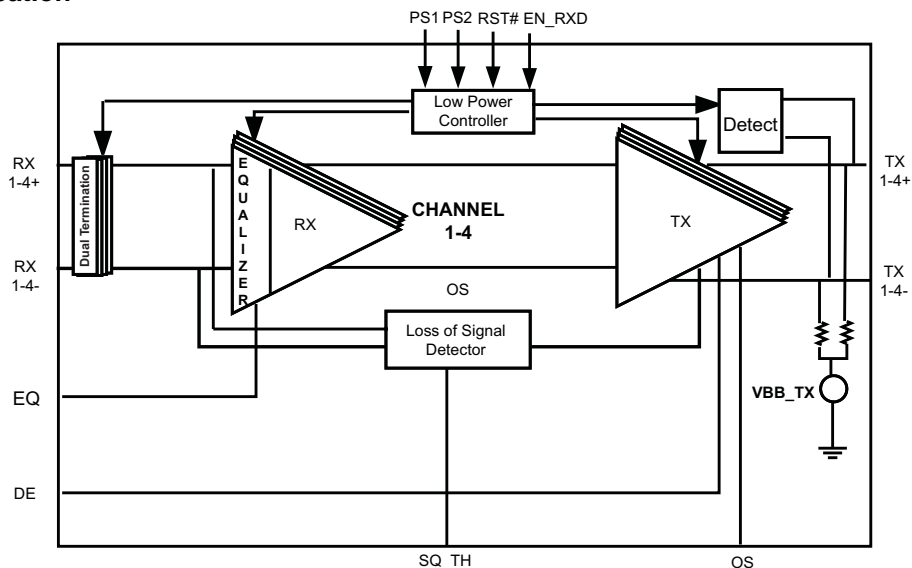


Figure 1. Data Flow Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DEVICE OPERATION

Device PowerOn

Device initiates internal power-on reset after V_{CC} has stabilized. External reset can also be applied at anytime by toggling \overline{RST} pin. External reset is recommended after every device power-up. After 50 μ s (MAX) from the application of \overline{RST} , device samples the state of EN_RXD, if it is set H device will enter Rx.Detect state where each of the four channels will perform Rx.Detect function (as described in PCIe spec). If EN_RXD is set L, automatic RX detect function is disabled and all channels are enabled with their termination set to Z_{RX_DC} .

Receiver Detection

While EN_RXD pin is H and device is not in reset state (\overline{RST} is H), LVPE504 performs RX.Detect on all its 4 channels indefinitely until remote termination is detected on at least one channel. When termination is detected on ≥ 1 CH, RX.Detect cycle is limited to 5 more tries on the other channels. At the end of 5th try those channels which failed to detect remote termination will be turned off to save power and their Rx termination is set to Z_{RX_HIGH} . In the event device detects only three channels, all four channels are enabled.

Automatic Rx detection feature on all four channels can be forced off by driving EN_RXD low. In this state all four channels input termination are set to Z_{RX_DC} .

Standby Mode

This is low power state triggered by $\overline{RST} = L$. In standby mode receiver termination resistor for each of the four channels is switched to Z_{RX_HIGH} of >50 k Ω and transmitters are pulled to Hi-Z state. Device power is reduced to <10mW (TYP). To get device out of standby mode \overline{RST} is toggled L-H.

Electrical Idle Support

A link is in an electrical idle state when the $T_{X\pm}$ voltage is held at a steady constant value like the common mode voltage. LVPE504 detects an electrical idle state when $R_{X\pm}$ input voltage of the associated channel falls below V_{EID_TH} min and stays in this state for at least 20ns. After detection of an electrical idle state in a given channel the device asserts electrical idle state in its corresponding TX. When $R_{X\pm}$ voltage exceeds V_{EID_TH} max, normal operation is restored and output start passing input signal. Electrical idle exit and entry time is specified at < 8 ns (MAX).

Electrical idle support is independent for each channel, however to lower active power it is possible to slave electrical idle function from channel 1 to CH2-CH4. This mode is selected by driving PS2 to H.

Power Save Features

Device supports three power save modes as below:

1. Standby Mode

This mode can be enabled from any state (Rx detect or active) by driving \overline{RST} L. In this state all 4 channels have their termination set to Z_{RX_HIGH} and outputs are at Hi-Z. Device power is 10mW (MAX).

2. Auto Low Power Mode

This mode is enabled when PS1 pin is tied H and device has been in active mode, i.e., past Rx detect state for >250ms (TYP). In this mode anytime $V_{in_diff_p-p}$ falls below selected V_{EID_TH} for a *given channel* and stays below V_{EID_TH} for >1 μ s, the associated CH enters auto low power (ALP) mode where power/CH is reduced by >80% of normal operating power/CH. A CH will exit ALP mode whenever $V_{in_diff_p-p}$ exceeds max V_{EID_TH} for that channel. Exit latency from ALP state is 30ns max. To use this mode link latency will need to account for the ALP exit time for N_FTS. ALP mode is handled by each channel independently based on its input differential signal level, unless slave mode is activated (PS2=H) when CH1 controls SQ detect of other channels based on its signal level.

3. Slave Power Mode

This mode is activated by driving PS2 high. Under normal operation squelch detection is handled by each channel independently. In slave mode SQ detection for CH2, CH3 and CH4 are turned off and squelch function is slaved to that of CH1. By turning off squelch detection circuitry for three of the four channels device saves power. To use this feature user must ensure all channels operate simultaneously

Squelch Control

Controls electrical idle detect threshold level. Three levels are supported as shown in [Table 1](#).

Beacon Support

With its broadband design, the SN65LVPE504 supports low frequency Beacon signal (as defined by PCIe 2.1 spec) used to indicate wake-up event to the system by a downstream device when in L2 power state. All requirements for a beacon signal as specified in PCI Express specification 2.1 must be met for device to pass beacon signals.

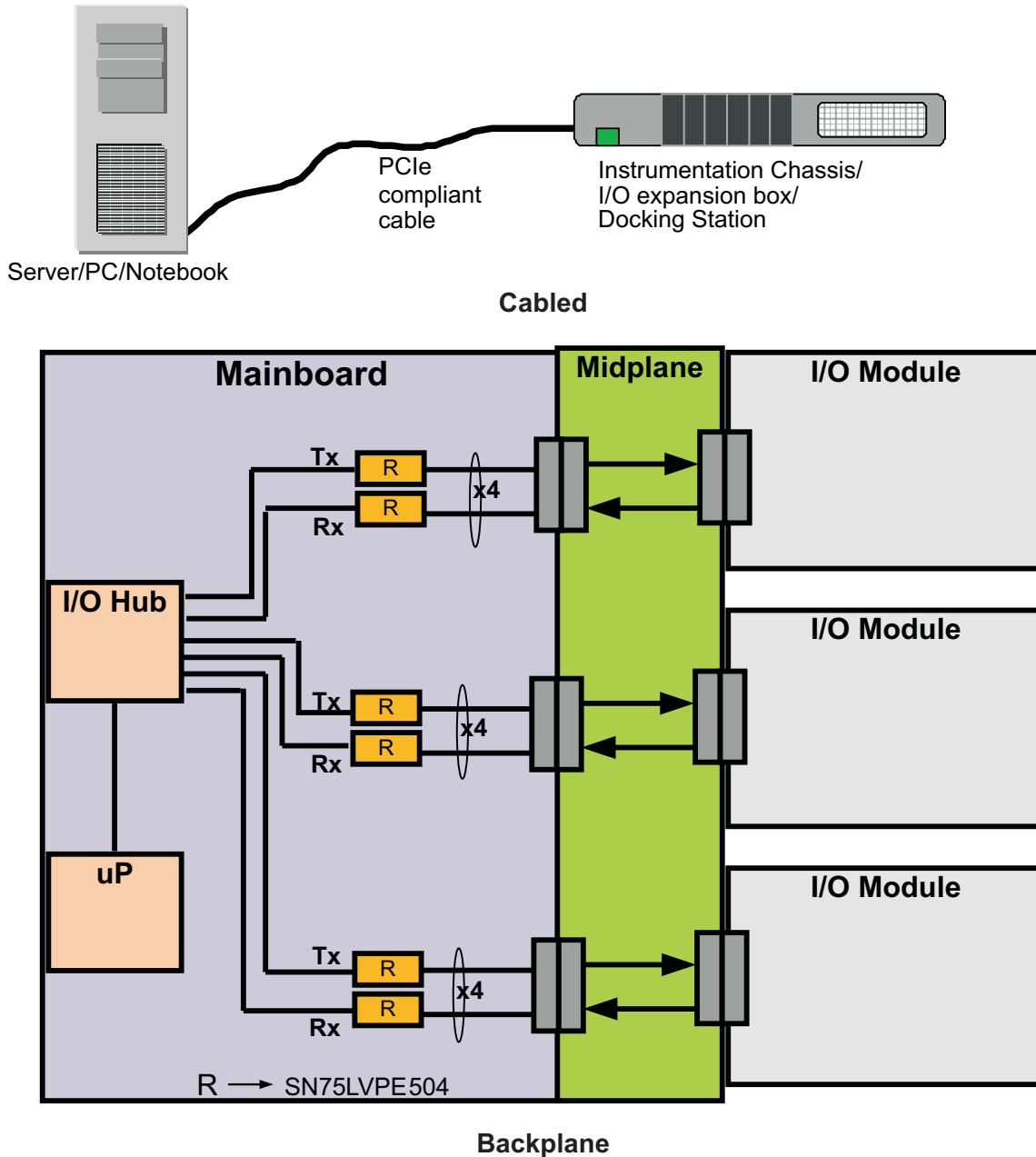


Figure 2. LVPE504 Typical Applications

DEVICE INFORMATION

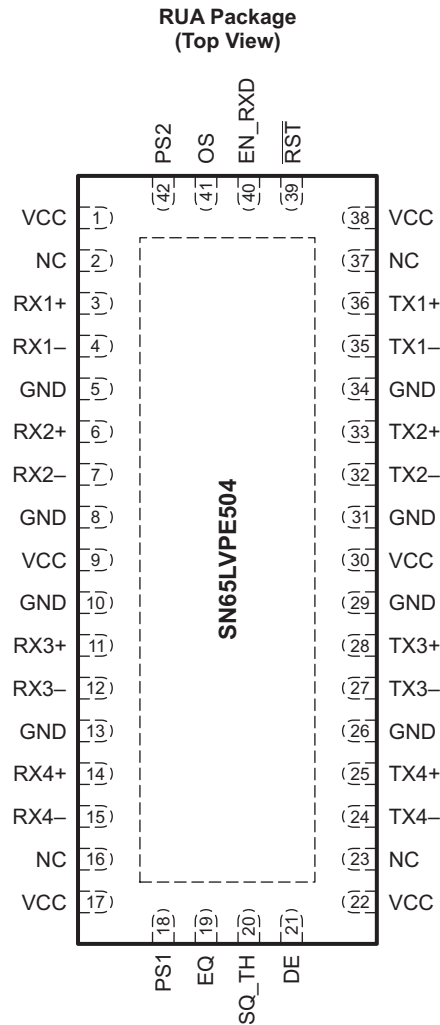


Figure 3. Flow-Through Pin-Out

PIN FUNCTIONS

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O PINS			
3	RX1+	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 4. These pins are tied to an internal voltage bias by dual termination resistor circuit
4	RX1-		
6	RX2+		
7	RX2-		
11	RX3+		
12	RX3-		
14	RX4+		
15	RX4-		
36	TX1+	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 4. These pins are internally tied to voltage bias by termination resistors
35	TX1-		
33	TX2+		
32	TX2-		

PIN FUNCTIONS (continued)

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O PINS (continued)			
28	TX3+	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 4. These pins are internally tied to voltage bias by termination resistors
27	TX3–		
25	TX4+		
24	TX4–		
DEVICE CONTROL PIN			
40	EN_RXD	I, LVCMOS	Sets device operation modes per Table 1 . Internally pulled to VCC
42	PS2	I, LVCMOS	Tying pin to VCC slaves CH2-4 electrical idle and Rx.Detect function to CH1. Internally pulled to GND
18	PS1	I, LVCMOS	Select auto-low power save mode per Table 1 . Internally pulled to GND
20	SQ_TH ⁽¹⁾	I, LVCMOS	Squelch threshold level select pin for electrical idle detect per Table 1 Internally pulled to VCC/2
39	RST	I, LVCMOS	Reset device, input active Low. Internally pulled to VCC
SIGNAL CONDITIONING PINS⁽¹⁾			
21	DE	I, LVCMOS	Selects de-emphasis settings for CH 1-CH 4 per Table 1 . Internally pulled to Vcc/2
19	EQ	I, LVCMOS	Selects equalization settings for CH 1-CH 4 per Table 1 . Internally pulled to Vcc/2
41	OS	I, LVCMOS	Selects output amplitude for CH 1-CH 4 per Table 1 . Internally pulled to Vcc/2
POWER PINS			
1,9,17,22,30,38	VCC	Power	Positive supply should be 3.3V ± 10%
5,8,10,13,26,29,31,34ū	GND	Power	Supply ground

- (1) Internally biased to Vcc/2 with >200kΩ pull-up/pull-down. When 3-state pins are left as NC, board leakage at the pin pad must be < 1 μA otherwise drive to Vcc/2 to assert mid-level state.

Table 1. Control Pin Settings

OUTPUT SWING (CH1-CH4) at 5Gbps				SQUELCH THRESHOLD (CH1-CH4)	
OS	TRANSITION BIT AMPLITUDE (TYP mVpp)			SQ_TH	MIN DIFFERENTIAL INPUT (CH1-CH4)
0	800			0	47 mVpp
NC (<i>default</i>)	929			NC (<i>default</i>)	61 mVpp
1	1047			1	83 mVpp
OUTPUT DE-EMPHASIS (CH1-CH4) at 5Gbps				INPUT EQUALIZATION (CH1-CH4)	
DE	OS = NC	OS = 0	OS = 1	EQ	Equalization dB (at 5Gbps)
NC (<i>default</i>)	–3.4dB	–2.1dB	–4.6dB	0	0
0	–6.2dB	–4.9dB	–7.2dB	NC	7 (<i>default</i>)
1	–10.3dB	–9.2dB	–11dB	1	15
EN_RXD		DEVICE FUNCTION			
0		Set input termination to Rx_DC			
1		Perform Rx detect after power up			
RST		DEVICE FUNCTION			
0		Device in standby state, inputs set to Hi-Z			
1		Device in active mode			
PS1		DEVICE FUNCTION			
0		Auto-low power mode disabled (<i>default</i>)			
1		Auto-low power mode enabled			
PS2		DEVICE FUNCTION			
0		Electrical Idle and Rx Detect independent for CH1-CH4 (<i>default</i>)			
1		CH2-CH4 Electrical Idle and Rx Detect slaved to CH1			

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE
SN65LVPE504RUAR	LVPE504	42-pin RUA Reel (large)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE	UNIT
Supply voltage range ⁽²⁾	V _{CC}	–0.5 to 4	V
Voltage range	Differential I/O	–0.5 to 4	V
	Control I/O	–0.5 to V _{CC} + 0.5	V
Electrostatic discharge	Human body model ⁽³⁾	±6000	V
	Charged-device model ⁽⁴⁾	±1000	V
	Machine model ⁽⁵⁾	±200	V
Continuous power dissipation		See Thermal Table	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101-A
- (5) Tested in accordance with JEDEC Standard 22, Test Method A115-A

THERMAL INFORMATION

THERMAL METRIC		SN65LVPE504	UNITS
		TQFN (42 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	30	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	12	
θ_{JB}	Junction-to-board thermal resistance	10	
Ψ_{JT}	Junction-to-top characterization parameter	0.5	
Ψ_{JB}	Junction-to-board characterization parameter	9	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	4.7	

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
V _{CC}	Supply voltage	3	3.3	3.6	V
C _{COUPLING}	AC Coupling capacitor	75		200	nF
Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

under recommended operating conditions

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE PARAMETERS						
I_{CC}	Supply current	\overline{RST} , DE _x , EQ _x , OS = NC, EN_RXD = NC, K28.5 pattern at 5 Gbps, VID = 1000mV _{p-p}		174	190	mA
$I_{CC_{Slave}}$		PS2 = V _{CC} ; \overline{RST} , DE _x , EQ _x , OS = NC, EN_RXD = NC, K28.5 pattern at 5 Gbps, V _{ID} = 1000mV _{p-p}		161	175	
$I_{CC_{ALP}}$		When auto-low power conditions are met, PS1 = V _{CC}		27	32	
$I_{CC_{ALP_Slave}}$		PS1, PS2 = V _{CC} and link in EID state		14	18	
$I_{CC_{NO_CONNECT}}$		EN_RXD = 1 No termination detected on any CH		2.5		
$I_{CC_{stdby}}$		\overline{RST} = GND			0.1	
	Maximum data rate				5	Gbps
AutoLP _{ENTRY}	Auto low power entry time	Electrical idle at input, Refer to Figure 7		1		μs
AutoLP _{EXIT}	Auto low power exit time	After first signal activity, Refer to Figure 7			30	ns
t_{ENB}	Device enable time	\overline{RST} 0 → 1		5	50	μs
t_{DIS}	Device disable time	\overline{RST} 1 → 0		0.1	2	μs
T_{RX_Detect}	Rx.Detect start event	EN_RXD = 1, Time to start Rx Detect after power up		6		μs
CONTROL LOGIC						
V_{IH}	High level Input Voltage		1.4		V _{CC}	V
V_{IL}	Low Level Input Voltage		-0.3		0.5	V
V_{HYS}	Input Hysteresis			150		mV
I_{IH}	High Level Input Current	OS, EQ, DE, SQ_TH, PS1, PS2 = V _{CC}			30	μA
		EN_RXD, \overline{RST} = V _{CC}			1	
I_{IL}	Low Level Input Current	PS1, PS2 = GND		-1		μA
		OS, EQ, DE, SQ_TH, EN_RXD, \overline{RST} = GND		-30		
RECEIVER AC/DC						
$V_{in_diff_p-p}$	RX1-RX4 Input voltage swing	AC coupled differential signal (5Gbps)	100		1200	mV _{p-p}
T_{RX_TJ}	Max Rx total timing error	At device pin (5Gbps)			0.4	UI
T_{RX_DJ}	Max Rx deterministic timing error	At device pin (5Gbps)			0.3	UI
V_{CM_RX}	RX1-RX4 Common mode voltage		0		3.6	V
$V_{in_COM_P}$	RX1-RX4 AC peak common mode voltage				150	mVP
Z_{RX_DC}	DC single ended impedance		40	55	60	Ω
Z_{RX_Diff}	DC Differential input impedance		80	98	120	Ω
Z_{RX_High}	DC Input high impedance	Device in standby mode. Rx termination not powered measured with respect to GND over 200 mV max	50	75		kΩ
V_{EID_TH}	Electrical idle detect threshold	Measured at receiver pin: SQ_TH = NC		61		mVpp
		SQ_TH = 1	58	83	107	
		SQ_TH = 0		47		
$RL_{RX-DIFF}$	Differential return loss	50 MHz – 1.25 GHz	10	15		dB
		1.25 GHz – 2.5 GHz	8	11		
RL_{RX-CM}	Common mode return loss	50 MHz – 2.5 GHz	9	14		dB

ELECTRICAL CHARACTERISTICS (continued)

under recommended operating conditions

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER AC/DC						
V _{TXDIFF_P-P}	Differential peak-to-peak output voltage	RL = 100Ω ±1%, OS = NC, transition Bit	866	929	1031	mV
		RL = 100Ω ±1%, OS = GND transition Bit	800			
		RL = 100Ω ±1% OS = VCC transition Bit	1047			
		RL = 100Ω ±1%, DE=NC, OS = 0,1,NC on-transition bit	620			
		RL = 100Ω ±1%, DE=OS = 0,1,NC on-transition bit	456			
		RL = 100Ω ±1%, DE=OS = 0,1,NC on-transition bit	288			
	De-emphasis level	OS = NC (Figure 9) for OS = 1 and NC see Table 1)	-3.0	-3.4	-4.0	dB
			-5.5	-6.2	-6.5	
			-9.0	-10.3	-10.6	
T _{DE}	De-emphasis width	At 5 Gbps	0.9			UI
Z _{TX_diff}	DC Differential impedance	Defined during signaling	80	100	120	Ω
RL _{diff_TX}	Differential return loss	f = 50 MHz – 1.25 GHz	10	20		dB
		f = 1.25 GHz – 2.5 GHz	8	13		
RL _{CM_TX}	Common mode return loss	f = 50 MHz – 2.5 GHz	6	12		dB
I _{TX_SC}	TX short circuit current	TX± shorted to GND		44	90	mA
V _{TX_CM_DC}	Transmitter DC common-mode voltage	Allowed DC CM voltage at TX pins		1.8	2.2	V
V _{TX_CM_AC2}	TX AC common mode voltage at Gen II speed	Max(V _{d+} + V _{d-}) / 2 – Min(V _{d+} + V _{d-})/2		30	100	mVpp
V _{TX_CM_AC1}	TX AC common mode voltage at Gen I speed	RMS(V _{d+} + V _{d-})/2 – DC _{AVG} (V _{d+} + V _{d-})/2		3	20	mV
V _{TX_CM_DeltaL0-L0s}	Absolute Delta DC CM voltage during active and idle states	V _{TX_CM_DC [L0]} – V _{TX_CM_DC [L0s]}	0		100	mV
V _{TX_CM-DC-Line-Delta}	Absolute delta of DC CM voltage between D+ and D-	V _{TX_CM_DC-D+ [L0]} – V _{TX_CM_DC-D- [L0]}	0		25	mV
V _{TX_idle_diff-AC-p}	Electrical idle differential peak output voltage	V _{TX-idle-D+} – V _{TX-idle-D-} , LP filtered to remove any DC component	0	1	20	mVpp
V _{TX_idle_diff-DC}	DC electrical idle differential output voltage	V _{TX_idle-D+} – V _{TX_idle-D-} , LP filtered to remove any AC component		1.9		mV
V _{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver			600	mV
t _R , t _F	Output rise/fall time	De-Emphasis = 0 dB, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output	30	55	70	ps
t _{RF_MM}	Output rise/fall time mismatch	De-Emphasis = 0dB, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output			20	ps
T _{diff_LH} , T _{diff_HL}	Differential propagation delay	De-Emphasis = 0dB (CH 0 and CH 1). Propagation delay between 50% level at input and output		280	350	ps
T _{INTRA_SKEW}	Output skew (same lane)	5 Gbps			15	ps
T _{INTER_SKEW}	Lane to lane skew	5 Gbps	-25		25	ps
t _{idleEntry} , t _{idleExit}	Idle entry and exit times	See Figure 5			8	ns
T _{tx_EID_min}	Minimum time in EID		20			ns
Tx EQUALIZATION AT GEN II SPEED						
TX _{DJ} ⁽¹⁾	Residual deterministic jitter	At point A1 in Figure 8, EQ/DE=NC, OS=HIGH		25	60	ps p-p
		At point A2 in Figure 8, EQ/DE=NC, OS=LOW		26	60	
		At point B in Figure 8, EQ/DE=NC, OS=HIGH		27	60	
TX _{RJ}	Residual random jitter	D24.3 pattern at point A1/A2/B in Figure 8			0.1	psrms

(1) Refer to Figure 8 with ±K28.5 pattern, -3.5dB DE from source AWG

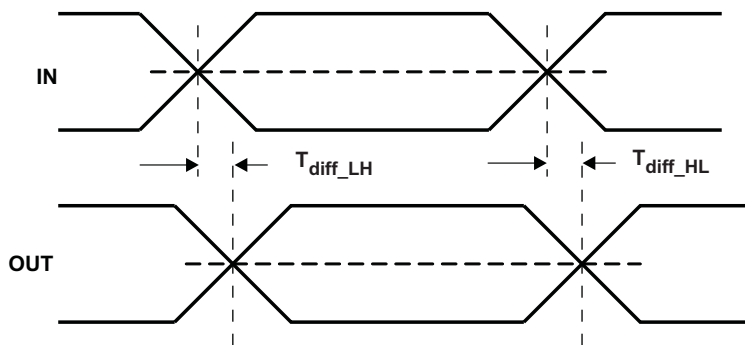


Figure 4. Propagation Delay

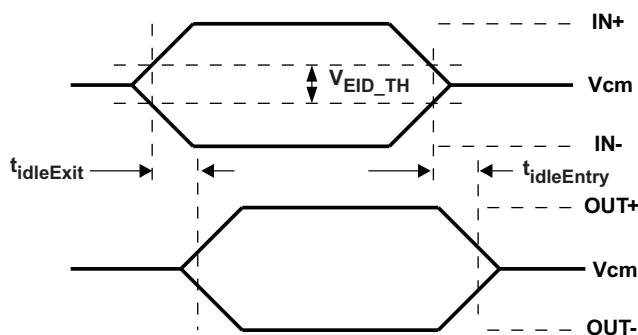


Figure 5. Idle Mode Exit and Entry Delay

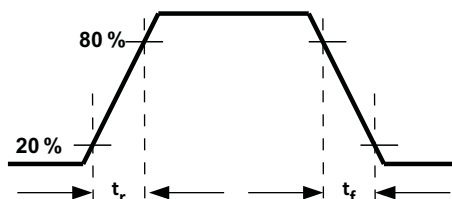


Figure 6. Output Rise and Fall Times

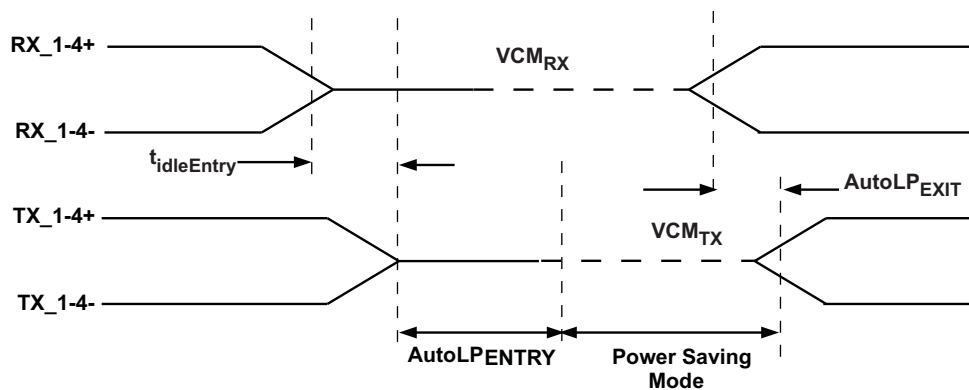


Figure 7. Auto Low Power Mode Timing (when enabled)

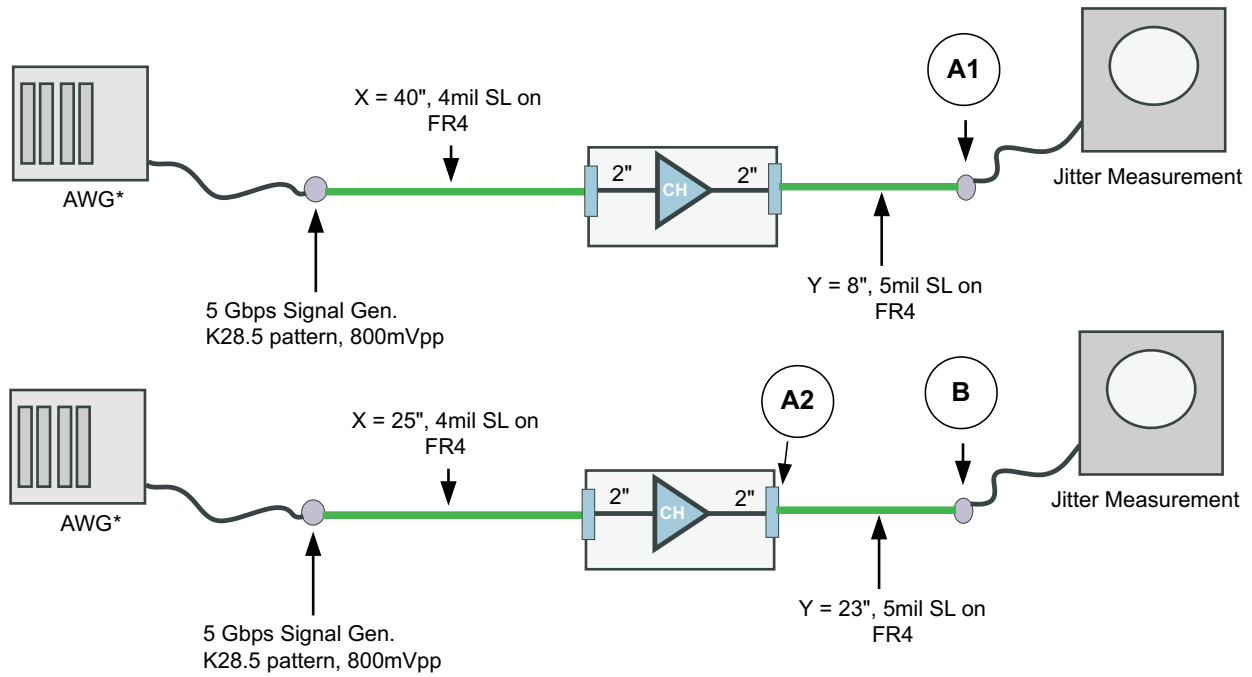


Figure 8. Jitter Measurement Setup

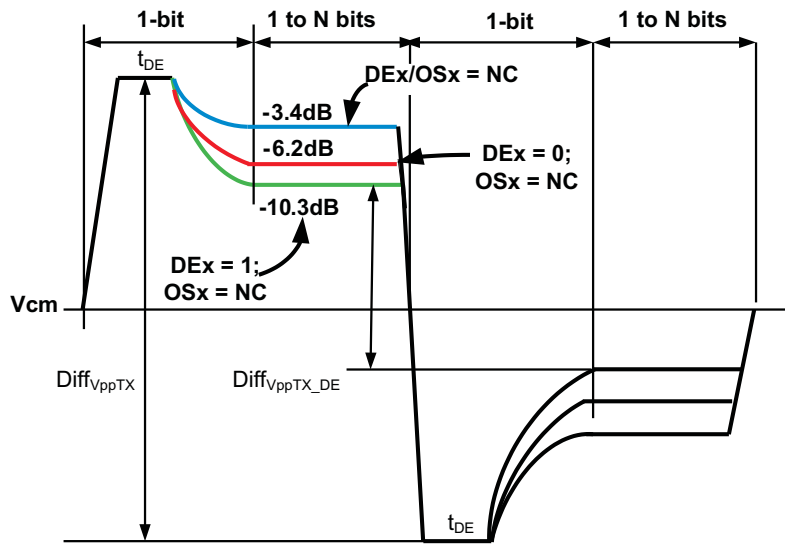


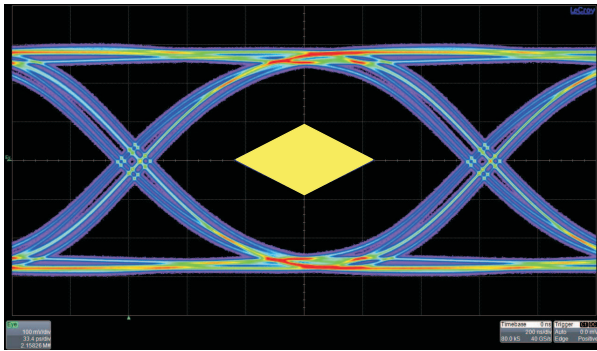
Figure 9. Output De-Emphasis Levels

TYPICAL CHARACTERISTICS

TYPICAL EYE DIAGRAM AND PERFORMANCE CURVES

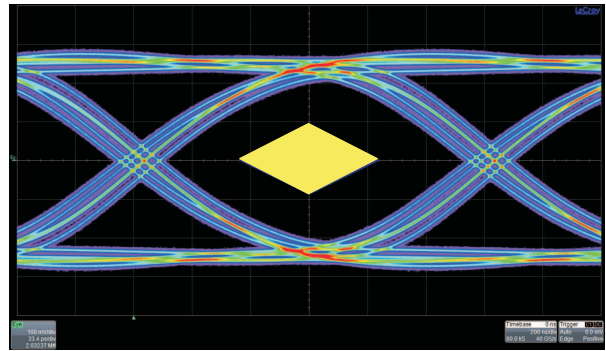
- Input Signal Characteristics – VID = 1000mVpp, DE = -3.5 dB, Pattern = K28.5
- Device Operating Conditions: VCC = 3.3 V, Temp = 25°C
- All trace are 4 mils
- PCIe Gen I and Gen II compliance mask shown

AT GEN II SPEED



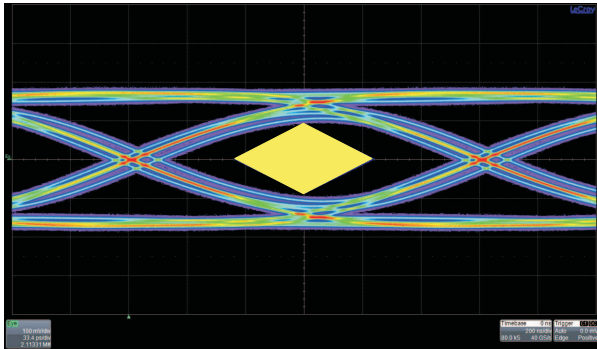
Input Trace = 4", Output Trace = 8"
EQ = 0 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 10.



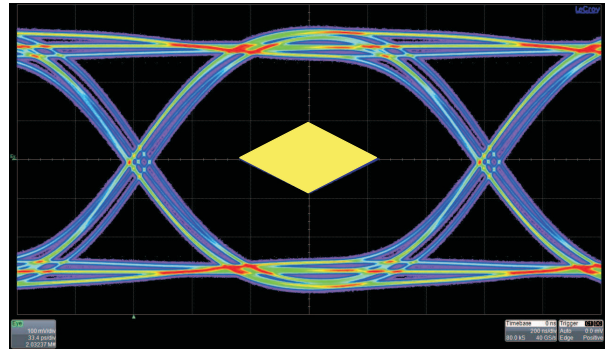
Input Trace = 4", Output Trace = 16"
EQ = 0 dB, OS = 1166 mVpp, DE = -4.9 dB

Figure 11.



Input Trace = 4", Output Trace = 28"
EQ = 0 dB, OS = 1166 mVpp, DE = -7.4 dB

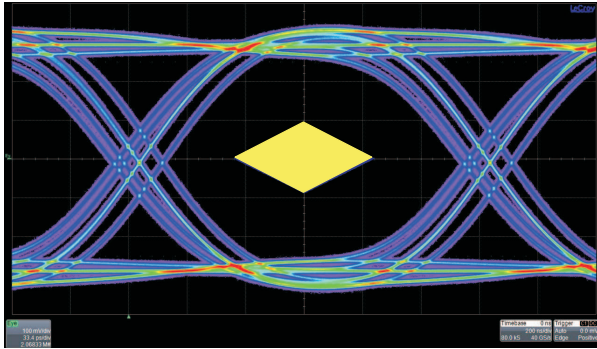
Figure 12.



Input Trace = 16", Output Trace = 4"
EQ = 0 dB, OS = 833 mVpp, DE = -1.9 dB

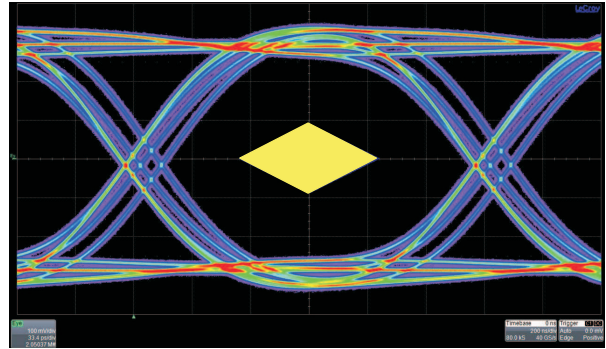
Figure 13.

TYPICAL CHARACTERISTICS (continued)



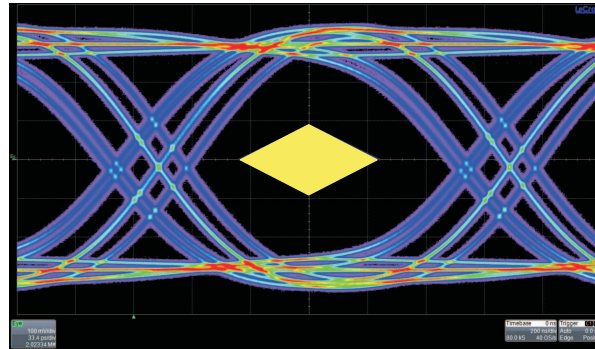
Input Trace = 28", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 14.



Input Trace = 36", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = -1.9 dB

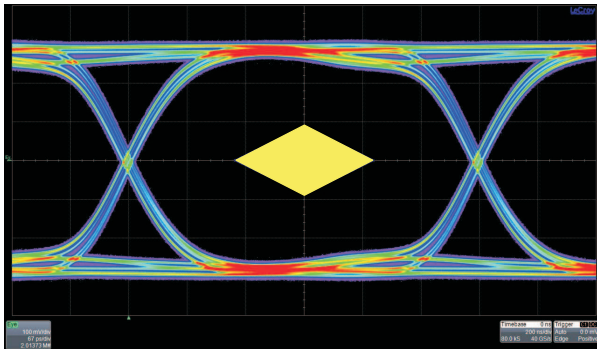
Figure 15.



Input Trace = 48", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = -1.9 dB

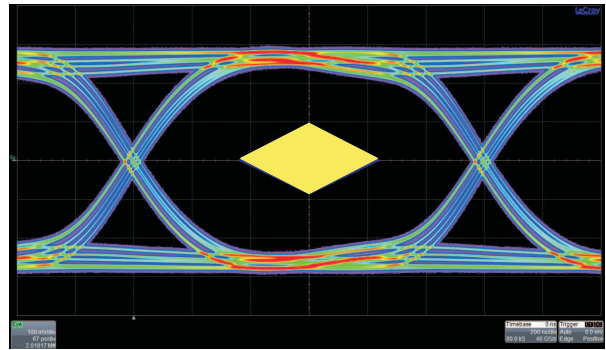
Figure 16.

AT GEN I SPEED



Input Trace = 4", Output Trace = 8"
EQ = 7 dB, OS = 833 mVpp, DE = -1.9 dB

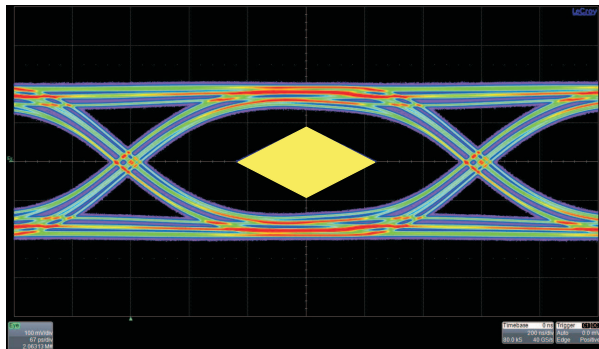
Figure 17.



Input Trace = 4", Output Trace = 16"
EQ = 7 dB, OS = 1166 mVpp, DE = -4.9 dB

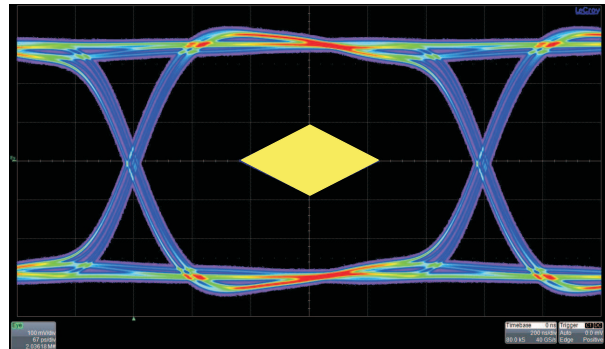
Figure 18.

TYPICAL CHARACTERISTICS (continued)



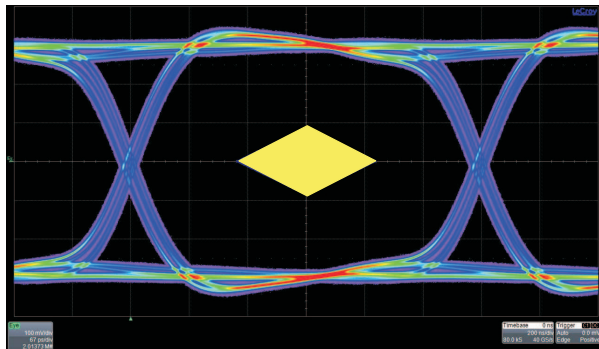
Input Trace = 4", Output Trace = 28"
EQ = 7 dB, OS = 1166 mVpp, DE = -7.4 dB

Figure 19.



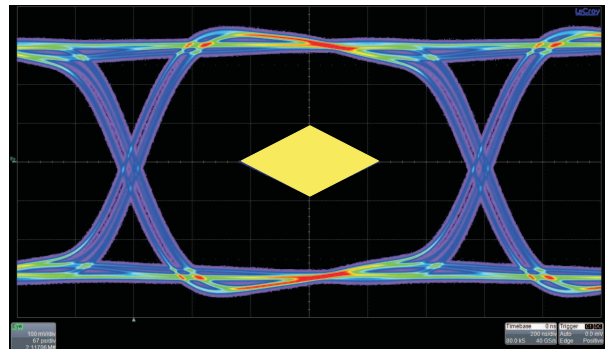
Input Trace = 16", Output Trace = 4"
EQ = 7 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 20.



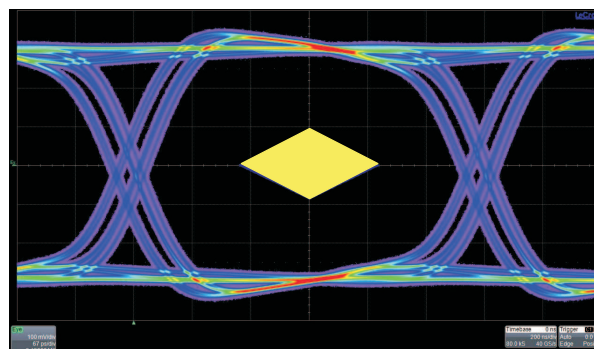
Input Trace = 28", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 21.



Input Trace = 36", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 22.



Input Trace = 48", Output Trace = 4"
EQ = 15 dB, OS = 833 mVpp, DE = -1.9 dB

Figure 23.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVPE504RUAR	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE504
SN65LVPE504RUAR.B	Active	Production	WQFN (RUA) 42	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE504

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE504RUAR	WQFN	RUA	42	3000	330.0	16.4	3.8	9.3	1.0	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE504RUAR	WQFN	RUA	42	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

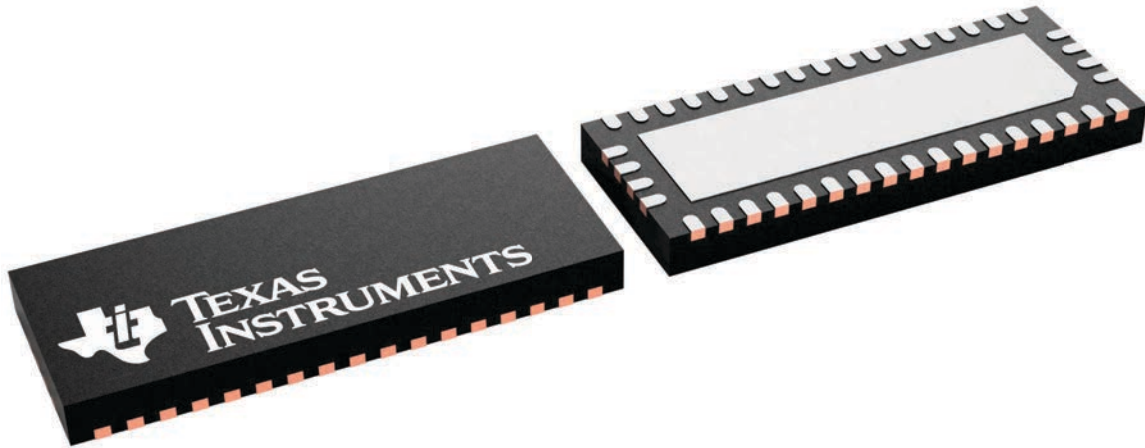
RUA 42

WQFN - 0.8 mm max height

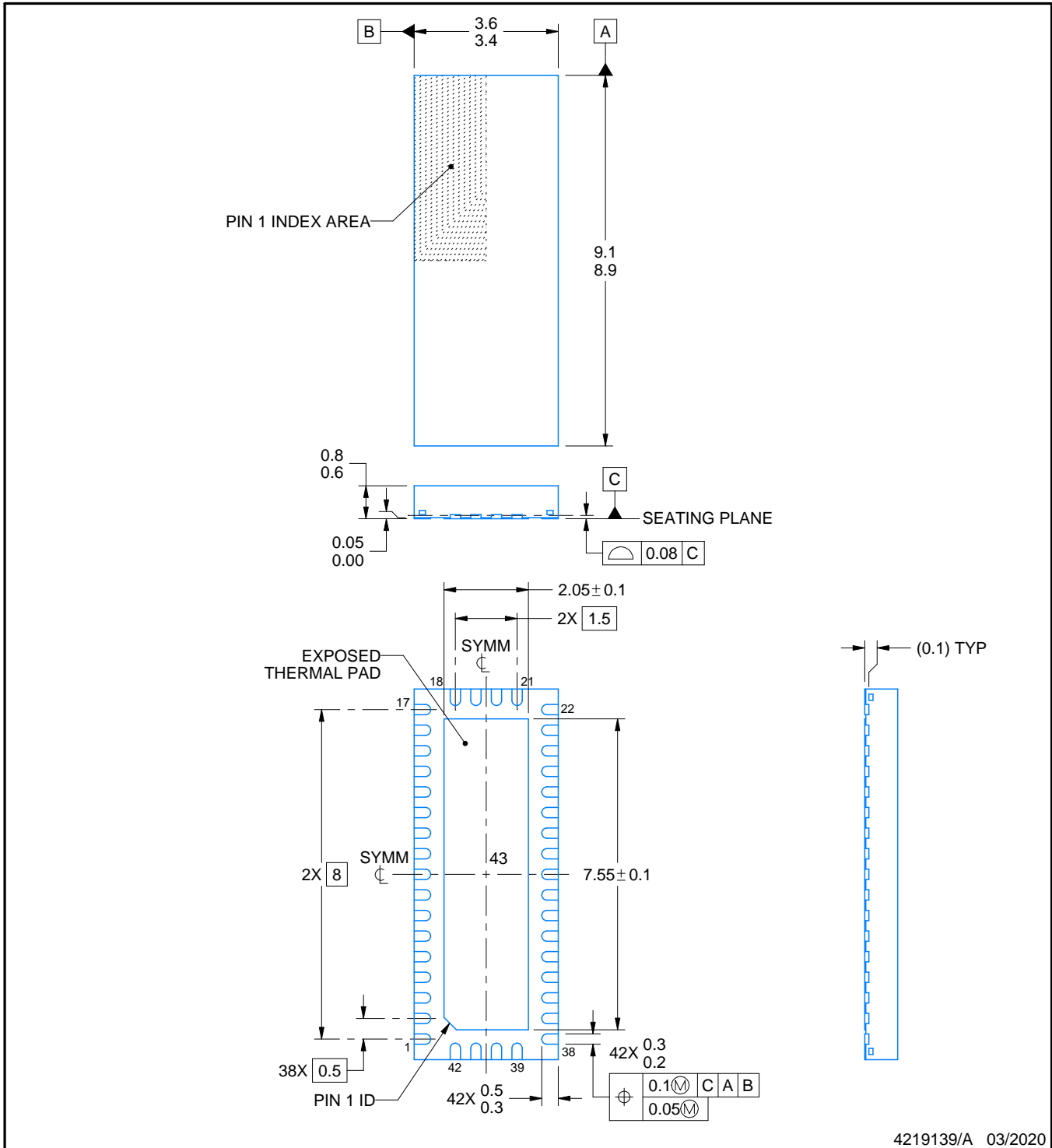
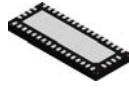
9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A



NOTES:

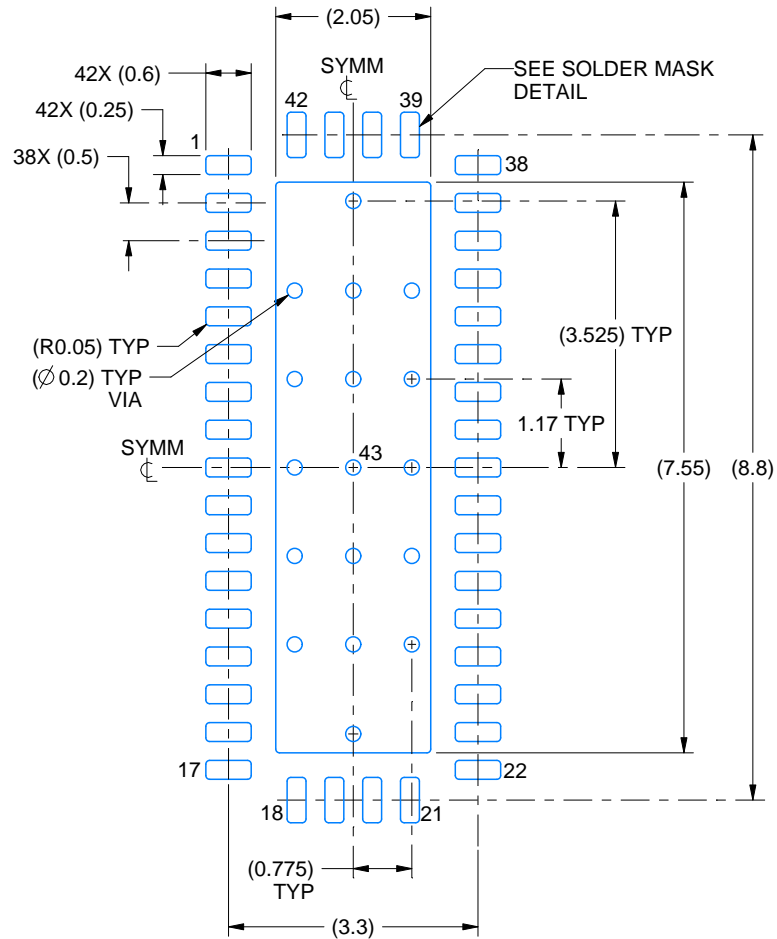
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

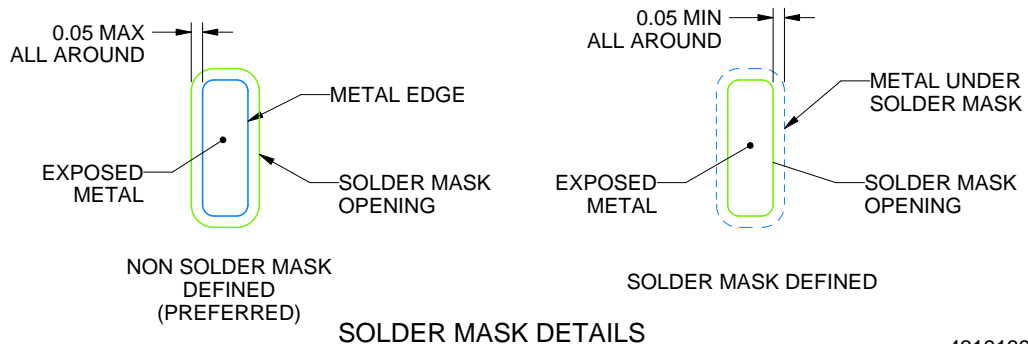
RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



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NOTES: (continued)

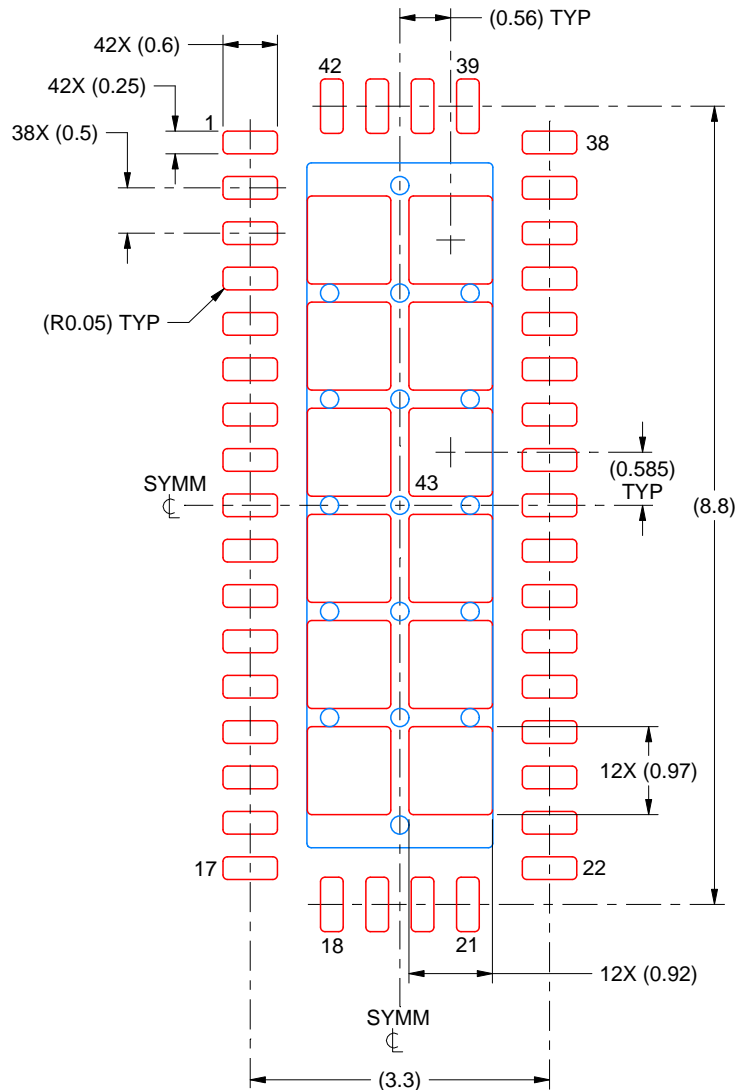
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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