

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs (-32 -mA I_{OH} , 64 -mA I_{OL})**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings**

description

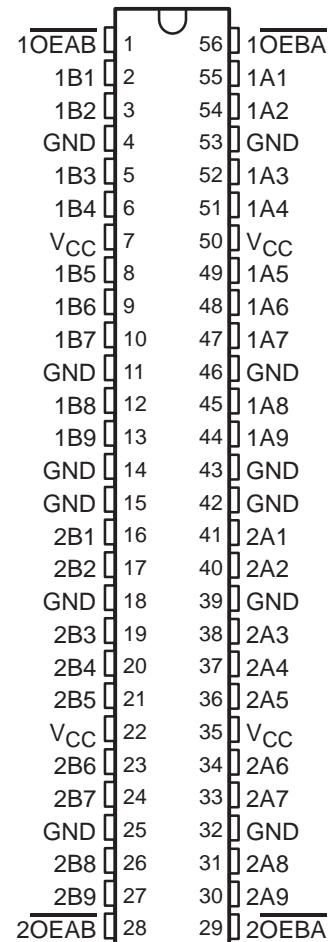
The 'ABT16863 are 18-bit noninverting transceivers designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

The 'ABT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable (\overline{OEAB} or \overline{OEBA}) inputs.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16863 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16863 is characterized for operation from -40°C to 85°C .

SN54ABT16863 . . . WD PACKAGE
SN74ABT16863 . . . DL PACKAGE
(TOP VIEW)



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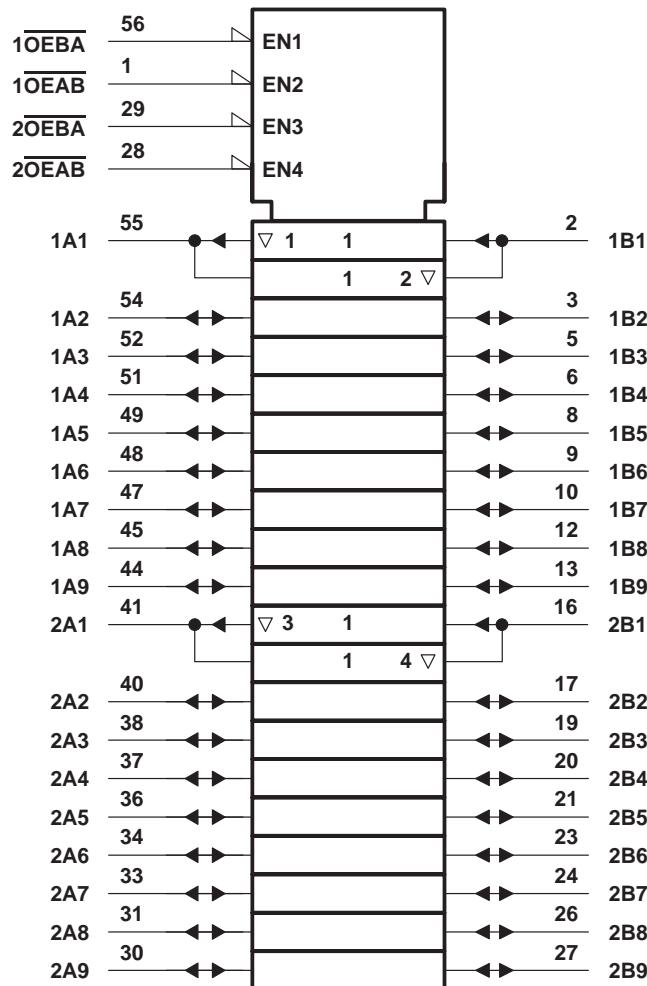
**SN54ABT16863, SN74ABT16863
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

SCBS225C – JUNE 1992 – REVISED MAY 1997

FUNCTION TABLE
(each 9-bit section)

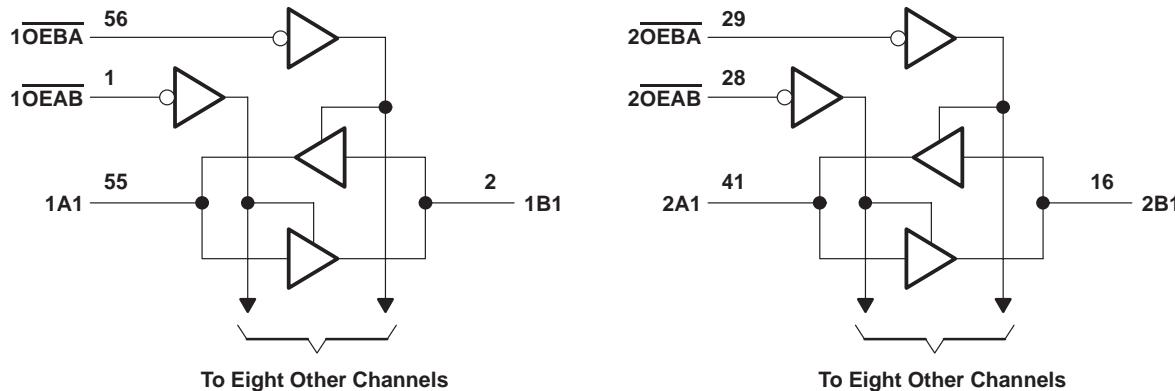
| INPUTS | | OPERATION |
|--------|------|-----------------|
| OEAB | OEBA | |
| H | L | B data to A bus |
| L | H | A data to B bus |
| H | H | Isolation |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

| | | |
|---|-------|-----------------|
| Supply voltage range, V_{CC} | | -0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT16863 | | 96 mA |
| SN74ABT16863 | | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DL package | | 74°C/W |
| Storage temperature range, T_{STG} | | -65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

| | | SN54ABT16863 | | SN74ABT16863 | | UNIT |
|--------------------------|------------------------------------|-----------------|----------|--------------|----------|-----------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -24 | | -32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta V$ | Input transition rise or fall rate | Outputs enabled | | 10 | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | | 200 | 200 | $\mu s/V$ |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TA = 25°C | | | SN54ABT16863 | | SN74ABT16863 | | UNIT |
|---------------------|---|--|------------------|-------|--------------|------|--------------|------|------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| VIK | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | -1.2 | | -1.2 | V |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -3 mA | 2.5 | | 2.5 | | 2.5 | | 2.5 | V |
| | V _{CC} = 5 V, I _{OH} = -3 mA | 3 | | 3 | | 3 | | 3 | |
| | V _{CC} = 4.5 V | I _{OH} = -24 mA | 2 | | 2 | | | 2 | |
| | | I _{OH} = -32 mA | 2* | | | | | 2 | |
| V _{OL} | V _{CC} = 4.5 V | I _{OL} = 48 mA | | 0.55 | | 0.55 | | | V |
| | | I _{OL} = 64 mA | | 0.55* | | | | 0.55 | |
| V _{hys} | | 100 | | | | | | | mV |
| I _I | Control inputs | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | | | ±1 | | ±1 | ±1 | µA |
| | A or B ports | V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND | | | ±20 | | ±20 | ±20 | |
| I _{OZPU} ‡ | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = X | | | ±50 | | ±50 | | ±50 | µA |
| I _{OZPD} ‡ | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = X | | | ±50 | | ±50 | | ±50 | µA |
| I _{OZH} § | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V | | | 10 | | 10 | | 10 | µA |
| I _{OZL} § | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V | | | -10 | | -10 | | -10 | µA |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | | ±100 | | | | ±100 | µA |
| I _{CEX} | Outputs high | V _{CC} = 5.5 V, V _O = 5.5 V | | | 50 | | 50 | 50 | µA |
| I _O ¶ | V _{CC} = 5.5 V, | V _O = 2.5 V | -50 | -100 | -180 | -50 | -180 | -50 | mA |
| I _{CC} | A or B ports | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 2 | | 2 | 2 | mA |
| | | | Outputs low | | 32 | | 32 | 32 | |
| | | | Outputs disabled | | 2 | | 2 | 2 | |
| ΔI _{CC} # | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | 1 | | 1.5 | 1 | mA |
| | | | Outputs disabled | | 0.05 | | 0.05 | 0.05 | |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | | | 1.5 | | 1.5 | 1.5 | |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | | 3.5 | | | | | pF |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | | 9.5 | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54ABT16863, SN74ABT16863
 18-BIT BUS TRANSCEIVERS
 WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$ | | | SN54ABT16863 | | SN74ABT16863 | | UNIT |
|-----------|--|----------------|--|-----|-----|--------------|-----|--------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 1 | 2.2 | 3.2 | 1 | 3.7 | 1 | 3.5 | ns |
| t_{PHL} | | | 1 | 2.2 | 3.4 | 1 | 4.2 | 1 | 3.9 | |
| t_{PZH} | \overline{OEBA} or \overline{OEAB} | A or B | 1 | 2.9 | 4.5 | 1 | 5.7 | 1 | 5.4 | ns |
| t_{PZL} | | | 1 | 2.6 | 4.1 | 1 | 5.2 | 1 | 4.8 | |
| t_{PHZ} | \overline{OEBA} or \overline{OEAB} | A or B | 1.6 | 4.1 | 5.4 | 1.6 | 6.3 | 1.6 | 6 | ns |
| t_{PLZ} | | | 1.5 | 3.3 | 4.5 | 1.5 | 5.3 | 1.5 | 5 | |

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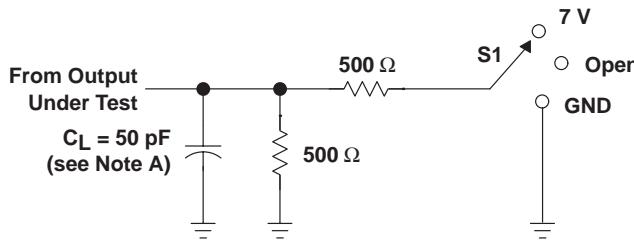


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**SN54ABT16863, SN74ABT16863
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS**

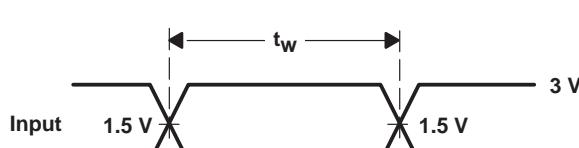
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PARAMETER MEASUREMENT INFORMATION

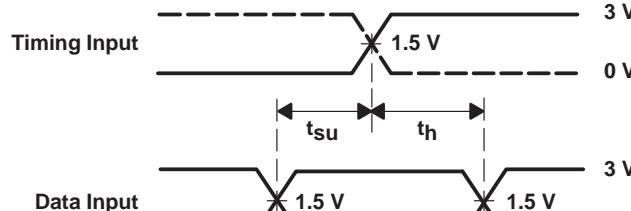


LOAD CIRCUIT

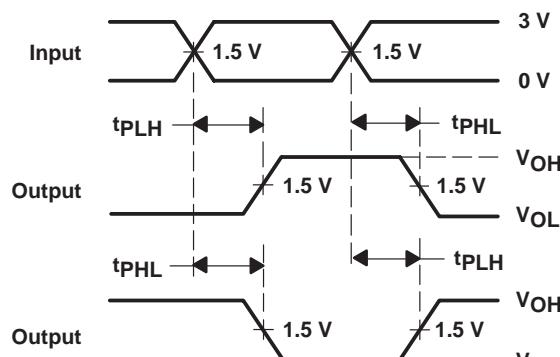
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



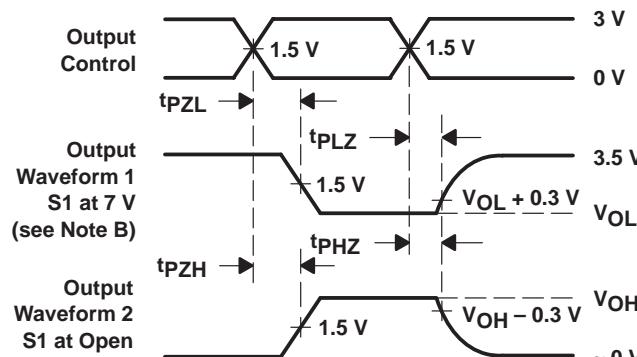
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

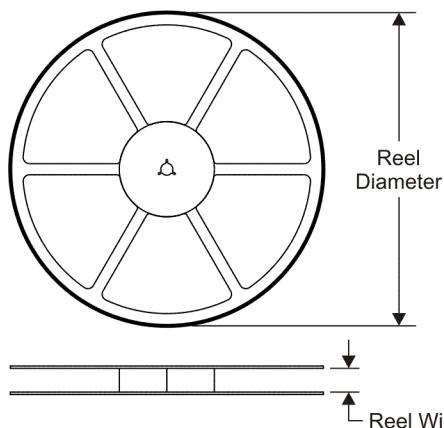
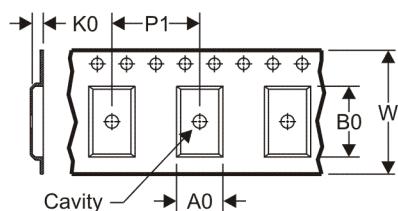
NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

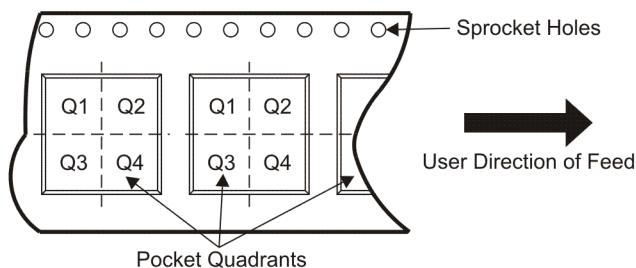
C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


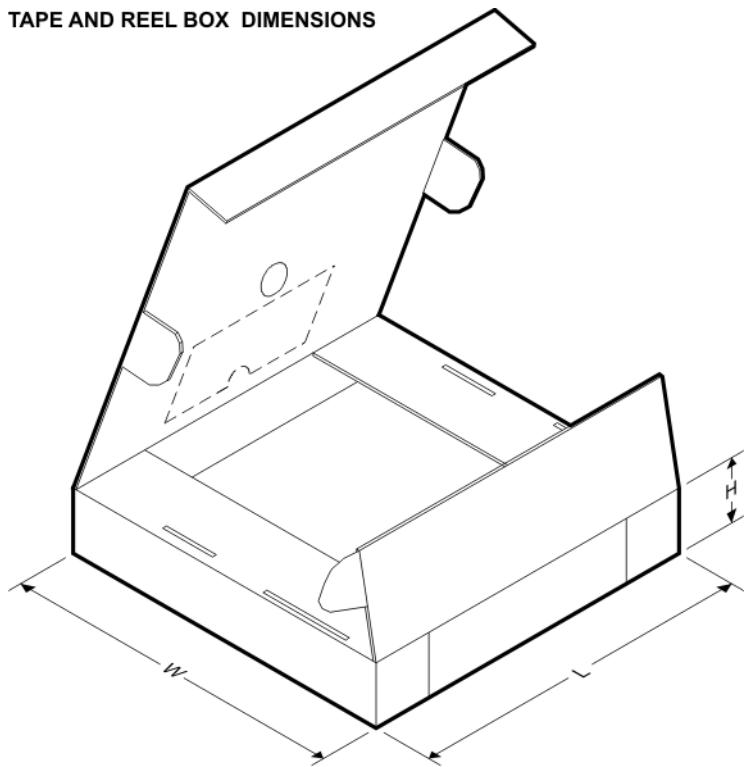
| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16863DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16863DLR | SSOP | DL | 56 | 1000 | 346.0 | 346.0 | 49.0 |

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74ABT16863DL | Active | Production | SSOP (DL) 56 | 20 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16863 |
| SN74ABT16863DL.B | Active | Production | SSOP (DL) 56 | 20 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16863 |
| SN74ABT16863DLR | Active | Production | SSOP (DL) 56 | 1000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16863 |
| SN74ABT16863DLR.B | Active | Production | SSOP (DL) 56 | 1000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ABT16863 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

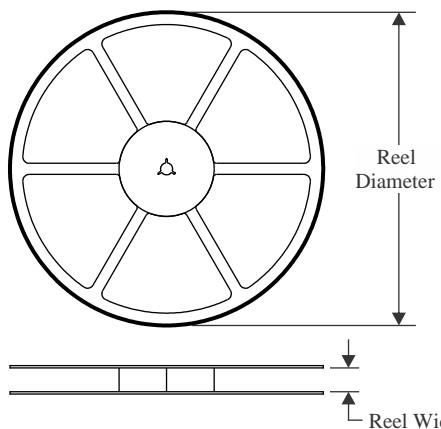
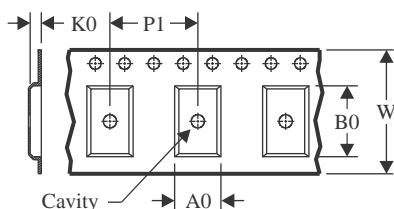
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

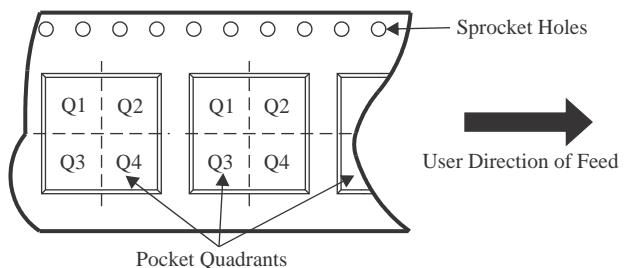
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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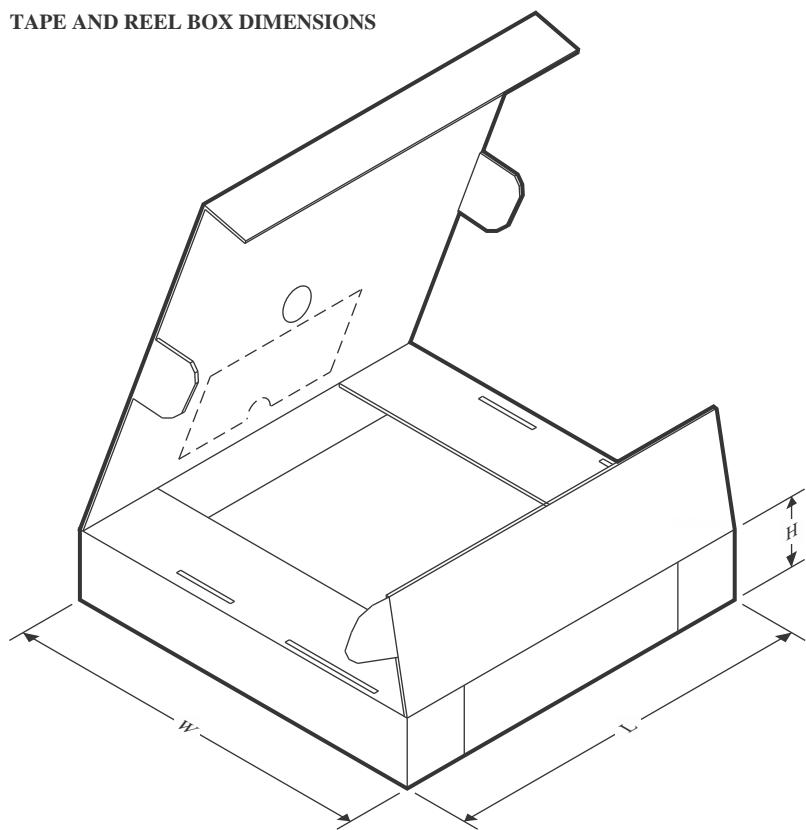
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


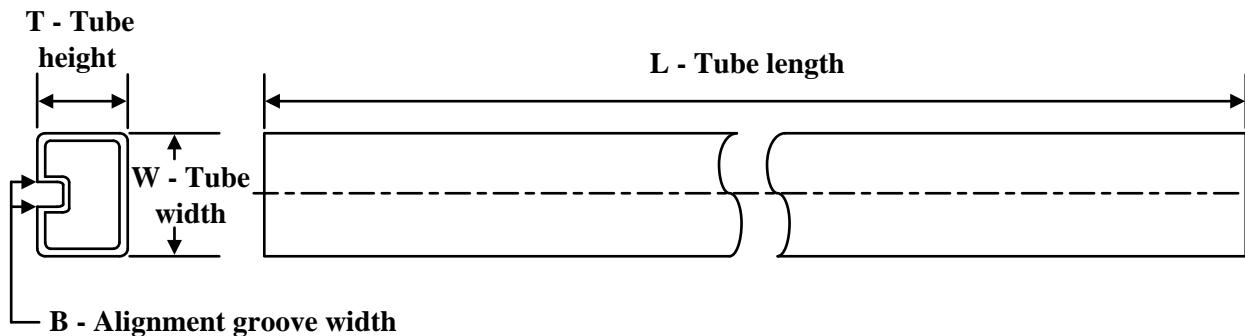
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16863DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16863DLR | SSOP | DL | 56 | 1000 | 356.0 | 356.0 | 53.0 |

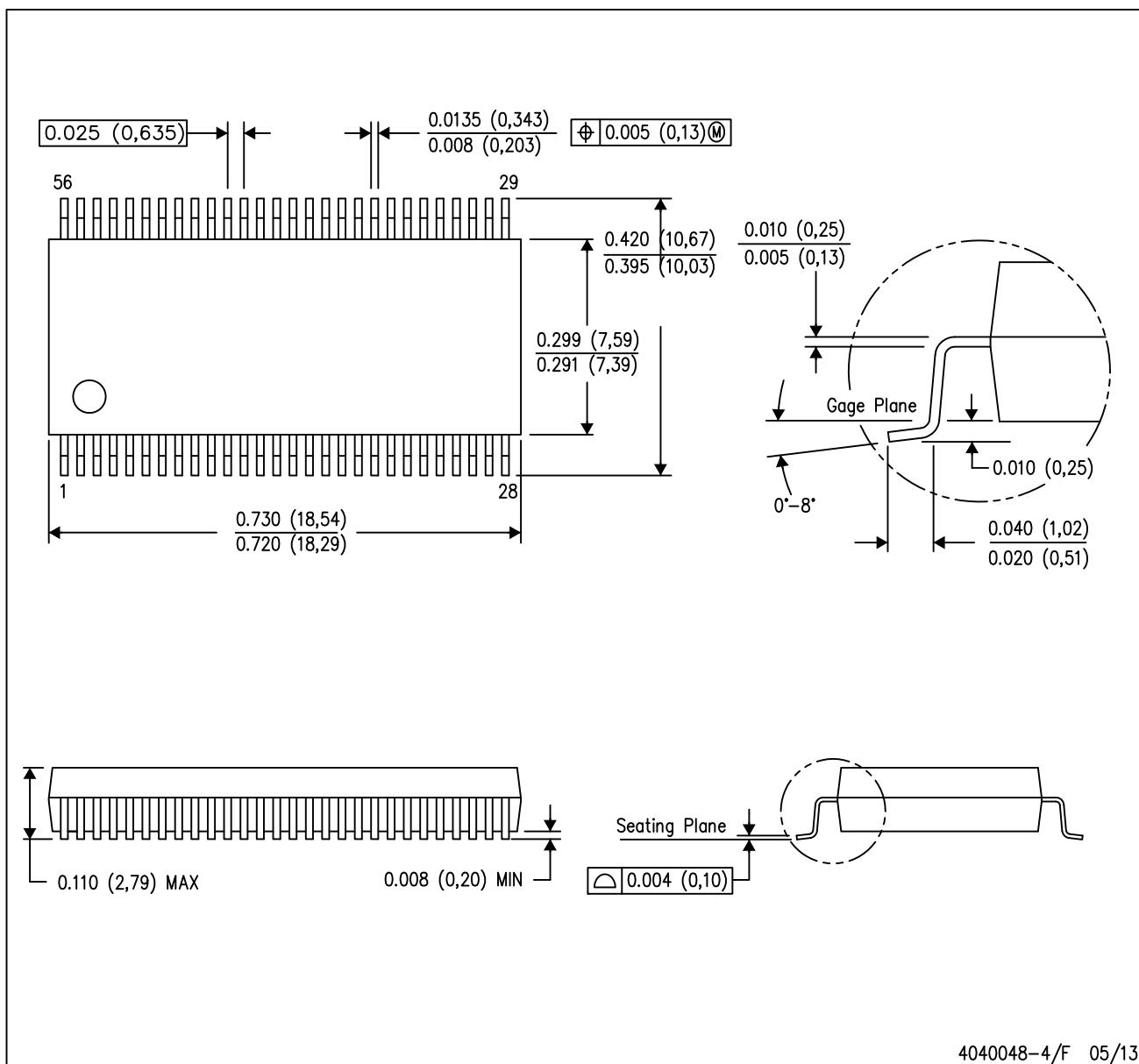
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μ m) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| SN74ABT16863DL | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |
| SN74ABT16863DL.B | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MO-118

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