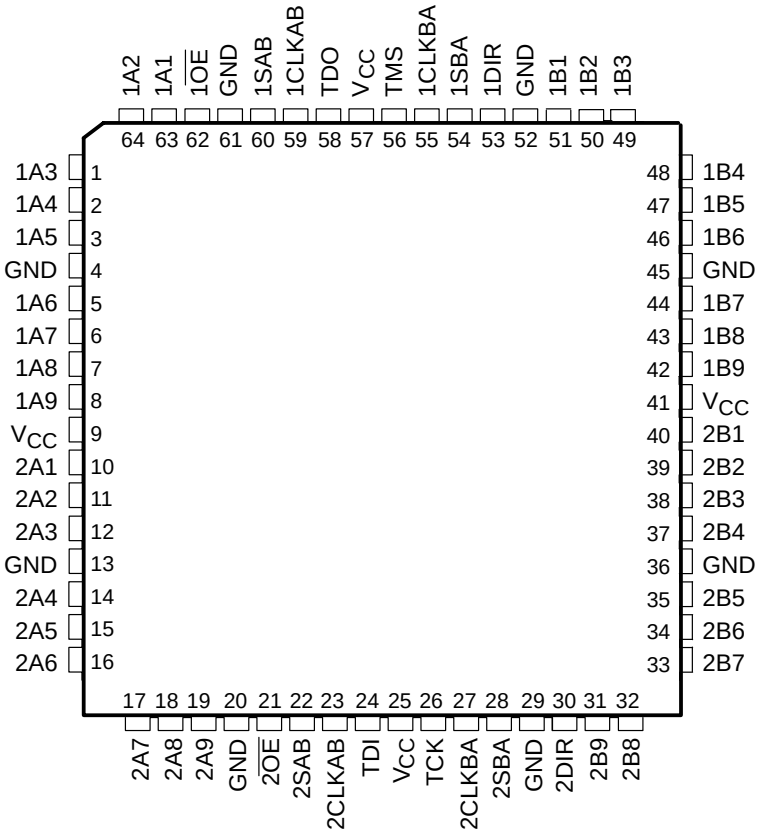
- **Member of the Texas Instruments Widebus™ Family**
- **Compatible With IEEE Std 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- **Includes D-Type Flip-Flops and Control Circuitry to Provide Multiplexed Transmission of Stored and Real-Time Data**
- **Two Boundary-Scan Cells Per I/O for Greater Flexibility**
- **SCOPE™ Instruction Set**
  - **IEEE Std 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudorandom Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**

PM PACKAGE
(TOP VIEW)



description

This scan test device with a 18-bit bus transceiver and register is a member of the Texas Instruments SCOPE™ testability IC family. This device supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the four-wire test access port (TAP) interface.

description (continued)

In the normal mode, this device is an 18-bit bus transceiver and register that allows for multiplexed transmission of data directly from the input bus or from the internal registers. It can be used either as two 9-bit transceivers or one 18-bit transceiver. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self-test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE bus transceivers and registers.

Transceiver function is controlled by output-enable ($\overline{OE}$) and direction (DIR) inputs. When $\overline{OE}$ is low, the transceiver is active and operates in the A-to-B direction when DIR is high or in the B-to-A direction when DIR is low. When $\overline{OE}$ is high, both the A and B outputs are in the high-impedance state, effectively isolating both buses.

Data flow is controlled by clock (CLKAB and CLKBA) and select (SAB and SBA) inputs. Data on the A bus is clocked into the associated registers on the low-to-high transition of CLKAB. When SAB is low, real-time A data is selected for presentation to the B bus (transparent mode). When SAB is high, stored A data is selected for presentation to the B bus (registered mode). The function of the CLKBA and SBA inputs mirrors that of CLKAB and SAB, respectively. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74ABT18646.

In the test mode, the normal operation of the SCOPE bus transceivers and registers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry can perform boundary scan test operations according to the protocol described in IEEE Std 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions, such as parallel signature analysis on data inputs and pseudorandom pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

ORDERING INFORMATION

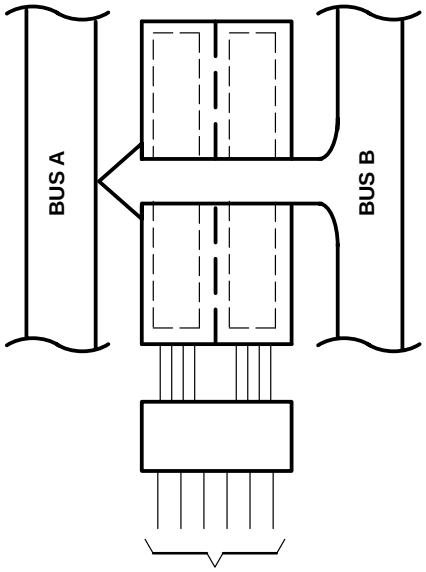
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	LQFP – PM	Tray	SN74ABT18646PM	ABT18646

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(normal mode, each 9-bit section)

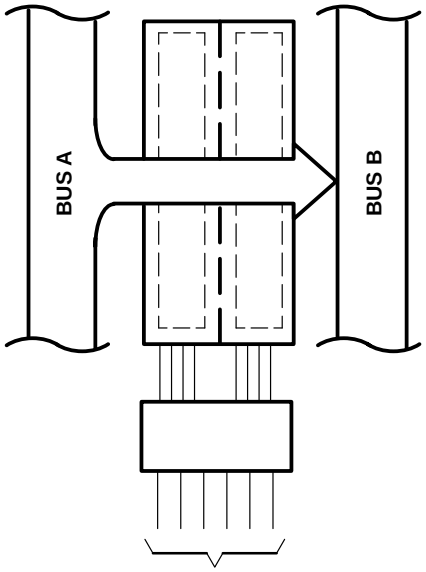
INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1–A9	B1–B9	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	L	L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	X	X	H	Output	Input disabled	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	L	X	H	X	Input disabled	Output	Stored A data to B bus

† The data output functions can be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



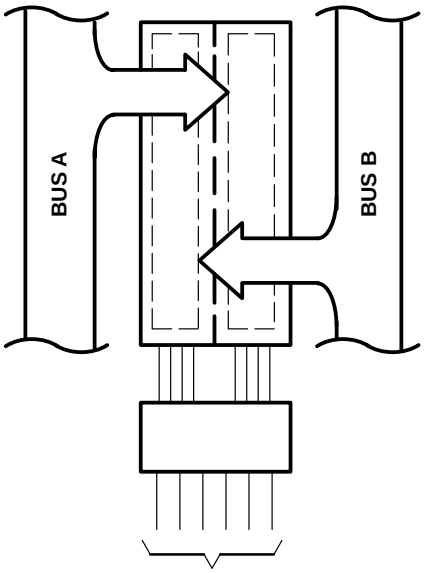
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



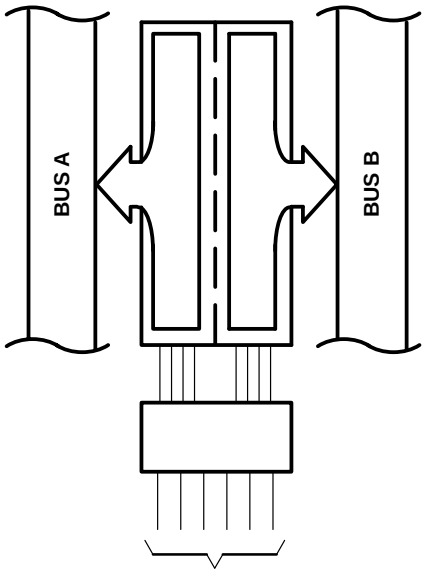
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

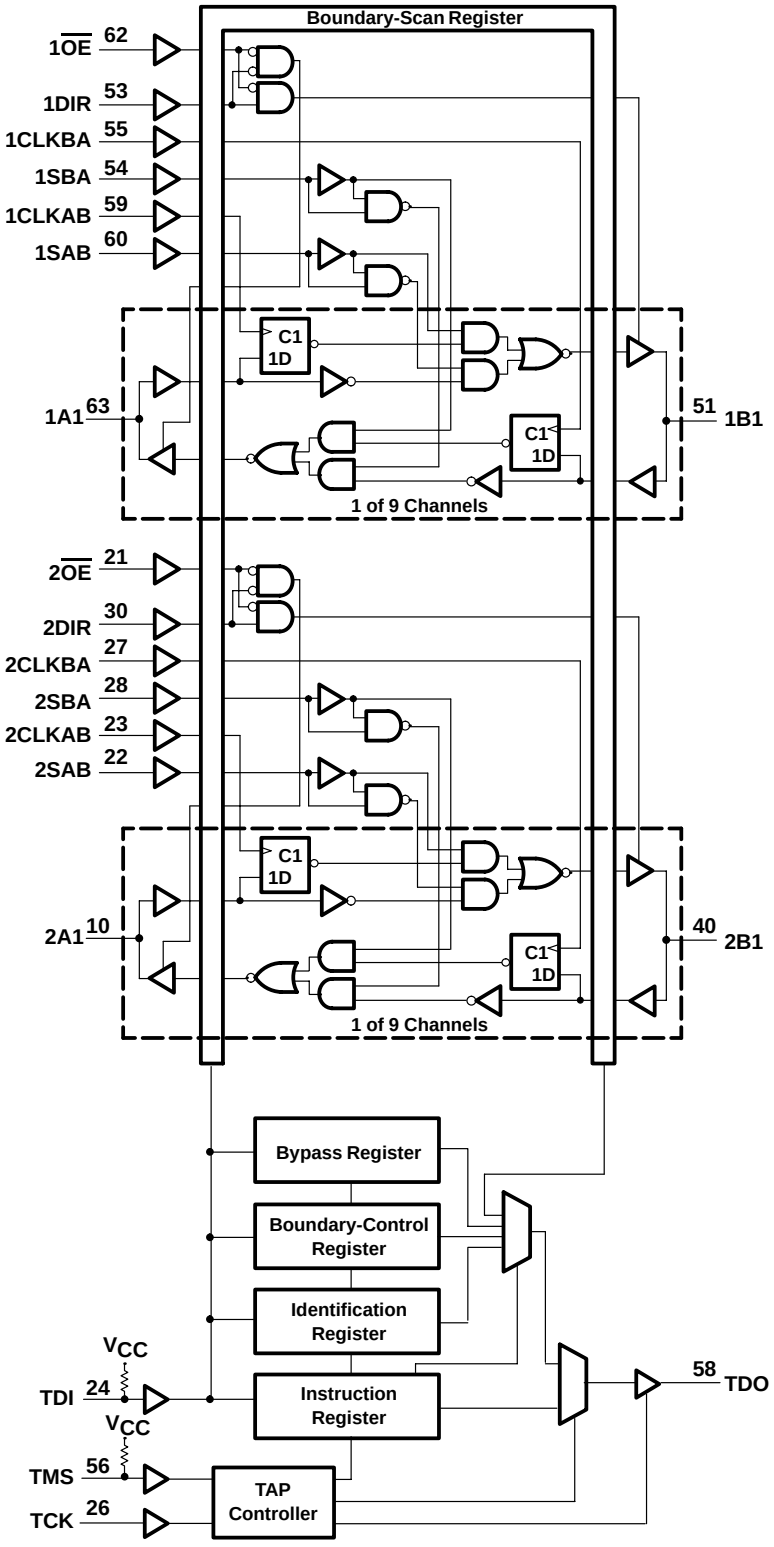


$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	H
L	H	L	X	H	X

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . –0.5 V to 7 V
I/O ports (see Note 1) . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 128 mA
Input clamp current, I_{IK} ($V_I < 0$) . . . . . –18 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . . 34°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10	ns/V
T_A	Operating free-air temperature	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			V
	V_{CC} = 4.5 V,	I_{OH} = –32 mA		2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 64 mA				0.55	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND	CLK, DIR, $\overline{OE}$, S, TCK			±1	µA
			A or B ports			±100	
I_{IH}	V_{CC} = 5.5 V,	V_I = V_{CC},	TDI, TMS			10	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = GND,	TDI, TMS			–150	µA
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.5 V				–50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 5.5 V				±100	µA
I_{CEX}	V_{CC} = 5.5 V,	V_O = 5.5 V,	Outputs high			50	µA
I_O§	V_{CC} = 5.5 V,	V_O = 2.5 V		–50		–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high			5.5	mA
			Outputs low			38¶	
			Outputs disabled			5	
ΔI_{CC}#	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			2	mA
C_i	V_I = 2.5 V or 0.5 V,		Control inputs		3		pF
C_{io}	V_O = 2.5 V or 0.5 V,		A or B ports		10		pF
C_o	V_O = 2.5 V or 0.5 V,		TDO		8		pF

NOTE 4: Preliminary specifications based on SPICE analysis
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ If both A and B ports are low, I_{CCL} is 76 mA.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	CLKAB or CLKBA		100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low	4		ns
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑	4.5		ns
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑	0		ns

NOTE 4: Preliminary specifications based on SPICE analysis

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency	TCK		50	MHz
t_w	Pulse duration	TCK high or low	8		ns
t_{su}	Setup time	A, B, CLK, DIR, $\overline{OE}$, or S before TCK↑	4.5		ns
		TDI before TCK↑	7.5		
		TMS before TCK↑	3		
t_h	Hold time	A or B after TCK↑	0.5		ns
		CLK, DIR, $\overline{OE}$, or S after TCK↑	0		
		TDI after TCK↑	0.5		
		TMS after TCK↑	0.5		
t_d	Delay time	Power up to TCK↑	50		ns
t_r	Rise time	V_{CC} power up	1		µs

NOTE 4: Preliminary specifications based on SPICE analysis

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	CLKAB or CLKBA		100		MHz
t_{PLH}	A or B	B or A	2	5.4	ns
t_{PHL}			2	6.6	
t_{PLH}	CLKAB or CLKBA	B or A	2.5	8	ns
t_{PHL}			2.5	7.4	
t_{PLH}	SAB or SBA	B or A	2	7.5	ns
t_{PHL}			2	8	
t_{PZH}	DIR	B or A	2	8	ns
t_{PZL}			3	9.1	
t_{PZH}	$\overline{OE}$	B or A	2.5	8.6	ns
t_{PZL}			3	9.3	
t_{PHZ}	DIR	B or A	3.5	11.1	ns
t_{PLZ}			3	8.8	
t_{PHZ}	$\overline{OE}$	B or A	3.5	10.5	ns
t_{PLZ}			2	8.5	

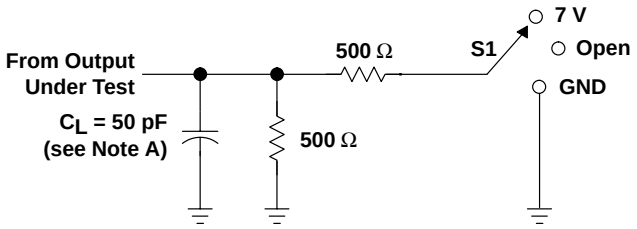
NOTE 4: Preliminary specifications based on SPICE analysis

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Note 4 and Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	TCK		50		MHz
t_{PLH}	TCK↓	A or B	2.5	13.5	ns
t_{PHL}			2.5	12.5	
t_{PLH}	TCK↓	TDO	2	6.5	ns
t_{PHL}			2	6.5	
t_{PZH}	TCK↓	A or B	4.5	13.8	ns
t_{PZL}			5	14.5	
t_{PZH}	TCK↓	TDO	2	7	ns
t_{PZL}			3	7.5	
t_{PHZ}	TCK↓	A or B	4	17	ns
t_{PLZ}			3	16	
t_{PHZ}	TCK↓	TDO	3	9	ns
t_{PLZ}			3	7.5	

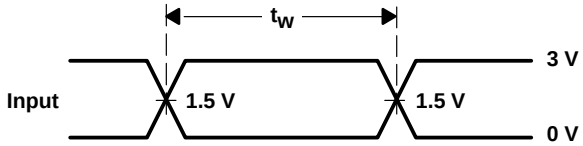
NOTE 4: Preliminary specifications based on SPICE analysis

PARAMETER MEASUREMENT INFORMATION

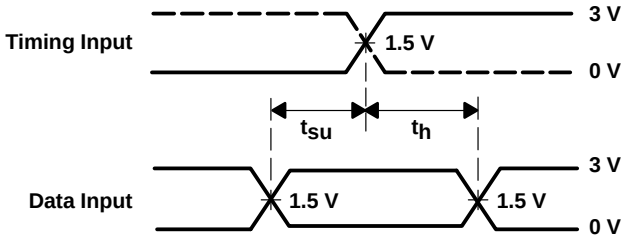


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

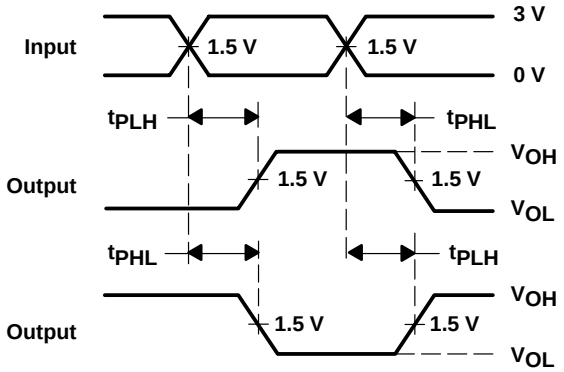
LOAD CIRCUIT



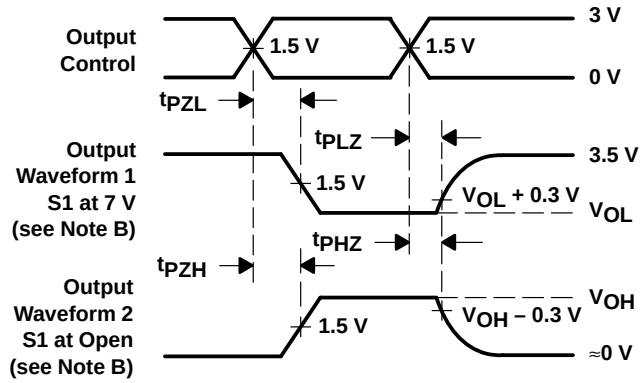
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT18646PM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18646
SN74ABT18646PM.B	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18646
SN74ABT18646PMG4	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18646
SN74ABT18646PMG4.B	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABT18646

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

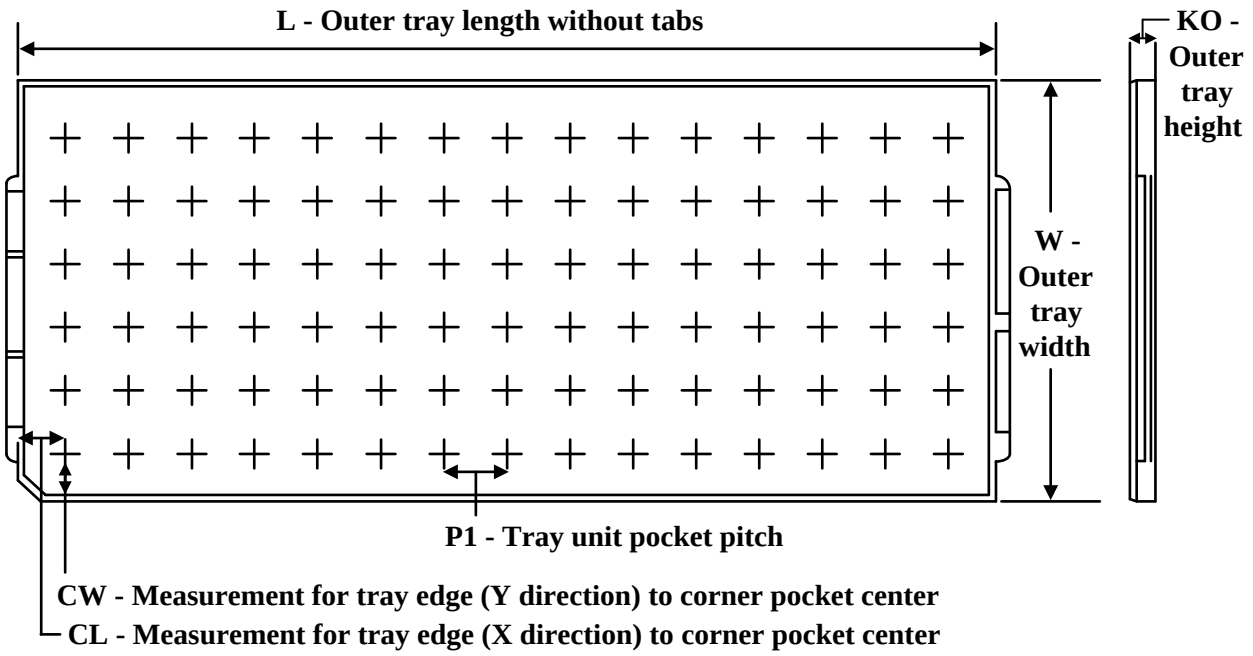
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

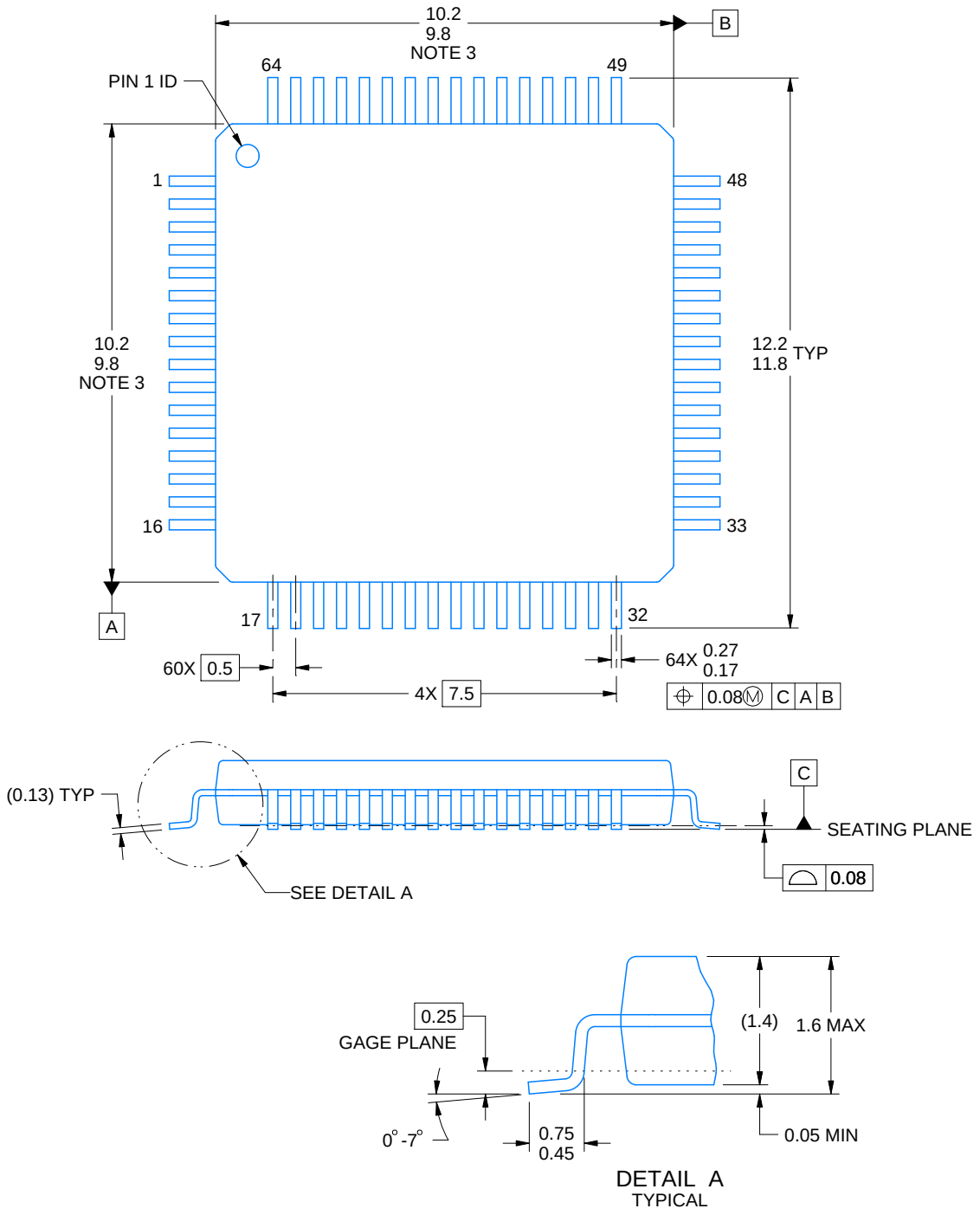
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74ABT18646PM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18646PM.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18646PMG4	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
SN74ABT18646PMG4.B	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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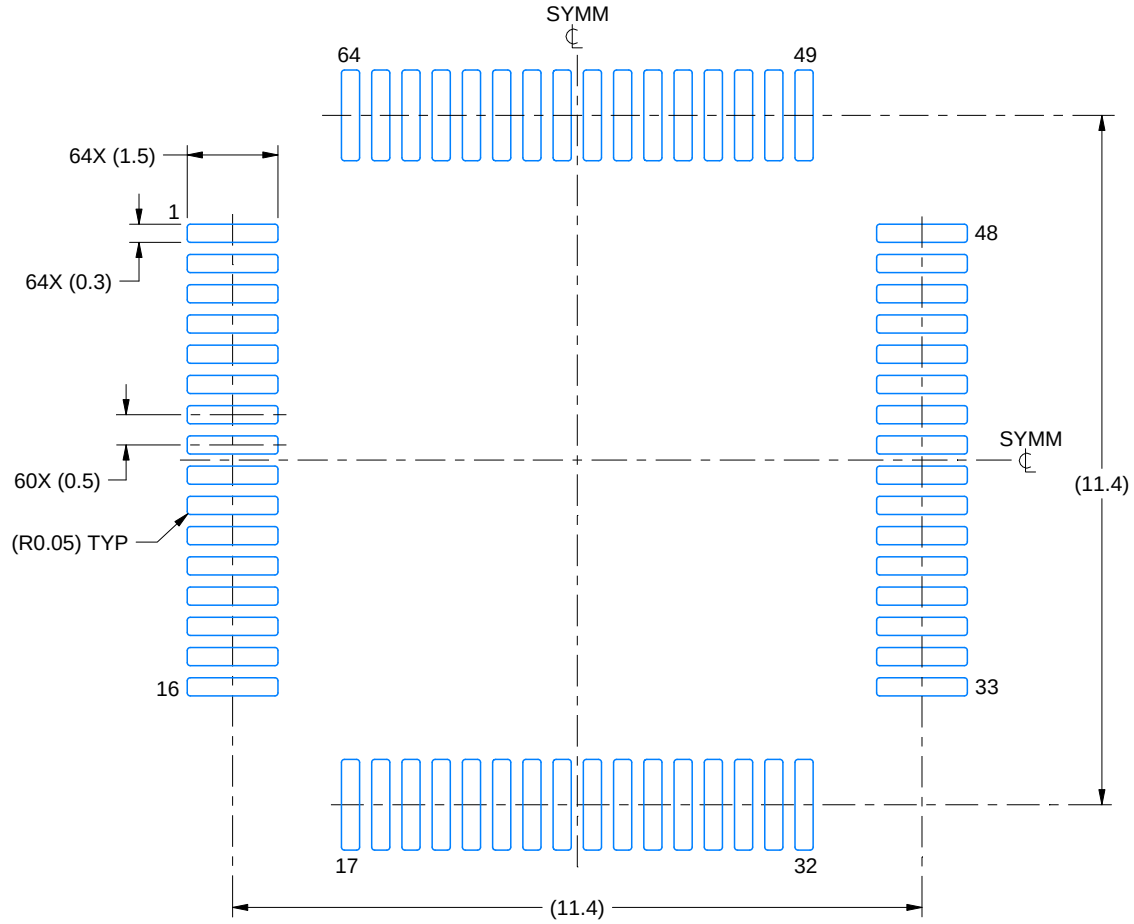
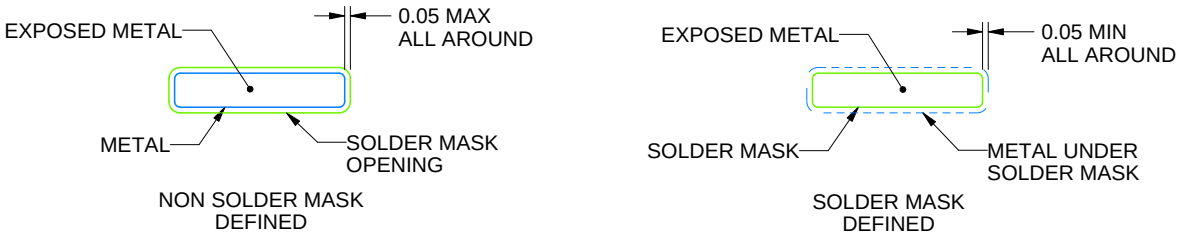
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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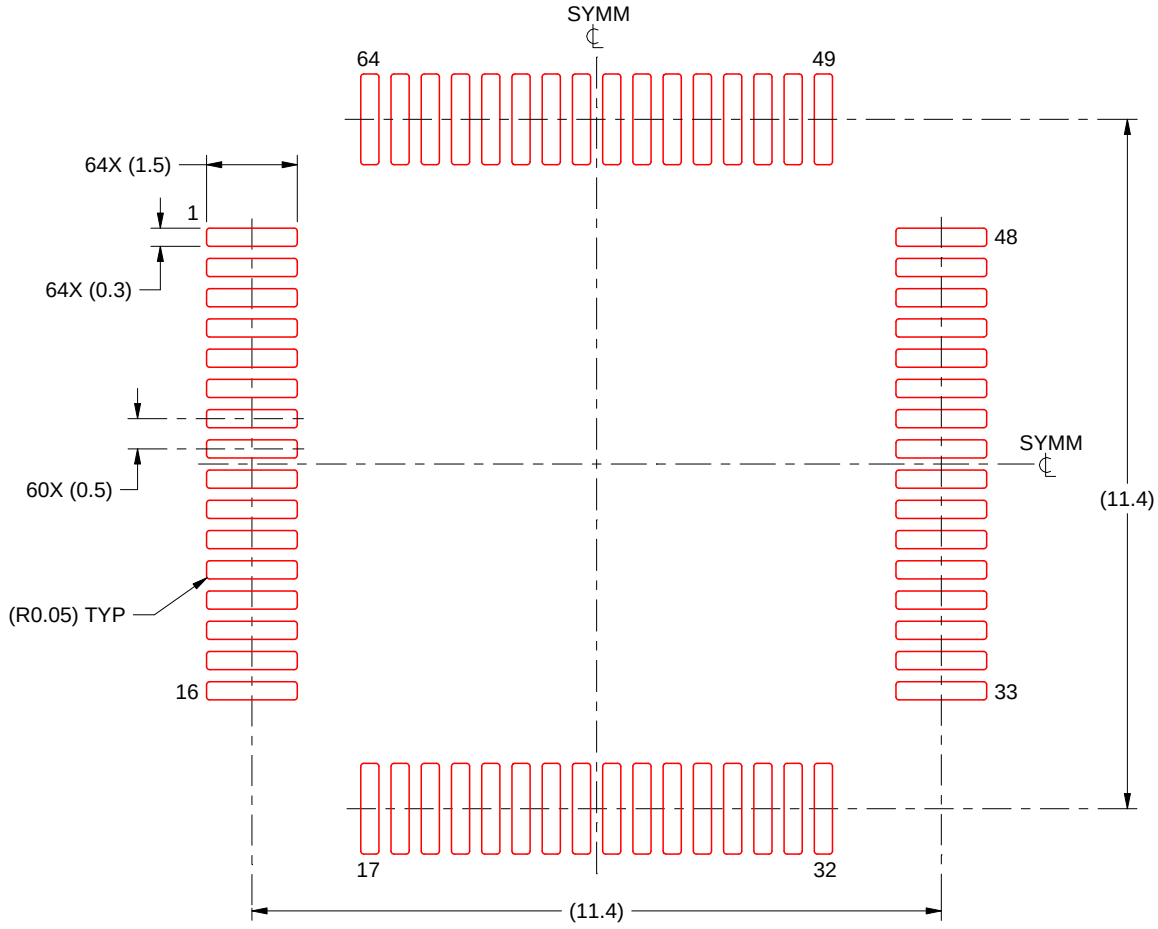
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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