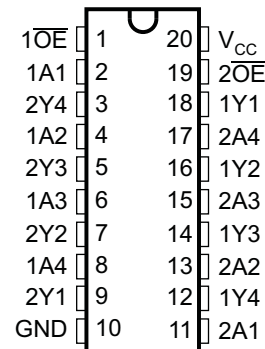


FEATURES

- **Controlled Baseline**
– One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5 V, T_A = 25^\circ C$**
- **High-Drive Outputs (–24-mA I_{OH} , 48-mA I_{OL})**
- **Packaged in Shrink Small-Outline (DB) Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DB PACKAGE
(TOP VIEW)



DESCRIPTION

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the SN54ABT240, SN74ABT240A, SN54ABT241, and SN74ABT241A, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary OE and \overline{OE} inputs.

The SN74ABT244A is organized as two 4-bit buffers/line drivers with separate \overline{OE} inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT244 is characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SSOP – DB Tape and reel	SN74ABT244AMDBREP	ABT244AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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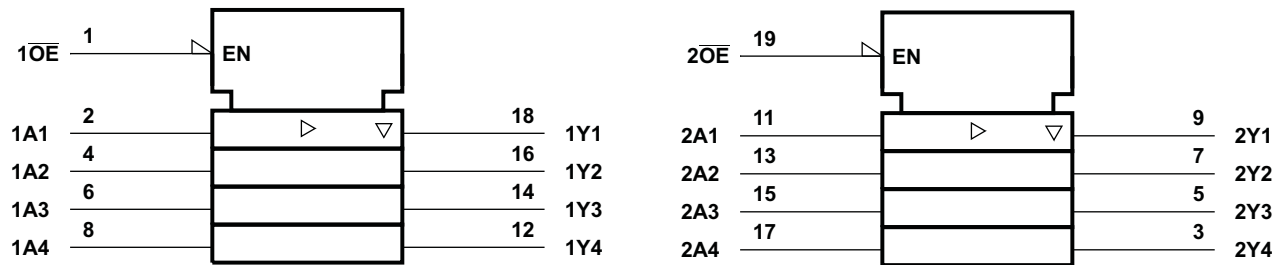
SN74ABT244A-EP OCTAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

SGBS312A—JULY 2006—REVISED JULY 2006

**FUNCTION TABLE
(EACH BUFFER)**

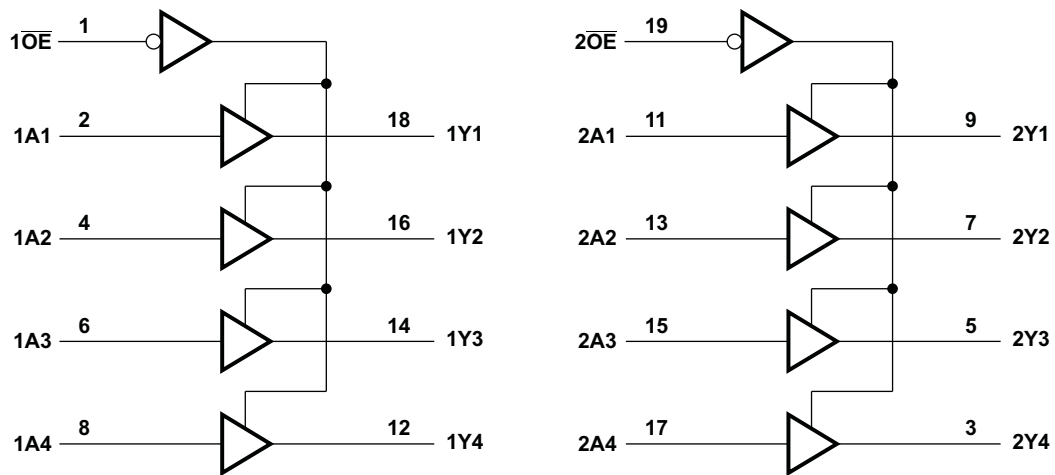
INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I	Input voltage range ⁽²⁾	-0.5	7	V
V_O	Voltage range applied to any output in the high or power-off state	-0.5	5.5	V
I_O	Current into any output in the low state		96	mA
I_{IK}	Input clamp current	$V_I < 0$	-18	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
θ_{JA}	Package thermal impedance ⁽³⁾		115	°C/W
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		-24	mA
I_{OL}	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
	Outputs enabled			
T_A	Operating free-air temperature	-55	125	°C

- (1) Unused inputs must be held high or low to prevent them from floating.

SN74ABT244A-EP

OCTAL BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SGBS312A–JULY 2006–REVISED JULY 2006

Electrical Characteristics⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			MIN	MAX	UNIT
		MIN	TYP ⁽²⁾	MAX			
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2	-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5	V	
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		
	V _{CC} = 4.5 V, I _{OH} = -24 mA	2			2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA			0.55	0.55	V	
V _{hys}			100			mV	
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1	±1	μA	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V			10	10	μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.5 V			-10	-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 5.5 V			±100		μA	
I _{CEX}	V _{CC} = 5.5 V, Outputs high			50	50	μA	
I _O ⁽³⁾	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	1	250	250	μA	
		Outputs low	24	30	30	mA	
		Outputs disabled	0.5	250	250	μA	
ΔI _{CC} ⁽⁴⁾	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled	1.5	1.5	mA	
		Outputs disabled	0.05	0.05			
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5	1.5		
C _i	V _I = 2.5 V or 0.5 V		3.5			pF	
C _o	V _O = 2.5 V or 0.5 V		7.5			pF	

(1) On products compliant to MIL-PRF-38535, this parameter does not apply.

(2) All typical values are at V_{CC} = 5 V.

(3) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

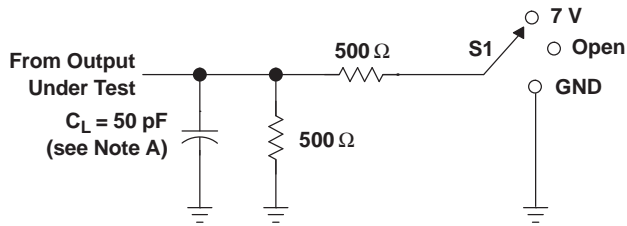
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted)

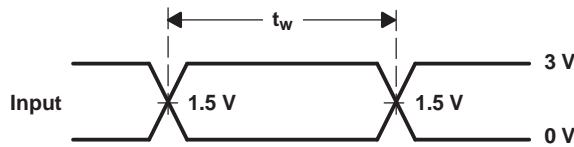
(see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t _{PLH}	A	Y	1	2.6	4.1	1	5.3	ns
t _{PHL}			1	2.9	4.2	1	5	
t _{PZH}	\overline{OE}	Y	1.1	3.1	4.6	0.8	5.7	ns
t _{PZL}			2.1	4.1	5.6	1.2	7.9	
t _{PHZ}	\overline{OE}	Y	2.1	4.1	5.6	1.2	7.6	ns
t _{PLZ}			1.5	3.7	5.6	1	7.9	

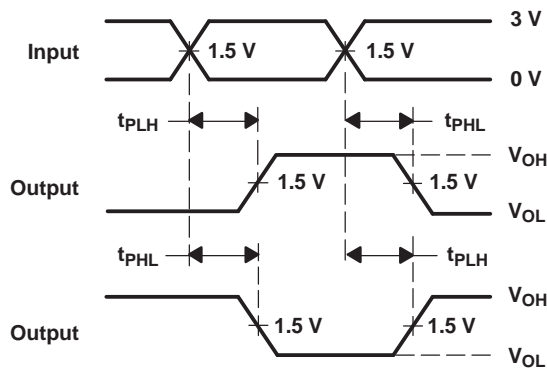
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

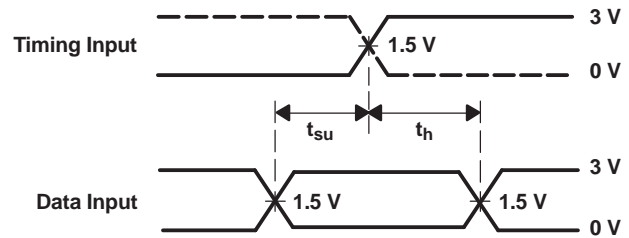


VOLTAGE WAVEFORMS
PULSE DURATION

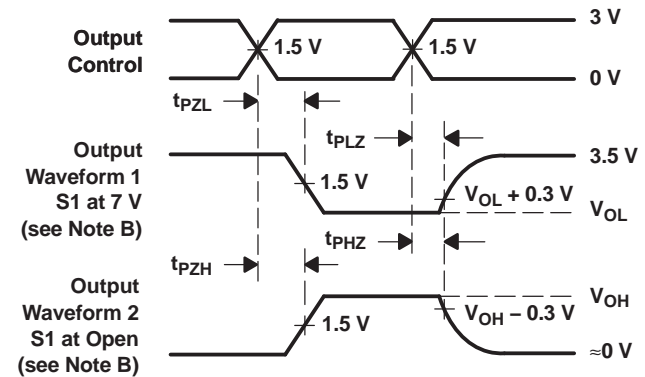


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABT244AMDBREP	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT244AMEP
V62/06667-01XE	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ABT244AMEP

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74ABT244A-EP :

- Catalog : [SN74ABT244A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT244AMDBREP	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT244AMDBREP	SSOP	DB	20	2000	353.0	353.0	32.0

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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