

SN54ABTH162260, SN74ABTH162260 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

SCBS240D – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABTH162260 . . . WD PACKAGE
SN74ABTH162260 . . . DL PACKAGE
(TOP VIEW)

OE $\overline{A}$	1	56	OE2B
LE1B	2	55	LEA2B
2B3	3	54	2B4
GND	4	53	GND
2B2	5	52	2B5
2B1	6	51	2B6
V_{CC}	7	50	V_{CC}
A1	8	49	2B7
A2	9	48	2B8
A3	10	47	2B9
GND	11	46	GND
A4	12	45	2B10
A5	13	44	2B11
A6	14	43	2B12
A7	15	42	1B12
A8	16	41	1B11
A9	17	40	1B10
GND	18	39	GND
A10	19	38	1B9
A11	20	37	1B8
A12	21	36	1B7
V_{CC}	22	35	V_{CC}
1B1	23	34	1B6
1B2	24	33	1B5
GND	25	32	GND
1B3	26	31	1B4
LE2B	27	30	LEA1B
SEL	28	29	OE1B

description

The 'ABTH162260 are 12-bit to 24-bit multiplexed D-type latches used in applications where two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing of address and data information in microprocessor or bus-interface applications. These devices are also useful in memory-interleaving applications.

Three 12-bit I/O ports (A1–A12, 1B1–1B12, and 2B1–2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OE A}$) inputs control the bus-transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B-port outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.



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**TEXAS
INSTRUMENTS**

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SN54ABTH162260, SN74ABTH162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCHES

WITH SERIES-DAMPING RESISTORS AND 3-STATE OUTPUTS

SCBS240D – JUNE 1992 – REVISED MAY 1997

description (continued)

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABTH162260 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABTH162260 is characterized for operation from -40°C to 85°C .

Function Tables

B TO A ($\overline{OEB} = \text{H}$)

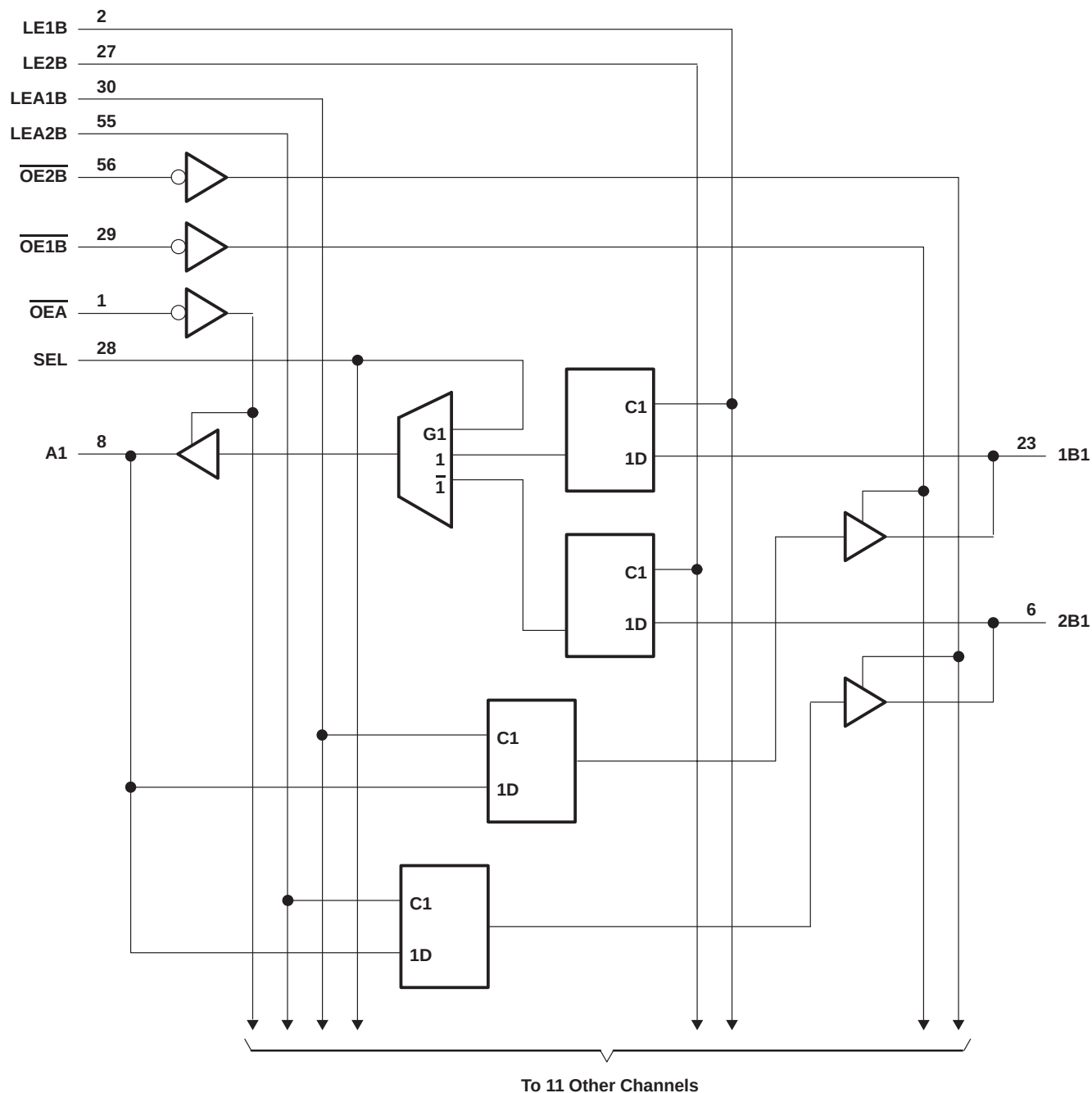
INPUTS						OUTPUT A
1B	2B	SEL	LE1B	LE2B	$\overline{OEA}$	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

A TO B ($\overline{OEA} = \text{H}$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	$\overline{OE1B}$	$\overline{OE2B}$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
L	L	H	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

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SCBS240D – JUNE 1992 – REVISED MAY 1997

logic diagram (positive logic)



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SCBS240D – JUNE 1992 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH162260 (A port)	96 mA
SN74ABTH162260 (A port)	128 mA
B port	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH162260		SN74ABTH162260		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
			12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

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SCBS240D – JUNE 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A = 25°C			SN54ABTH162260		SN74ABTH162260		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2			–1.2		–1.2		V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA		2.5			2.5		2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA		3			3		3		
		V _{CC} = 4.5 V	I _{OH} = –24 mA	2			2				
			I _{OH} = –32 mA	2*					2		
V _{OL}	A port	V _{CC} = 4.5 V	I _{OL} = 48 mA	0.55			0.55				V
			I _{OL} = 64 mA	0.55*					0.55		
	B port		I _{OL} = 12 mA	0.8			0.8		0.8		
V _{hys}				100							mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1			±1		±1		μA
	A or B ports	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND		±20			±20		±20		
I _I (hold)	A or B ports	V _{CC} = 4.5 V	V _I = 0.8 V						100		μA
			V _I = 2 V						–100		
I _{OZPU} ‡		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{OZPD} ‡		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE}$ = X		±50			±50		±50		μA
I _{OZH} §		V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE}$ ≥ 2 V		10			10		10		μA
I _{OZL} §		V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE}$ ≥ 2 V		–10			–10		–10		μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100					±100		μA
I _{CEX}	Outputs high	V _{CC} = 5.5 V, V _O = 5.5 V		50			50		50		μA
I _O ¶		V _{CC} = 5.5 V, V _O = 2.5 V		–50	–100	–225	–50	–225	–50	–225	mA
I _{CC}	Outputs high	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		1.5			1.5		1.5		mA
	Outputs low			63			63		63		
	Outputs disabled			1			1		1		
ΔI _{CC} #		V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1			1.5		1		mA
C _i		V _I = 2.5 V or 0.5 V		3							pF
C _O		V _O = 2.5 V or 0.5 V		11.5							pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized but not tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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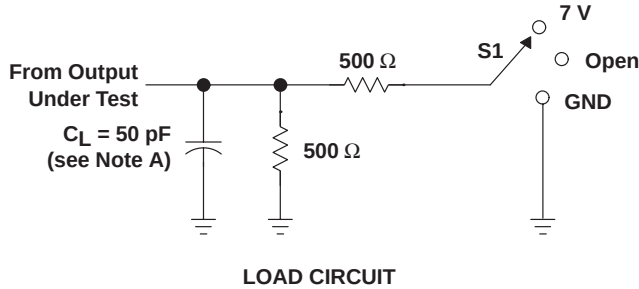
timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		V _{CC} = 5 V, T _A = 25°C		SN54ABTH162260		SN74ABTH162260		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high	3.3		3.3		3.3		ns
t _{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B↓	1.5		1.5		1.5		ns
t _h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B↓	1		1		1		ns

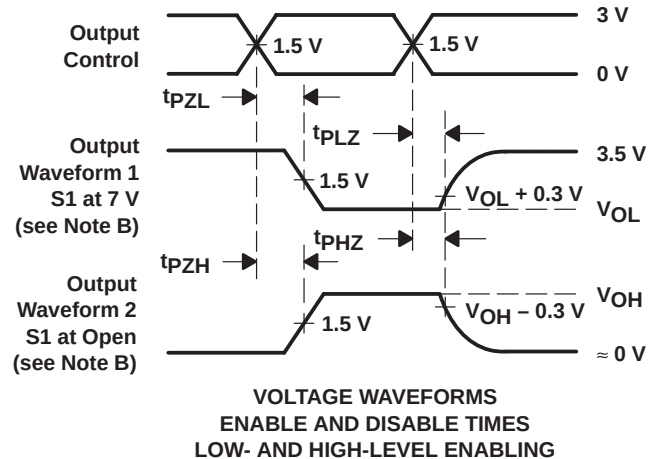
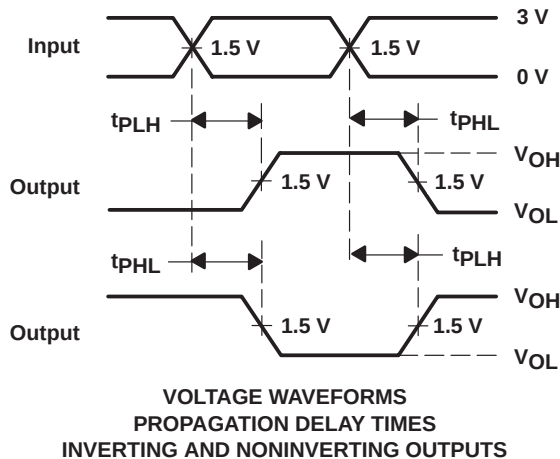
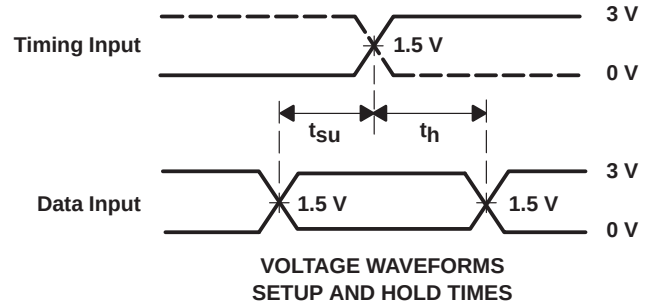
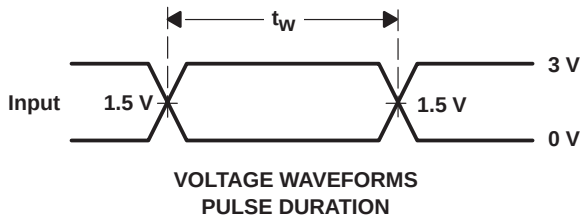
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, T _A = 25°C			SN54ABTH162260		SN74ABTH162260		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	B	1.4	3.6	5.2	1.4	6.3	1.4	6.1	ns
t _{PHL}			2.7	4.8	6.4	2.7	7.4	2.7	7.1	
t _{PLH}	B	A	1.6	3.6	5.2	1.6	6.4	1.6	6	ns
t _{PHL}			1.7	3.8	5.5	1.7	6.5	1.7	6.2	
t _{PLH}	LE	A	1.8	3.9	5.3	1.8	6.6	1.8	6.3	ns
t _{PHL}			2.3	4.1	5.4	2.3	6.1	2.3	5.8	
t _{PLH}	LE	B	1.6	3.7	5.4	1.6	6.4	1.6	6.1	ns
t _{PHL}			2.8	4.9	6.4	2.8	7.5	2.8	7.1	
t _{PLH}	SEL (1B)	A	1.5	3.6	5	1.5	5.9	1.5	5.6	ns
t _{PHL}			1.8	3.5	4.8	1.8	5.2	1.8	5	
t _{PLH}	SEL (2B)	A	1.2	3.6	5.1	1.2	6.5	1.2	6.3	ns
t _{PHL}			1.7	4	5.5	1.7	6.5	1.7	6.2	
t _{PZH}	$\overline{\text{OE}}$	A	1.1	3.5	5.2	1.1	6.5	1.1	6.3	ns
t _{PZL}			2.1	4.2	5.7	2.1	6.6	2.1	6.5	
t _{PZH}	$\overline{\text{OE}}$	B	1	3.4	4.9	1	6.4	1	6.3	ns
t _{PZL}			2.9	5.5	6.8	2.9	8.3	2.9	8.2	
t _{PHZ}	$\overline{\text{OE}}$	A	2.5	4.5	5.9	2.5	6.9	2.5	6.7	ns
t _{PLZ}			1.8	3.4	4.8	1.8	5.6	1.8	5.2	
t _{PHZ}	$\overline{\text{OE}}$	B	2.1	4.4	5.7	2.1	7.7	2.1	7.5	ns
t _{PLZ}			1.7	3.9	5.4	1.7	6.3	1.7	6.2	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ABTH162260DLRG4	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260
74ABTH162260DLRG4.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260
SN74ABTH162260DL	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260
SN74ABTH162260DL.B	Active	Production	SSOP (DL) 56	20 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260
SN74ABTH162260DLR	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260
SN74ABTH162260DLR.B	Active	Production	SSOP (DL) 56	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH162260

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

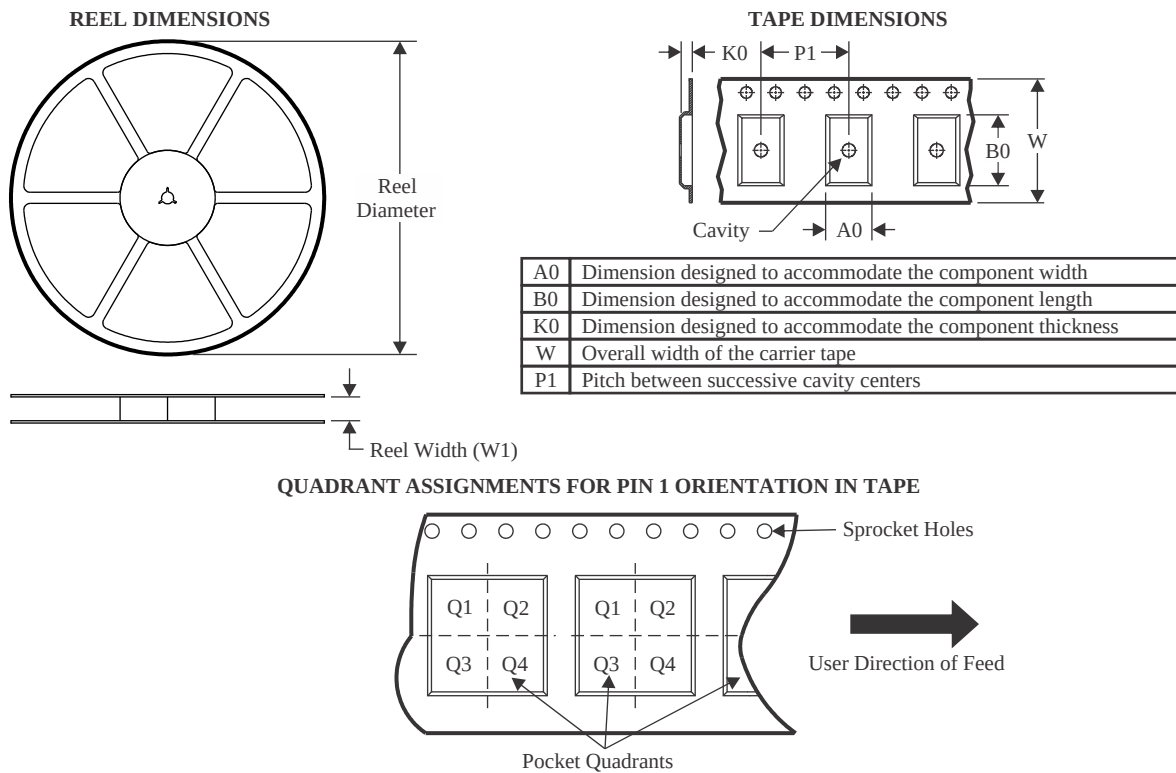
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ABTH162260DLRG4	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN74ABTH162260DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ABTH162260DLRG4	SSOP	DL	56	1000	356.0	356.0	53.0
SN74ABTH162260DLR	SSOP	DL	56	1000	356.0	356.0	53.0

TUBE

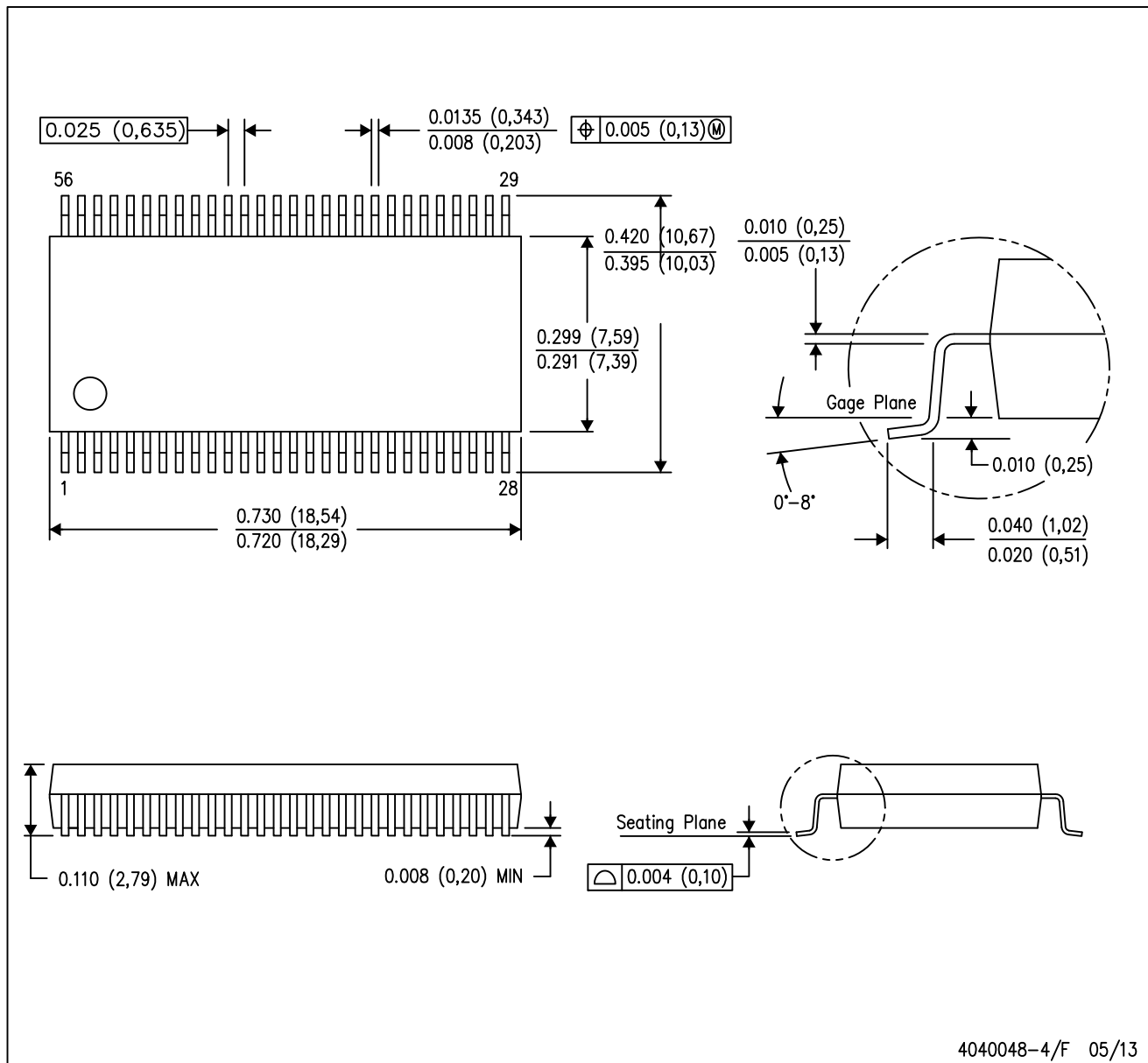


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABTH162260DL	DL	SSOP	56	20	473.7	14.24	5110	7.87
SN74ABTH162260DL.B	DL	SSOP	56	20	473.7	14.24	5110	7.87

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

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