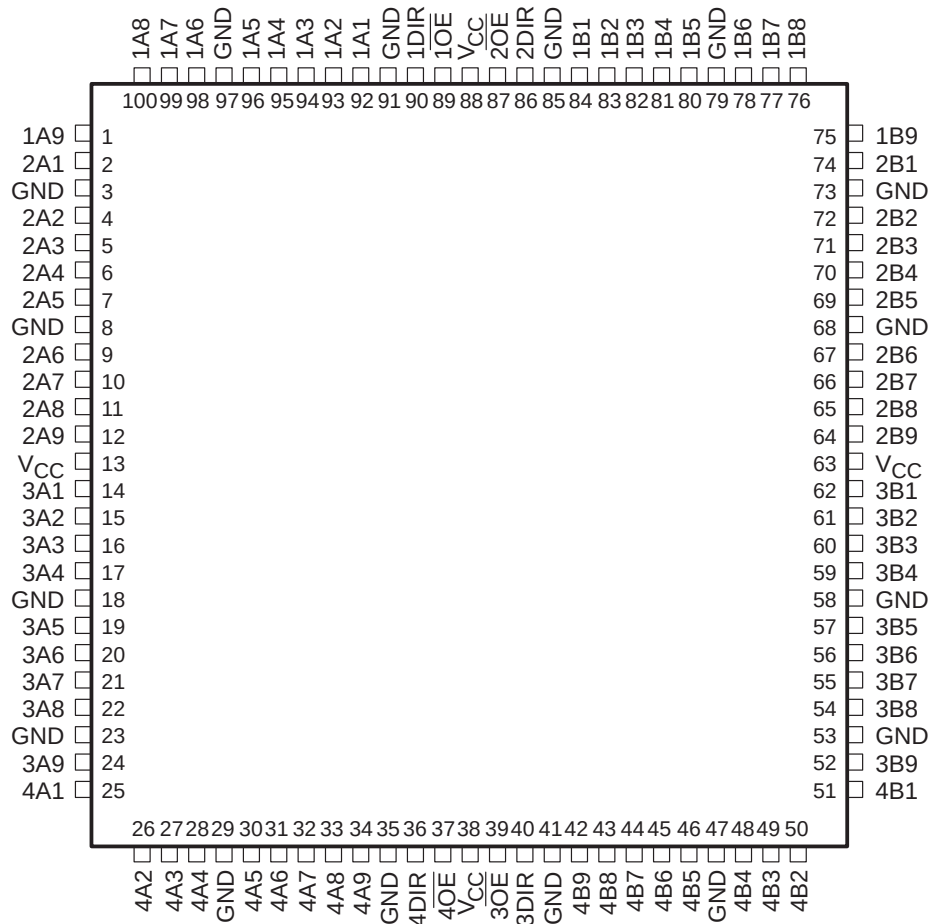


SN54ABTH32245, SN74ABTH32245 36-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus+™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Released as DSCC SMD 5962-9557701NXD
- PZ Package Qualified for Military Per MIL-PRF-38535 (QML)
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include 100-Pin Plastic Thin Quad Flat (PZ) Package With $14 \times 14\text{-mm}$ Body Using 0.5-mm Lead Pitch and Space-Saving 100-Pin Ceramic Quad Flat (HS) Package†

'ABTH32245 . . . PZ PACKAGE
(TOP VIEW)



† The HS package is not production released.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ and EPIC-II B are trademarks of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

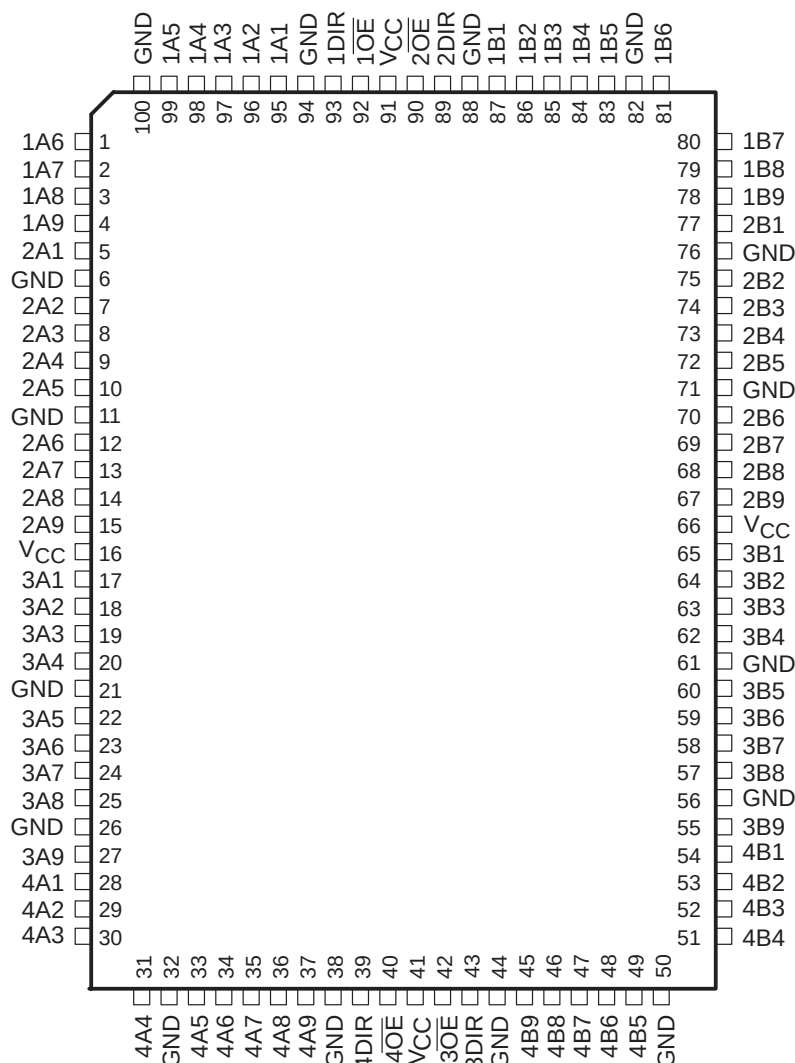
SN54ABTH32245, SN74ABTH32245

36-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

SN54ABTH32245 . . . HS PACKAGE†
(TOP VIEW)



† For HS package availability, please contact the factory or your local TI Field Sales Office.

description

The 'ABTH32245 are 36-bit (quad 9-bit) noninverting 3-state transceivers designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

These devices can be used as four 9-bit transceivers, two 18-bit transceivers, or one 36-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) inputs. The output-enable ($\overline{OE}$) inputs can be used to disable the device so that the buses are effectively isolated.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or floating data inputs at a valid logic level.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

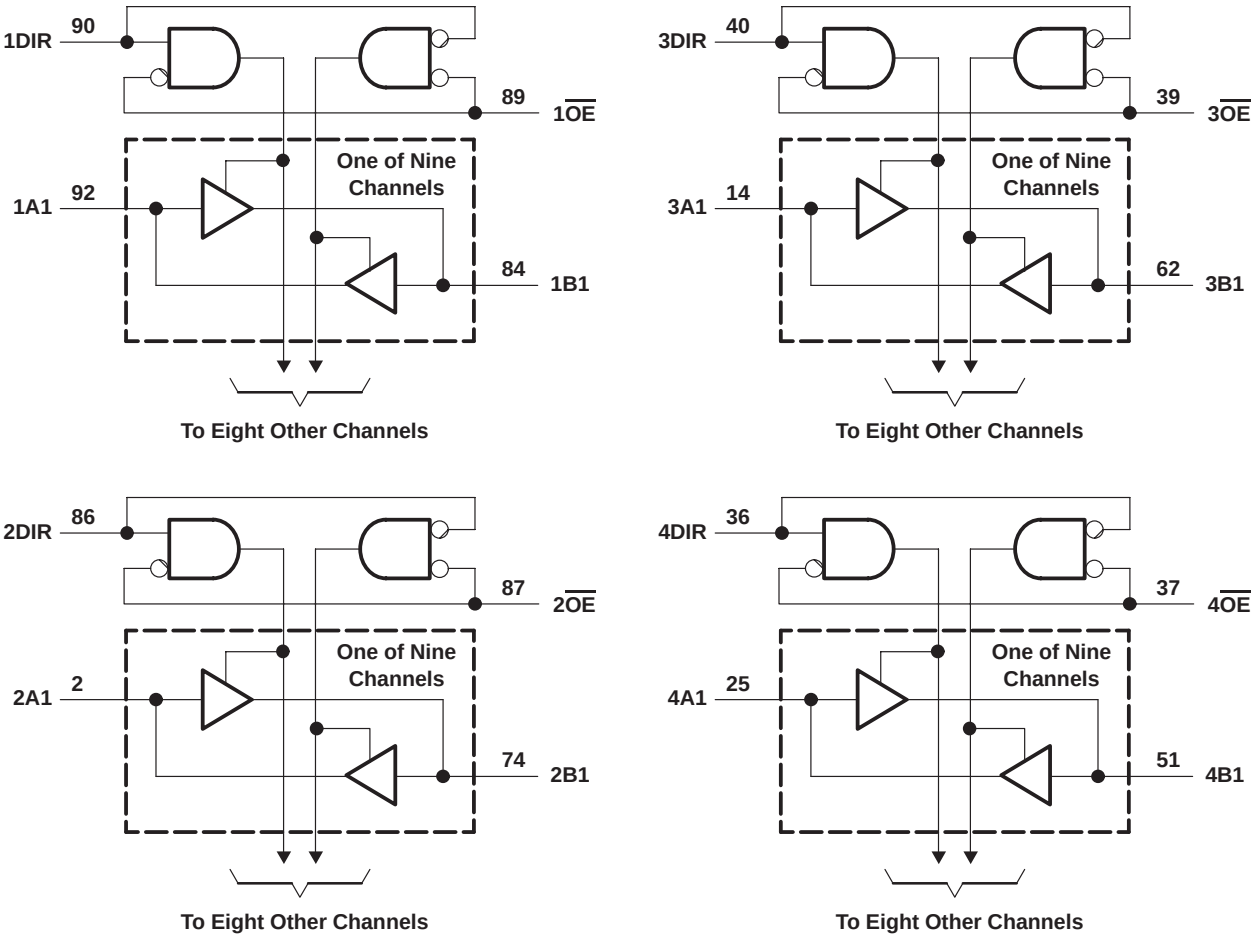
description (continued)

The SN54ABTH32245 is characterized for operation over the full military temperature range of -55°C to 125°C .
 The SN74ABTH32245 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
 (each 9-bit section)

INPUTS		OPERATION
$\overline{\text{OE}}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



Pin numbers shown are for the PZ package.

SN54ABTH32245, SN74ABTH32245

36-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABTH32245	96 mA
SN74ABTH32245	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): PZ package	50°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

		SN54ABTH32245		SN74ABTH32245		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: Unused control pins must be held high or low to prevent them from floating.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54ABTH32245, SN74ABTH32245
36-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS228G – JUNE 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ABTH32245			SN74ABTH32245			UNIT
			MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.5			2.5			V
		$V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$	3			3			
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -24\text{ mA}$	2						
		$V_{CC} = 4.5\text{ V}$, $I_{OH} = -32\text{ mA}$				2			
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 48\text{ mA}$			0.55			0.55	V
		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 64\text{ mA}$						0.55	
V_{hys}				100			100		mV
I_I	Control inputs	$V_{CC} = 0\text{ to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$						± 1	μA
	A or B ports	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$						± 20	
	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 1				μA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}\text{ or GND}$			± 20				
$I_I(\text{hold})$	A or B ports	$V_{CC} = 4.5\text{ V}$, $V_I = 0.8\text{ V}$	100			100			μA
		$V_{CC} = 4.5\text{ V}$, $V_I = 2\text{ V}$	-100			-100			
$I_{OZPU}^{\ddagger}$		$V_{CC} = 0\text{ to }2.1\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50			± 50	μA
$I_{OZPD}^{\ddagger}$		$V_{CC} = 2.1\text{ V to }5.5\text{ V}$, $V_O = 0.5\text{ V to }2.7\text{ V}$, $\overline{OE} = X$			± 50			± 50	μA
I_{off}		$V_{CC} = 0$, $V_I\text{ or }V_O \leq 4.5\text{ V}$						± 100	μA
I_{CEX}		$V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$, Outputs high			50			50	μA
$I_O^{\S}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$	-50	-100	-180	-50	-100	-180	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$							mA
		Outputs high			3			3	
		Outputs low			20			20	
		Outputs disabled			2			2	
$\Delta I_{CC}^{\parallel}$		$V_{CC} = 5.5\text{ V}$, One input at 3.4 V , Other inputs at $V_{CC}\text{ or GND}$			1			1	mA
C_i	Control inputs	$V_I = 2.5\text{ V or }0.5\text{ V}$			3.5			3.5	pF
C_{iO}	A or B ports	$V_O = 2.5\text{ V or }0.5\text{ V}$			9.5			9.5	pF

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] This parameter is specified by characterization.

[§] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

^{||} This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}^{\#}$			SN54ABTH32245		SN74ABTH32245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.7	3.2	4.4	1	5.3	1.7	5	ns
t_{PHL}			1.7	3.3	4.6	1	5.3	1.7	5.2	
t_{PZH}	$\overline{OE}$	B or A	1.6	4.2	6.1	1	7.6	1.6	7.3	ns
t_{PZL}			2.7	5.2	7	1.5	8.2	2.7	8.1	
t_{PHZ}	$\overline{OE}$	B or A	1.3	3.9	6.1	0.8	6.7	1.3	6.5	ns
t_{PLZ}			2	4.4	6.6	1	7.2	2	6.9	

[#] These limits apply only to the SN74ABTH32245



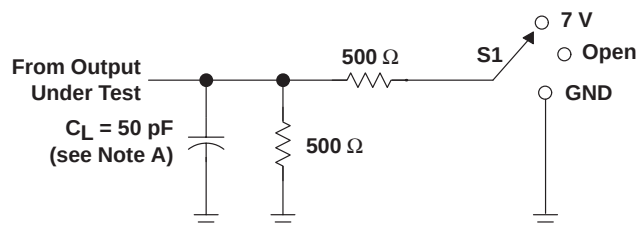
SN54ABTH32245, SN74ABTH32245

36-BIT BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

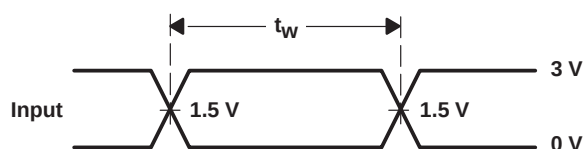
SCBS228G – JUNE 1992 – REVISED MAY 1997

PARAMETER MEASUREMENT INFORMATION

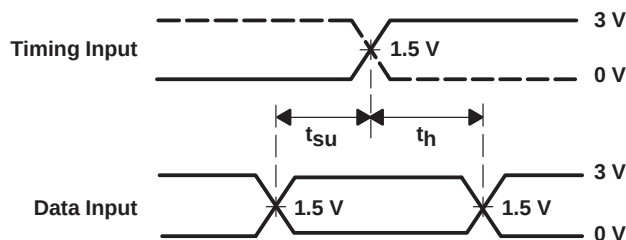


LOAD CIRCUIT

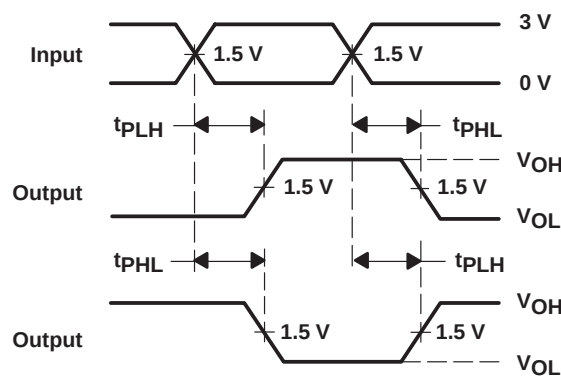
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



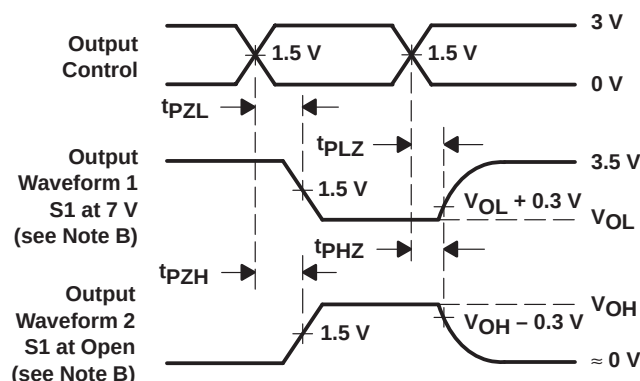
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9557701NXD	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	9557701NXD ABTH32245
SN74ABTH32245PZ	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32245
SN74ABTH32245PZ.B	Active	Production	LQFP (PZ) 100	90 JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32245

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

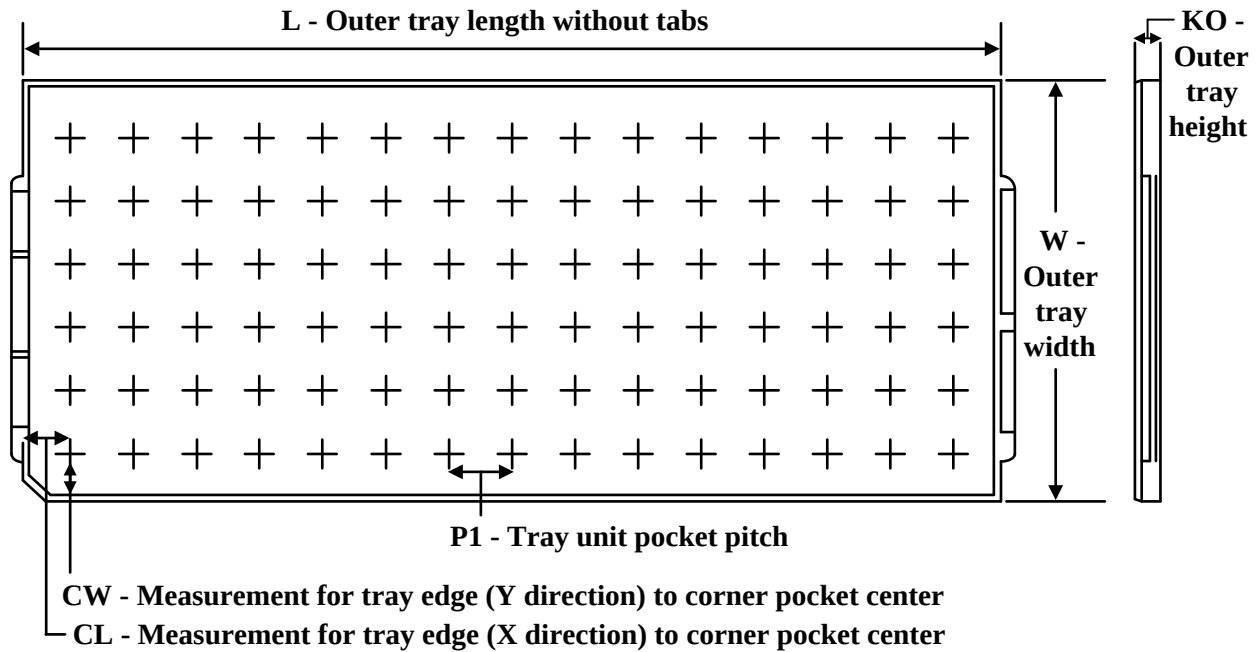
OTHER QUALIFIED VERSIONS OF SN54ABTH32245, SN74ABTH32245 :

- Catalog : [SN74ABTH32245](#)
- Military : [SN54ABTH32245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

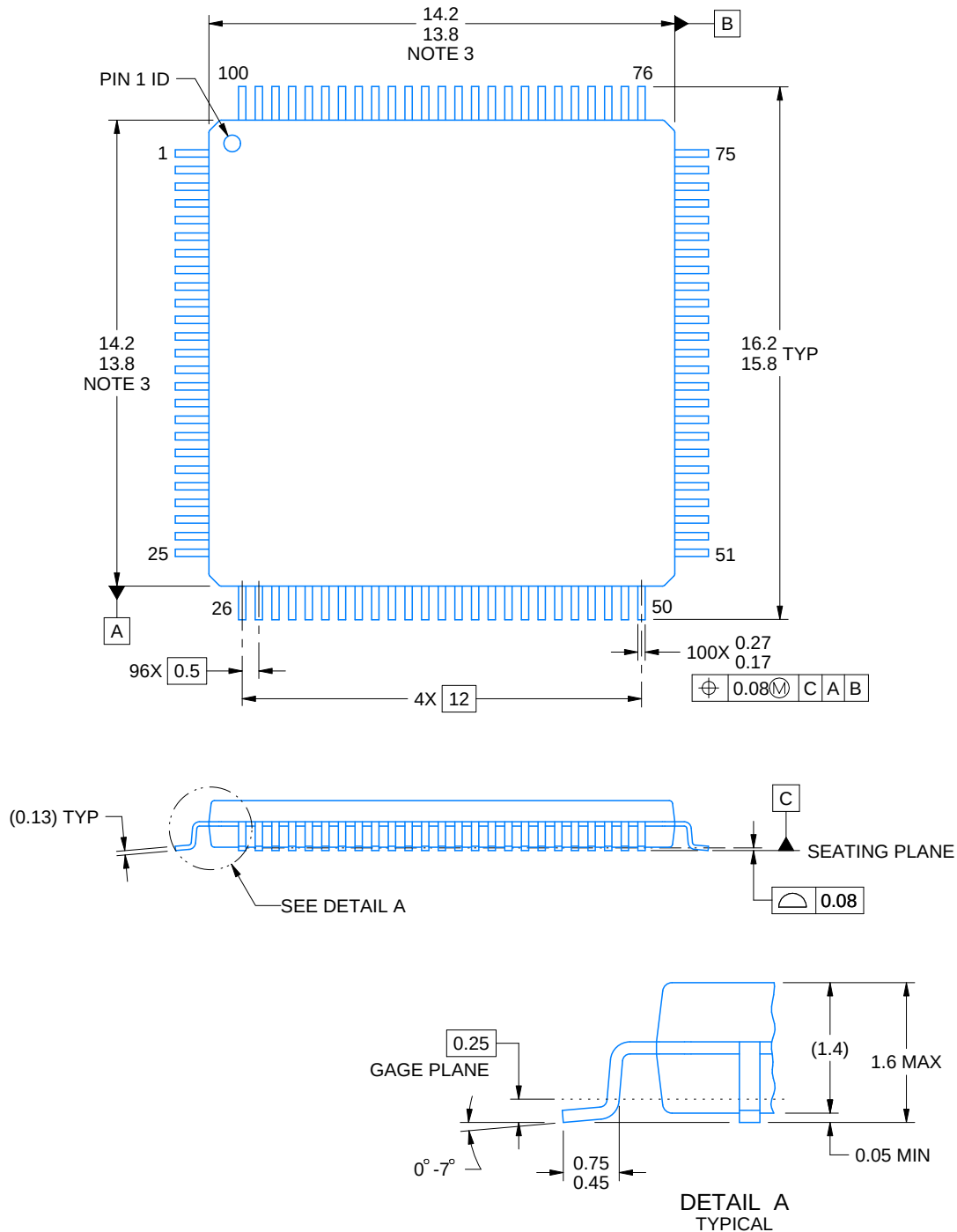
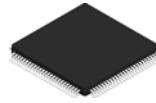
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
5962-9557701NXD	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74ABTH32245PZ	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45
SN74ABTH32245PZ.B	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.45



4215169/A 03/2017

NOTES:

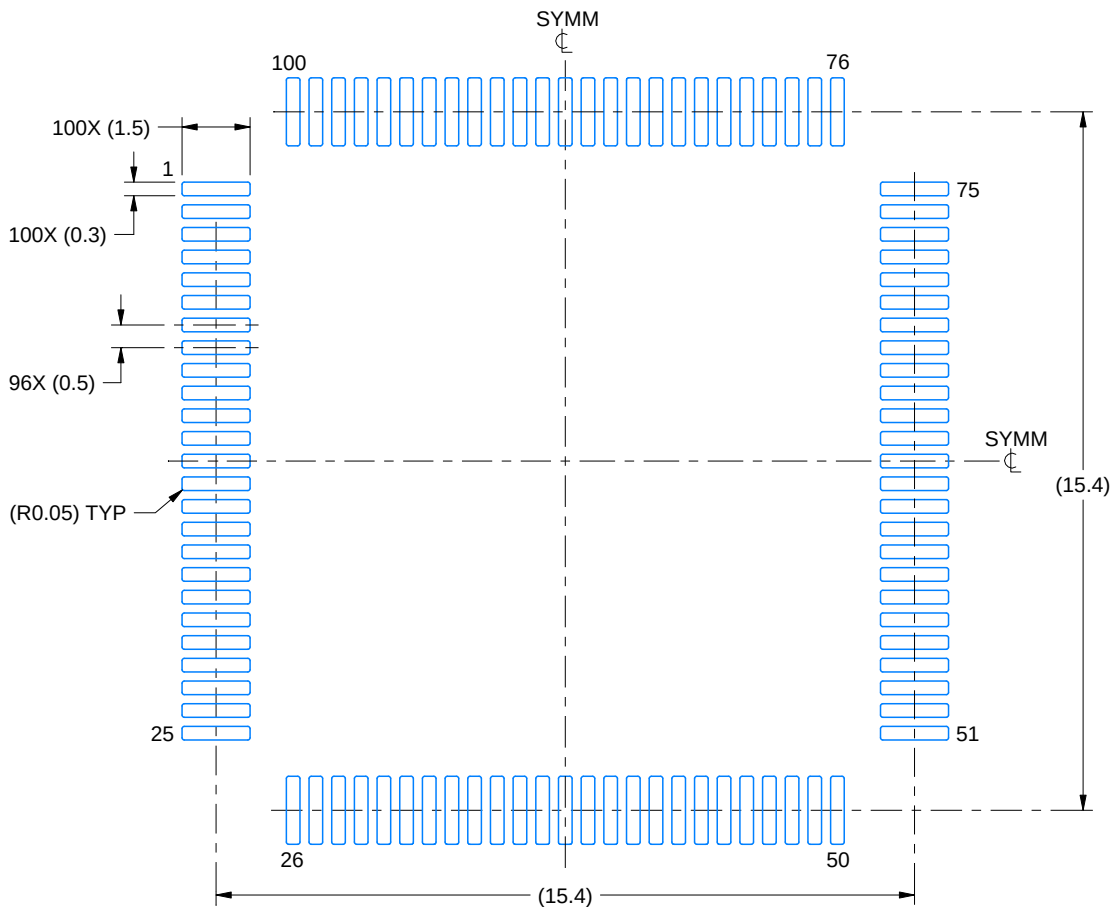
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

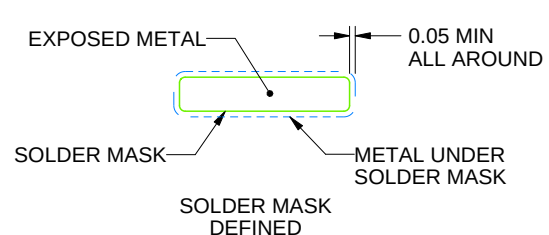
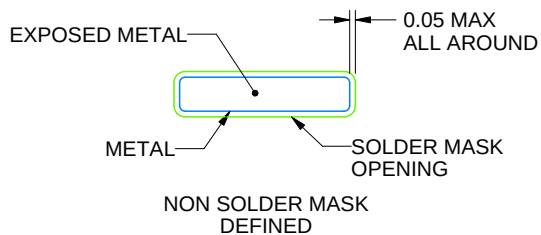
PZ0100A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215169/A 03/2017

NOTES: (continued)

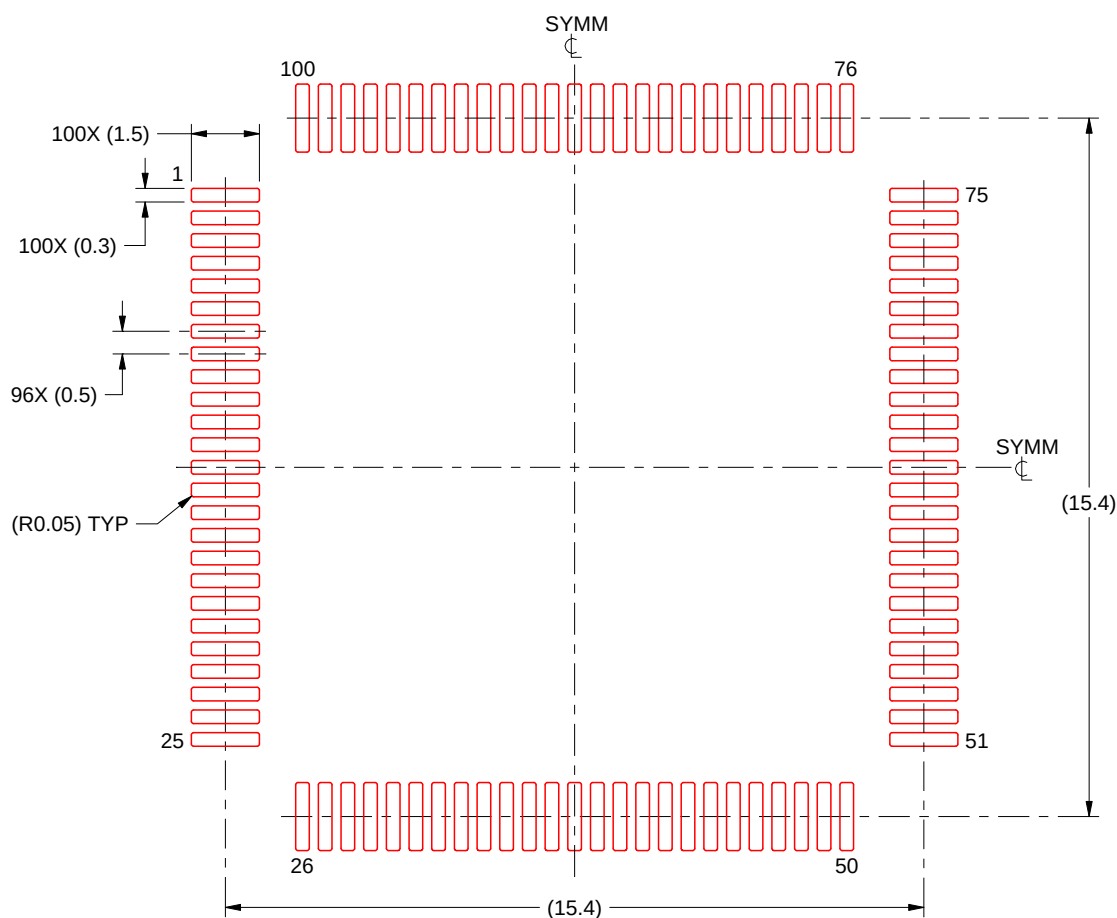
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PZ0100A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215169/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025