

# SN74ACT596-Q1 Automotive 8-Bit Shift Register With Open-Drain Output Registers And TTL-Compatible Inputs

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Available in [wetable flank](#) QFN package
- Operating voltage range of 4.5V to 5.5V
- TTL-compatible inputs
- Continuous  $\pm 24\text{mA}$  output drive at 5V
- Supports up to  $\pm 75\text{mA}$  output drive at 5V in short bursts
- Drives 50 $\Omega$  transmission lines
- Fast operation with delay of 11.6ns max

## 2 Applications

- [Increase the number of outputs on a microcontroller](#)
- Store up to 8 bits of data temporarily

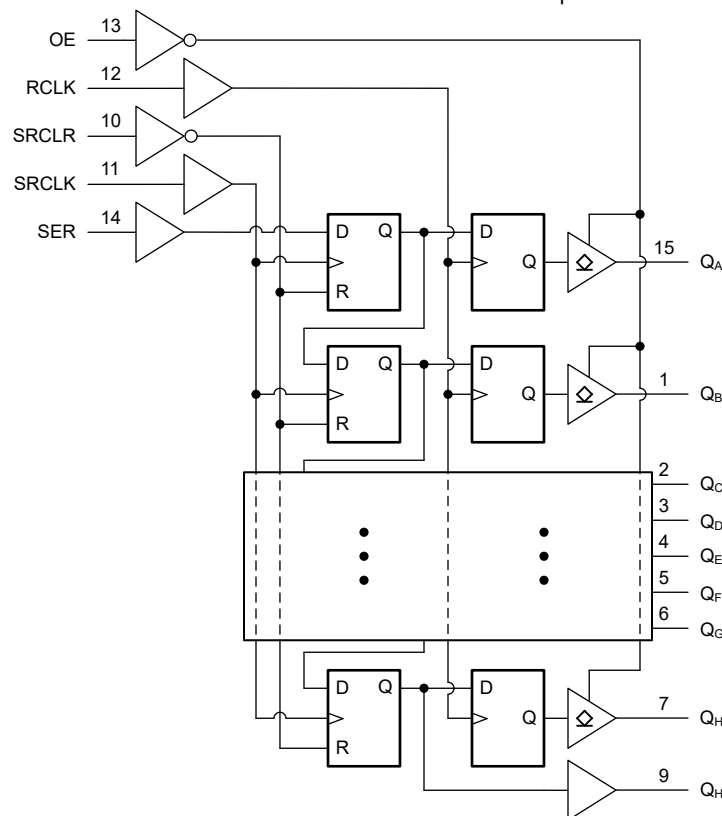
## 3 Description

The SN74ACT596-Q1 device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel open-drain outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and a serial output ( $Q_H$ ) for cascading. When the output-enable ( $\overline{OE}$ ) input is high, the outputs are in a high-impedance state. Internal register data is not impacted by the operation of the  $\overline{OE}$  input.

### Device Information

| PART NUMBER   | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|---------------|------------------------|-----------------------------|--------------------------|
| SN74ACT596-Q1 | BQB (WQFN, 16)         | 3.5mm × 2.5mm               | 3.5mm × 2.5mm            |
|               | PW (TSSOP, 16)         | 5mm × 6.4mm                 | 5mm × 4.4mm              |

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



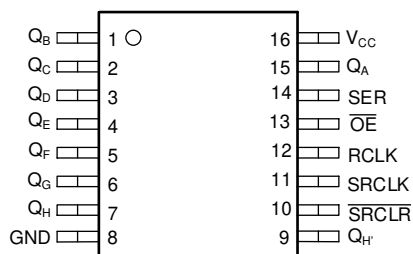
**Functional Diagram**



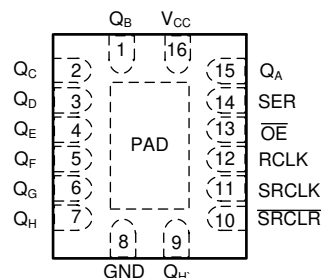
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## 4 Pin Configuration and Functions



**PW Package, 16-Pin TSSOP (Top View)**



**BQB Package, 16-Pin WQFN (Transparent Top View)**

**Table 4-1. Pin Functions**

| PIN                        |     | TYPE <sup>(1)</sup> | DESCRIPTION                                                                                           |
|----------------------------|-----|---------------------|-------------------------------------------------------------------------------------------------------|
| NAME                       | NO. |                     |                                                                                                       |
| Q <sub>B</sub>             | 1   | O                   | Q <sub>B</sub> output (open-drain)                                                                    |
| Q <sub>C</sub>             | 2   | O                   | Q <sub>C</sub> output (open-drain)                                                                    |
| Q <sub>D</sub>             | 3   | O                   | Q <sub>D</sub> output (open-drain)                                                                    |
| Q <sub>E</sub>             | 4   | O                   | Q <sub>E</sub> output (open-drain)                                                                    |
| Q <sub>F</sub>             | 5   | O                   | Q <sub>F</sub> output (open-drain)                                                                    |
| Q <sub>G</sub>             | 6   | O                   | Q <sub>G</sub> output (open-drain)                                                                    |
| Q <sub>H</sub>             | 7   | O                   | Q <sub>H</sub> output (open-drain)                                                                    |
| GND                        | 8   | G                   | Ground                                                                                                |
| Q <sub>H</sub> '           | 9   | O                   | Serial output, can be used for cascading (push-pull)                                                  |
| $\overline{\text{SRCLR}}$  | 10  | I                   | Shift register clear, active low                                                                      |
| SRCLK                      | 11  | I                   | Shift register clock, rising edge triggered                                                           |
| RCLK                       | 12  | I                   | Output register clock, rising edge triggered                                                          |
| $\overline{\text{OE}}$     | 13  | I                   | Output Enable, active low                                                                             |
| SER                        | 14  | I                   | Serial input                                                                                          |
| Q <sub>A</sub>             | 15  | O                   | Q <sub>A</sub> output (open-drain)                                                                    |
| V <sub>CC</sub>            | 16  | P                   | Positive supply                                                                                       |
| Thermal Pad <sup>(2)</sup> |     | —                   | The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply. |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

(2) BQB package only.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                                          |                                                                   | MIN  | MAX                    | UNIT |
|------------------|----------------------------------------------------------|-------------------------------------------------------------------|------|------------------------|------|
| V <sub>CC</sub>  | Supply voltage range                                     |                                                                   | -0.5 | 7                      | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                       |                                                                   | -0.5 | V <sub>CC</sub> + 0.5V | V    |
| V <sub>O</sub>   | Open-drain output voltage range <sup>(2)</sup>           |                                                                   | -0.5 | 7                      | V    |
| V <sub>O</sub>   | Push-pull output voltage range <sup>(2)</sup>            |                                                                   | -0.5 | V <sub>CC</sub> + 0.5V | V    |
| I <sub>IK</sub>  | Input clamp current                                      | V <sub>I</sub> < -0.5V or V <sub>I</sub> > V <sub>CC</sub> + 0.5V |      | ±20                    | mA   |
| I <sub>OK</sub>  | Open-drain output clamp current                          | V <sub>O</sub> < -0.5V                                            |      | -50                    | mA   |
| I <sub>OK</sub>  | Push-pull output clamp current                           | V <sub>O</sub> < -0.5V or V <sub>O</sub> > V <sub>CC</sub> + 0.5V |      | ±50                    | mA   |
| I <sub>O</sub>   | Open-drain continuous output current                     | V <sub>O</sub> = 0 to V <sub>CC</sub>                             |      | 50                     | mA   |
| I <sub>O</sub>   | Push-pull continuous output current                      | V <sub>O</sub> = 0 to V <sub>CC</sub>                             |      | ±50                    | mA   |
|                  | Continuous output current through V <sub>CC</sub> or GND |                                                                   |      | ±200                   | mA   |
| T <sub>J</sub>   | Junction temperature                                     |                                                                   |      | 150                    | °C   |
| T <sub>stg</sub> | Storage temperature                                      |                                                                   | -65  | 150                    | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                    |                         |                                                                                        | VALUE | UNIT |
|--------------------|-------------------------|----------------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 <sup>(1)</sup> | ±2000 | V    |
|                    |                         | Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B          | ±1000 |      |

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                 |                                          |  | MIN | MAX             | UNIT |
|-----------------|------------------------------------------|--|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                           |  | 4.5 | 5.5             | V    |
| V <sub>IH</sub> | High-level input voltage                 |  | 2   |                 | V    |
| V <sub>IL</sub> | Low-Level input voltage                  |  |     | 0.8             | V    |
| V <sub>I</sub>  | Input Voltage                            |  | 0   | V <sub>CC</sub> | V    |
| V <sub>O</sub>  | Open-drain output voltage                |  | 0   | 5.5             | V    |
| V <sub>O</sub>  | Push-pull output Voltage                 |  | 0   | V <sub>CC</sub> | V    |
| I <sub>OH</sub> | High-level output current <sup>(1)</sup> |  |     | -24             | mA   |
| I <sub>OL</sub> | Low-level output current                 |  |     | 24              | mA   |
| Δt/Δv           | Input transition rise or fall rate       |  |     | 20              | ns/V |
| T <sub>A</sub>  | Operating free-air temperature           |  | -40 | 125             | °C   |

- (1) Applies to Q<sub>H</sub> output only.

### 5.4 Thermal Information

| PACKAGE    | PINS | THERMAL METRIC <sup>(1)</sup> |                       |                  |                 |                 |                       | UNIT |
|------------|------|-------------------------------|-----------------------|------------------|-----------------|-----------------|-----------------------|------|
|            |      | R <sub>θJA</sub>              | R <sub>θJC(top)</sub> | R <sub>θJB</sub> | Ψ <sub>JT</sub> | Ψ <sub>JB</sub> | R <sub>θJC(bot)</sub> |      |
| PW (TSSOP) | 16   | 126.2                         | 60.5                  | 84.2             | 7.5             | 83.3            | -                     | °C/W |

| PACKAGE    | PINS | THERMAL METRIC <sup>(1)</sup> |                       |                  |                 |                 |                       | UNIT |
|------------|------|-------------------------------|-----------------------|------------------|-----------------|-----------------|-----------------------|------|
|            |      | R <sub>θJA</sub>              | R <sub>θJC(top)</sub> | R <sub>θJB</sub> | Ψ <sub>JT</sub> | Ψ <sub>JB</sub> | R <sub>θJC(bot)</sub> |      |
| BQB (WQFN) | 16   | 91.2                          | 95.1                  | 61.4             | 18.0            | 61.2            | 38.0                  | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                          | TEST CONDITIONS                                             | V <sub>CC</sub> | -40°C to 125°C |       |      | UNIT |
|------------------------------------|-------------------------------------------------------------|-----------------|----------------|-------|------|------|
|                                    |                                                             |                 | MIN            | TYP   | MAX  |      |
| V <sub>OH</sub> <sup>(4)</sup>     | I <sub>OH</sub> = -50μA                                     | 4.5V            | 4.4            | 4.499 |      | V    |
|                                    |                                                             | 5.5V            | 5.4            | 5.499 |      |      |
|                                    | I <sub>OH</sub> = -24mA                                     | 4.5V            | 3.7            |       |      |      |
|                                    | I <sub>OH</sub> = -24mA                                     | 5.5V            | 4.7            |       |      |      |
|                                    | I <sub>OH</sub> = -75mA <sup>(3)</sup>                      | 5.5V            | 3.85           |       |      |      |
| V <sub>OL</sub>                    | I <sub>OL</sub> = 50μA                                      | 4.5V            |                | 0.001 | 0.1  | V    |
|                                    |                                                             | 5.5V            |                | 0.001 | 0.1  |      |
|                                    | I <sub>OL</sub> = 24mA                                      | 4.5V            |                |       | 0.5  |      |
|                                    | I <sub>OL</sub> = 24mA                                      | 5.5V            |                |       | 0.5  |      |
|                                    | I <sub>OL</sub> = 75mA <sup>(3)</sup>                       | 5.5V            |                |       | 1.65 |      |
| I <sub>I</sub>                     | V <sub>I</sub> = 5.5V or GND                                | 0V to 5.5V      |                |       | ±1   | μA   |
| I <sub>OZ</sub>                    | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5V            |                |       | ±1   | μA   |
| I <sub>CC</sub>                    | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5V            |                |       | 2    | μA   |
| ΔI <sub>CC</sub>                   | V <sub>I</sub> = V <sub>CC</sub> - 2.1V; Any Input          | 4.5V to 5.5V    |                |       | 200  | μA   |
| C <sub>I</sub>                     | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5V              |                | 2     |      | pF   |
| C <sub>O</sub>                     | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5V              |                | 4     |      | pF   |
| C <sub>PD</sub> <sup>(1) (2)</sup> | C <sub>L</sub> = 50pF, F = 1MHz                             | 5V              |                | 57    |      | pF   |

- (1) C<sub>PD</sub> is used to determine the dynamic power consumption, per channel  
(2) P<sub>D</sub> = V<sub>CC</sub><sup>2</sup> × F<sub>I</sub> × (C<sub>PD</sub> + C<sub>L</sub>) where F<sub>I</sub> = input frequency, C<sub>L</sub> = output load capacitance, V<sub>CC</sub> = supply voltage  
(3) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.  
(4) Applies to Q<sub>H</sub> output only.

## 5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER          | DESCRIPTION     | CONDITION                           | V <sub>CC</sub> | -40°C to 125°C |     | UNIT |
|--------------------|-----------------|-------------------------------------|-----------------|----------------|-----|------|
|                    |                 |                                     |                 | MIN            | MAX |      |
| f <sub>clock</sub> | Clock frequency |                                     | 5V              |                | 92  | MHz  |
| t <sub>w</sub>     | Pulse duration  | RCLK or SRCLK high or low           | 5V              | 1.5            |     | ns   |
| t <sub>w</sub>     | Pulse duration  | SRCLR low                           | 5V              | 1.8            |     | ns   |
| t <sub>su</sub>    | Setup time      | SER before SRCLK↑                   | 5V              | 1              |     | ns   |
| t <sub>su</sub>    | Setup time      | SRCLK↑ before RCLK↑                 | 5V              | 2.5            |     | ns   |
| t <sub>su</sub>    | Setup time      | SRCLR low before RCLK↑              | 5V              | 2.4            |     | ns   |
| t <sub>su</sub>    | Setup time      | SRCLR high (inactive) before SRCLK↑ | 5V              | 0.4            |     | ns   |
| t <sub>h</sub>     | Hold time       | SER after SRCLK↑                    | 5V              | 0.7            |     | ns   |

## 5.7 Switching Characteristics

$C_L = 50$  pF; over operating free-air temperature range; typical values measured at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | $-40^\circ\text{C}$ to $125^\circ\text{C}$ |     |      | UNIT |
|-----------|--------------|-------------|----------|--------------------------------------------|-----|------|------|
|           |              |             |          | MIN                                        | TYP | MAX  |      |
| $t_{plh}$ | RCLK         | $Q_A-Q_H$   | 5V       |                                            | 4.5 | 6.5  | ns   |
| $t_{phl}$ | RCLK         | $Q_A-Q_H$   | 5V       |                                            | 7.9 | 11.6 | ns   |
| $t_{plh}$ | SRCLK        | $Q_H'$      | 5V       |                                            | 7.2 | 10.5 | ns   |
| $t_{phl}$ | SRCLK        | $Q_H'$      | 5V       |                                            | 7.2 | 10.4 | ns   |
| $t_{phl}$ | SRCLR        | $Q_H'$      | 5V       |                                            | 7.6 | 10.7 | ns   |

## 5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$  (unless otherwise noted)

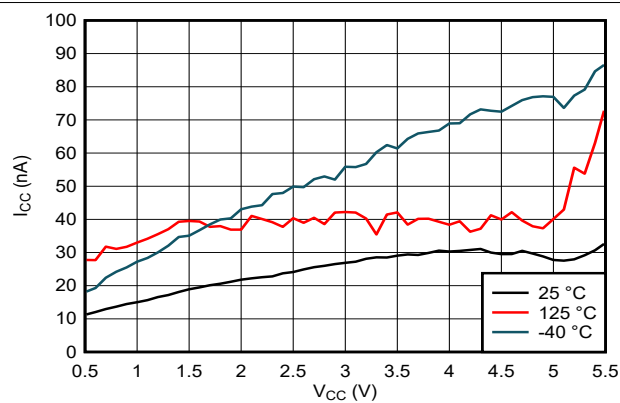


Figure 5-1. Supply Current Across Supply Voltage

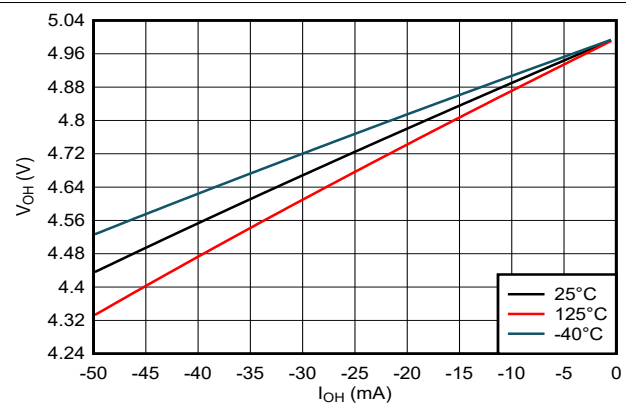


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

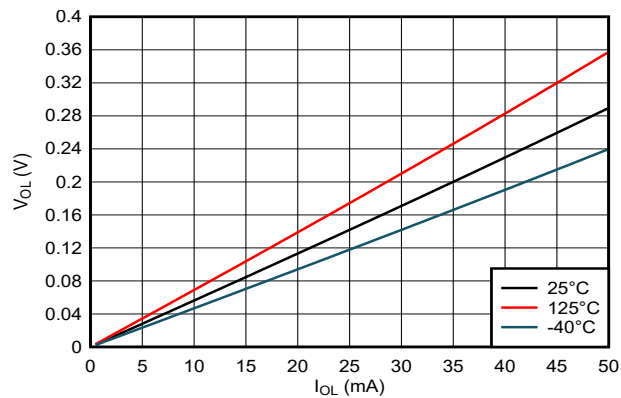


Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

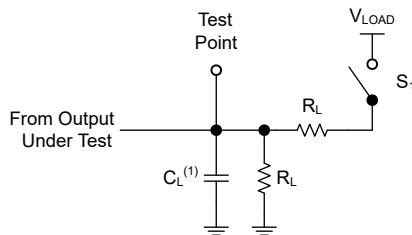
## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_f < 2.5\text{ns}$ ,  $V_t = 1.5\text{V}$ . For push-pull outputs,  $R_L = 500\Omega$ .

For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.

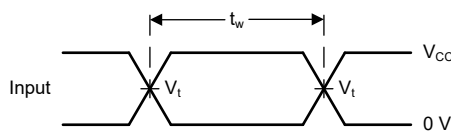
The outputs are measured individually with one input transition per measurement.

| TEST                                | S1     | $R_L$       | $C_L$         | $\Delta V$    | $V_{\text{LOAD}}$        |
|-------------------------------------|--------|-------------|---------------|---------------|--------------------------|
| $t_{\text{PLZ}}$ , $t_{\text{PZL}}$ | CLOSED | $500\Omega$ | $50\text{pF}$ | $0.3\text{V}$ | $2 \times V_{\text{CC}}$ |

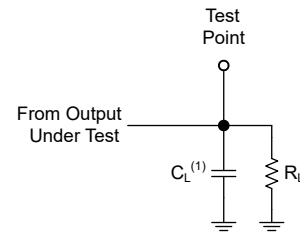


(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for Open-Drain Outputs**

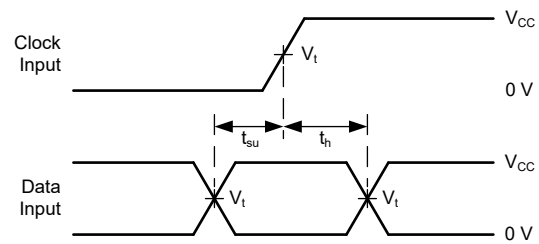


**Figure 6-3. Voltage Waveforms, Pulse Duration**

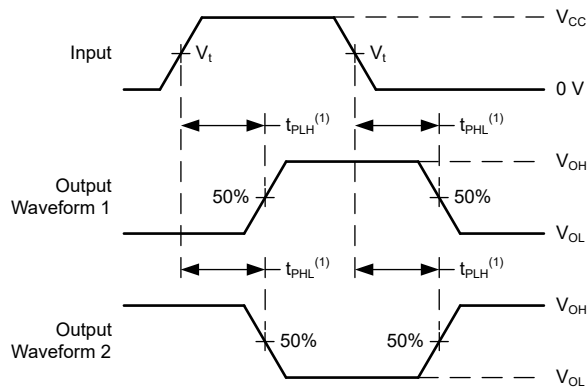


(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-2. Load Circuit for Push-Pull Outputs**

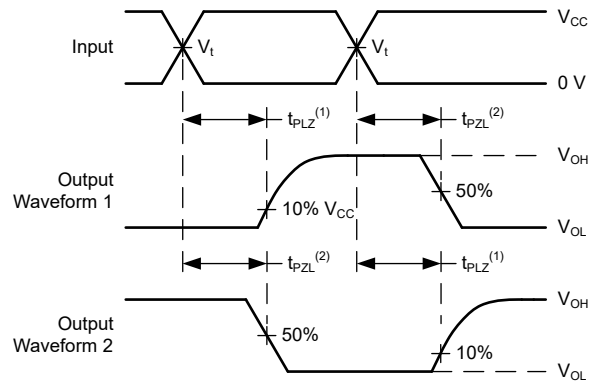


**Figure 6-4. Voltage Waveforms, Setup and Hold Times**



(1) The greater between  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  is the same as  $t_{\text{pd}}$ .

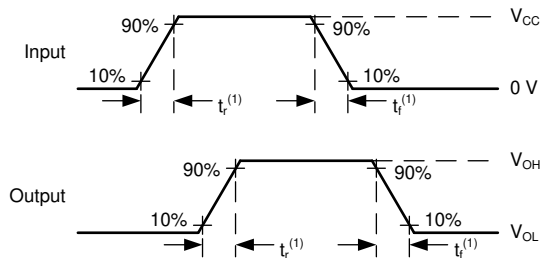
**Figure 6-5. Voltage Waveforms Propagation Delays**



(1)  $t_{\text{PLZ}}$  is the same as  $t_{\text{dis}}$ .

(2)  $t_{\text{PZL}}$  is the same as  $t_{\text{en}}$ .

**Figure 6-6. Voltage Waveforms Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_{tr}$ .

**Figure 6-7. Voltage Waveforms, Input and Output Transition Times**



being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused open-drain CMOS outputs should be left disconnected.

### 7.3.3 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

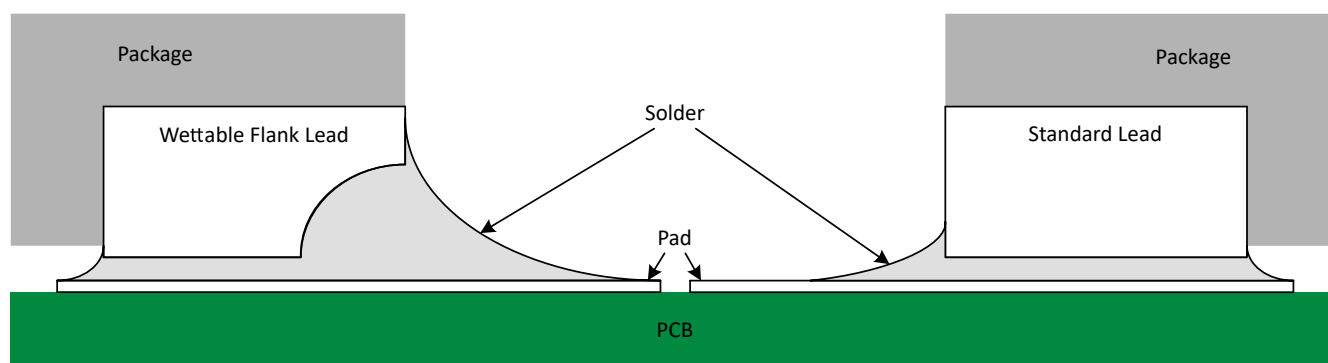
TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ( $R = V \div I$ ).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the [Implications of Slow or Floating CMOS Inputs](#) application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at  $V_{CC}$  or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and typically will meet all requirements.

### 7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet where packages include this feature.



**Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering**

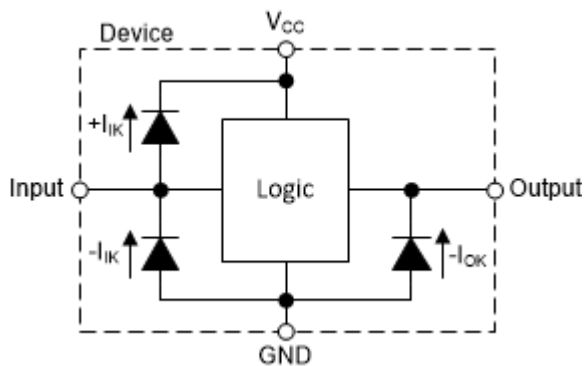
Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 7-2](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

### 7.3.5 Clamp Diode Structure

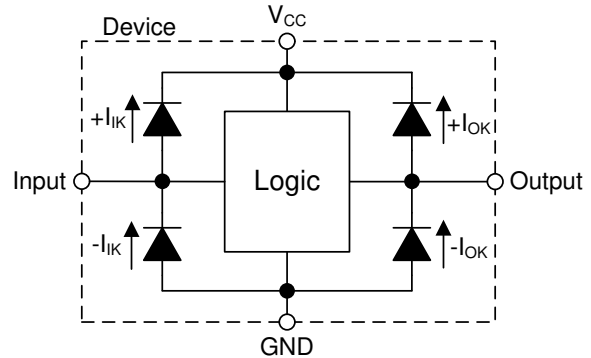
The open-drain outputs to this device have negative clamping diodes only as depicted in Figure 7-3, and the push-pull outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-4. The inputs to this device have both positive and negative clamping diodes as depicted in both previously referenced figures.

#### CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.



**Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Open-Drain Output**



**Figure 7-4. Electrical Placement of Clamping Diodes for Each Input and Push-Pull Output**

### 7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74ACT596-Q1. Outputs  $Q_A - Q_H$  are open-drain. Open-drain outputs drive low when in the low (L) state, and enter the high-impedance (Z) state when set to the high (H) state.

**Table 7-1. Function Table**

| INPUTS |       |       |      |    | FUNCTION                                                                                                  |
|--------|-------|-------|------|----|-----------------------------------------------------------------------------------------------------------|
| SER    | SRCLK | SRCLR | RCLK | OE |                                                                                                           |
| X      | X     | X     | X    | H  | Outputs $Q_A - Q_H$ are disabled.                                                                         |
| X      | X     | X     | X    | L  | Outputs $Q_A - Q_H$ are enabled.                                                                          |
| X      | X     | L     | X    | X  | Shift register is cleared.                                                                                |
| L      | ↑     | H     | X    | X  | First stage of the shift register goes low. Other stages store the data of previous stage, respectively.  |
| H      | ↑     | H     | X    | X  | First stage of the shift register goes high. Other stages store the data of previous stage, respectively. |
| X      | X     | H     | ↑    | X  | Shift-register data is stored in the storage register.                                                    |
| X      | ↑     | H     | ↑    | X  | Data in shift register is stored in the storage register, the data is then shifted through.               |

## 8 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

### 8.1 Application Information

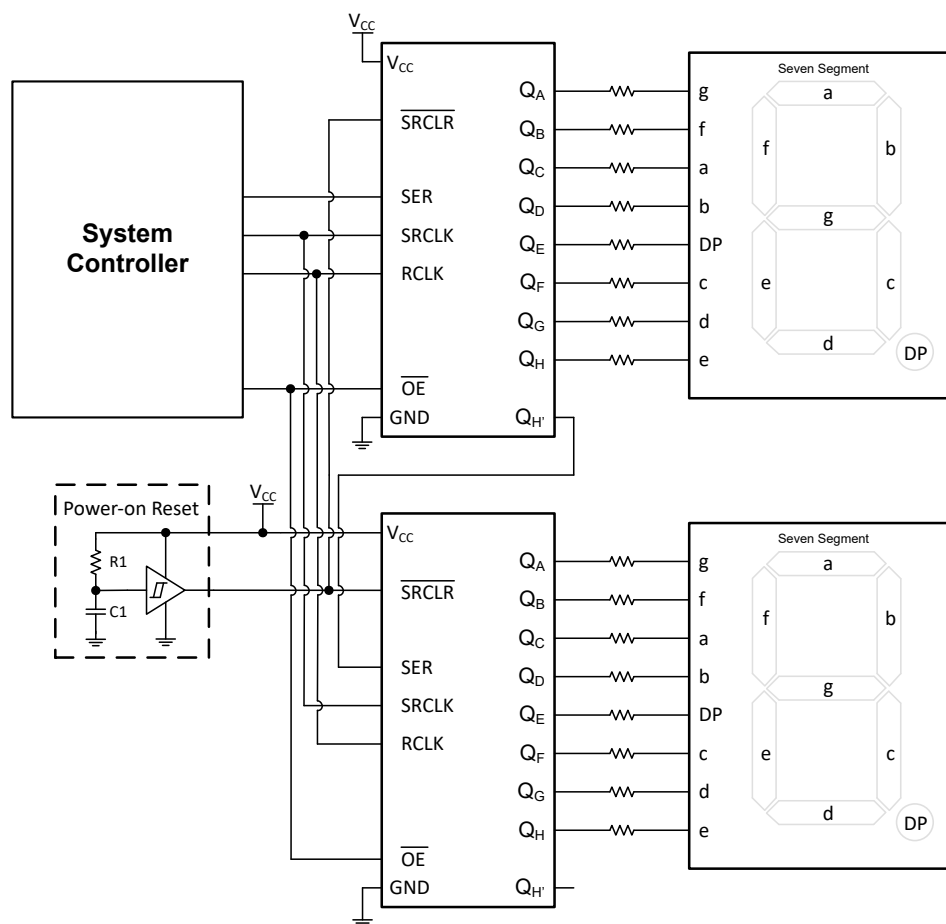
In this application, the SN74ACT596-Q1 is used to control seven-segment displays. Utilizing the serial output and combining a few of the input signals, this implementation reduces the number of I/O pins required to control the displays from sixteen, one per LED, to only four. Unlike other I/O expanders, the SN74ACT596-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins. With separate control for the shift registers and output registers, the desired digit can be displayed while the data for the next digit is loaded into the shift register. All storage register outputs are open-drain.

The  $\overline{OE}$  pin is used to easily disable the outputs when the displays need to be turned off or connected to a PWM signal to control brightness. However, this pin can be tied low and the outputs of the SN74ACT596-Q1 can be controlled accordingly to turn off all the outputs reducing the I/O needed to three.

There is no practical limitation to how many SN74ACT596-Q1 devices can be cascaded. To add more, the serial output will need to be connected to the following serial input and the clocks will need to be connected accordingly. The  $Q_H$  pin is a push-pull output, which does not require a pull-up resistor to operate. It is also always active, regardless of the  $\overline{OE}$  pin input state.

At power-up, the initial state of the shift registers and output registers are unknown. To give them a defined state, the shift register needs to be cleared and then clocked into the output register.

## 8.2 Typical Application



**Figure 8-1. Typical Application Block Diagram**

## 8.2.1 Design Requirements

### 8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74ACT596-Q1 plus the maximum static supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through  $V_{CC}$  listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74ACT596-Q1 plus the maximum supply current,  $I_{CC}$ , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74ACT596-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74ACT596-Q1 can drive a load with total resistance described by  $R_L \geq V_O / I_O$ , with the output voltage and current defined in the *Electrical Characteristics* table with  $V_{OH}$  and  $V_{OL}$ . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the  $V_{CC}$  pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

#### CAUTION

The maximum junction temperature,  $T_{J(max)}$  listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

### 8.2.1.2 Input Considerations

Input signals must cross  $V_{IL(max)}$  to be considered a logic LOW, and  $V_{IH(min)}$  to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either  $V_{CC}$  or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74ACT596-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k $\Omega$  resistor value is often used due to these factors.

The SN74ACT596-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the  $V_{OH}$  specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the  $V_{OL}$  specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Open-drain outputs can be connected together directly to produce a wired-AND configuration or for additional output drive strength.

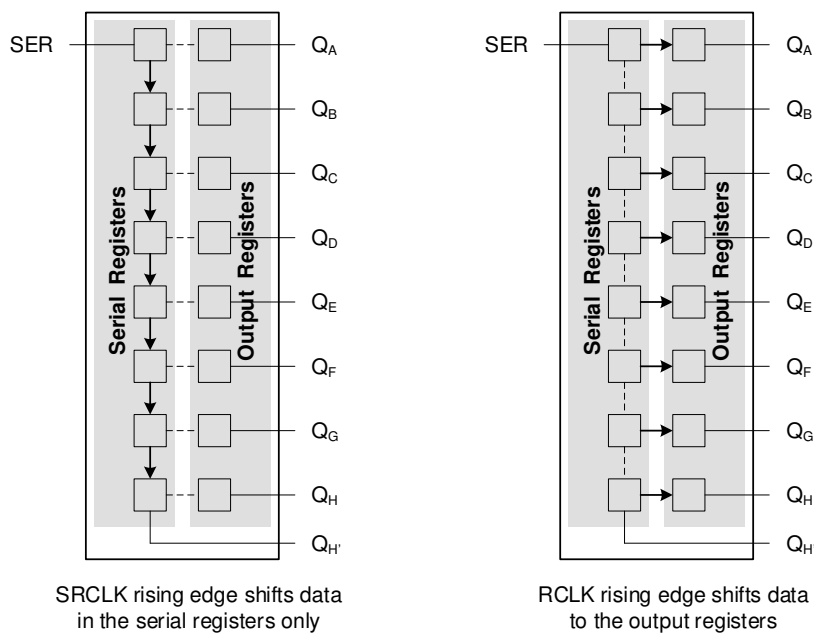
Unused outputs can be left floating. Do not connect outputs directly to  $V_{CC}$  or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

## 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from  $V_{CC}$  to GND. The capacitor needs to be placed physically close to the device and electrically close to both the  $V_{CC}$  and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is  $\leq 50\text{pF}$ . This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74ACT596-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than  $(V_{CC} / I_{O(max)})\Omega$ . Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in  $M\Omega$ ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

## 8.2.3 Application Curves



**Figure 8-2. Simplified Functional Diagram Showing Clock Operation**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For the SN74ACT596-Q1, a  $0.1\mu\text{F}$  bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of  $0.1\mu\text{F}$  and  $1\mu\text{F}$  are commonly used in parallel.

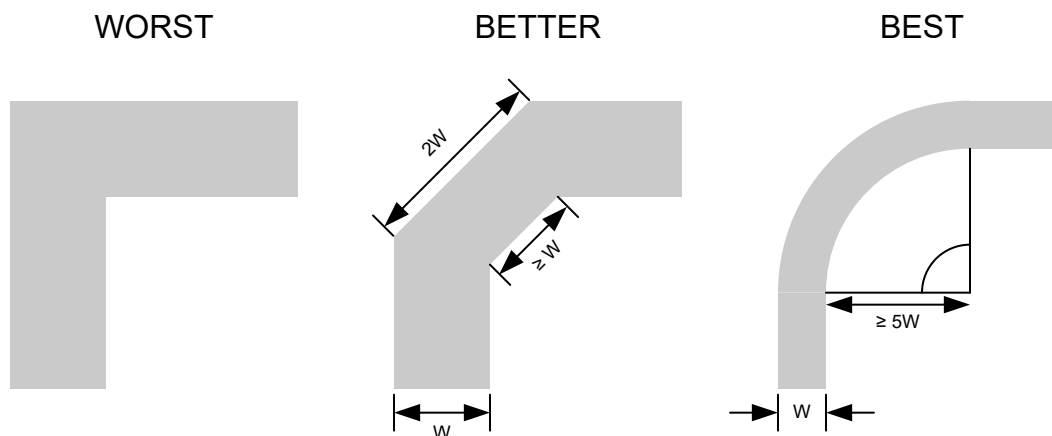
## 8.4 Layout

### 8.4.1 Layout Guidelines

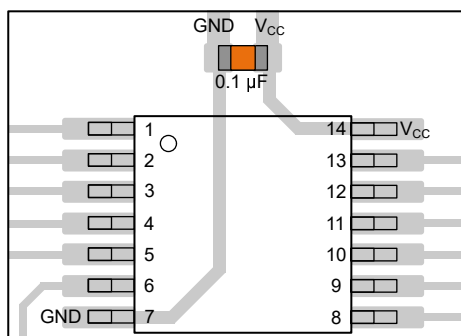
- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry

- 8mil to 12mil trace width
- Lengths less than 12cm to minimize transmission line effects
- Avoid 90° corners for signal traces
- Use an unbroken ground plane below signal traces
- Flood fill areas around signal traces with ground
- For traces longer than 12cm
  - Use impedance controlled traces
  - Source-terminate using a series damping resistor near the output
  - Avoid branches; buffer signals that must branch separately

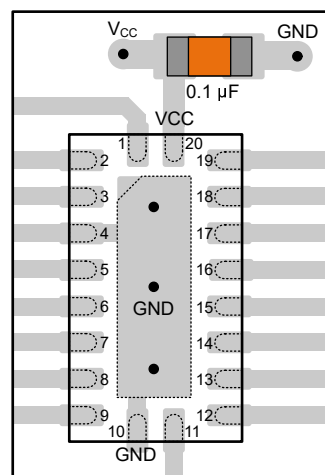
#### 8.4.2 Layout Example



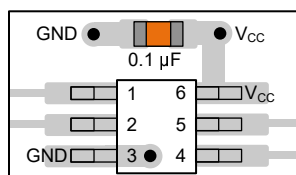
**Figure 8-3. Example Trace Corners for Improved Signal Integrity**



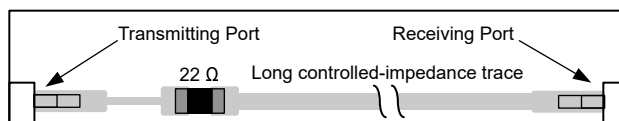
**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and  \$C\_{pd}\$  Calculation application report](#)
- Texas Instruments, [Designing With Logic application report](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application report](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE          | REVISION | NOTES           |
|---------------|----------|-----------------|
| November 2024 | *        | Initial release |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ACT596PWRQ1</a>   | Active        | Production           | TSSOP (PW)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ACT596Q             |
| SN74ACT596PWRQ1.A                 | Active        | Production           | TSSOP (PW)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | ACT596Q             |
| <a href="#">SN74ACT596WBQBRQ1</a> | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AD596Q              |
| SN74ACT596WBQBRQ1.A               | Active        | Production           | WQFN (BQB)   16 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | AD596Q              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

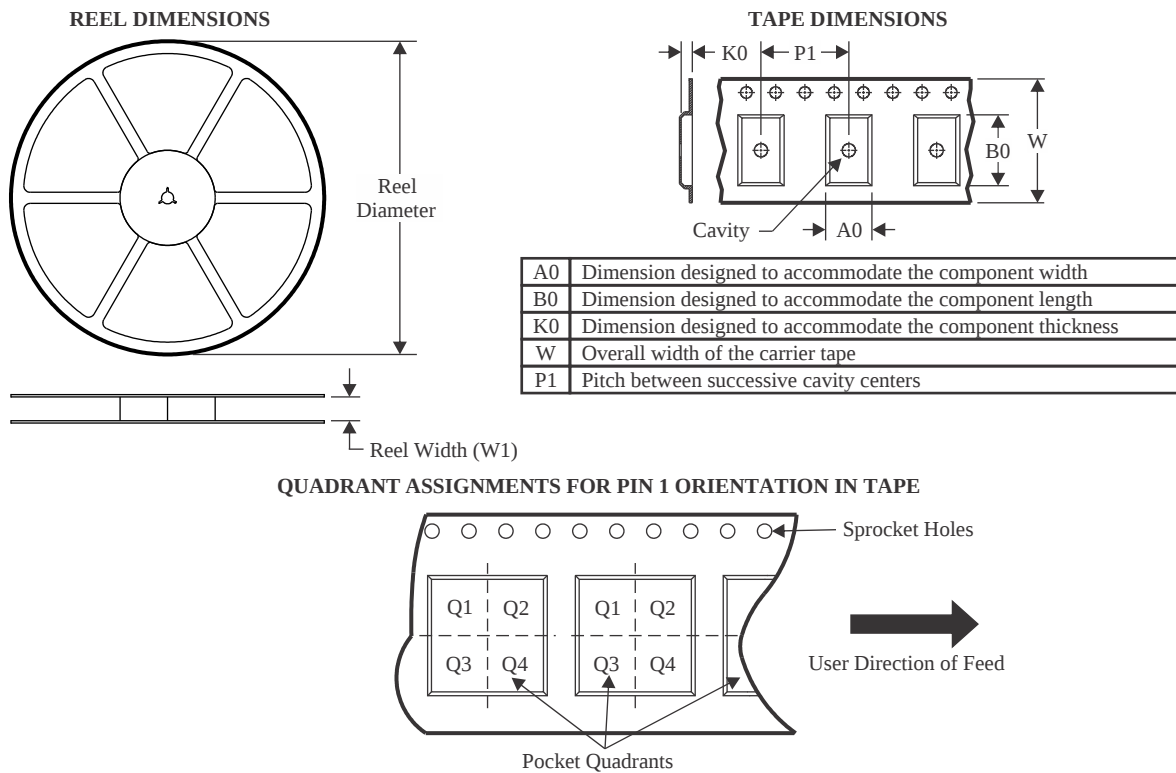
**OTHER QUALIFIED VERSIONS OF SN74ACT596-Q1 :**

- Catalog : [SN74ACT596](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

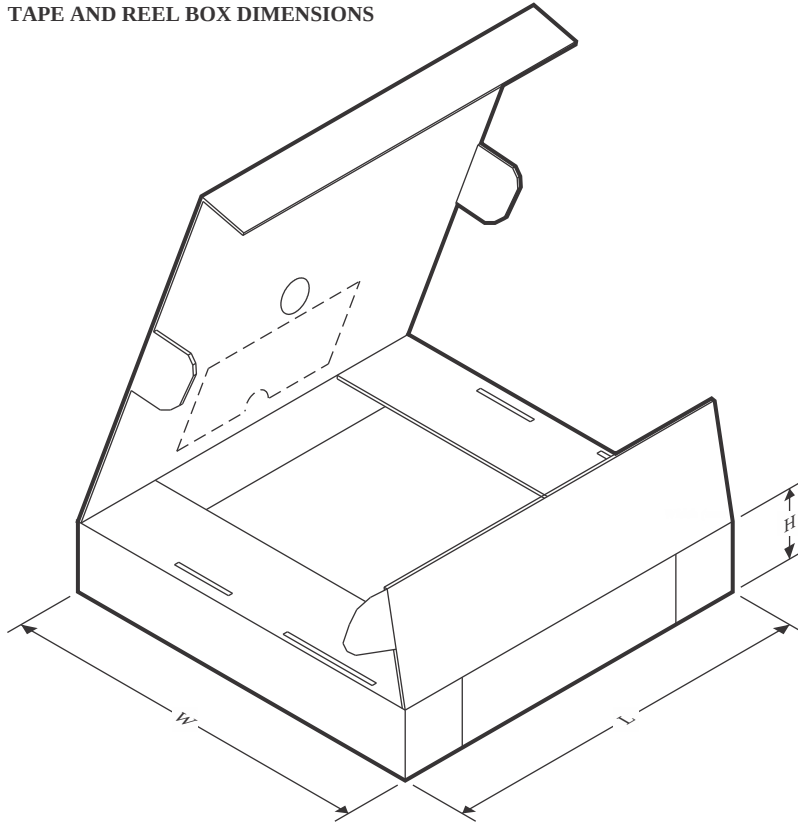
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT596PWRQ1   | TSSOP        | PW              | 16   | 3000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74ACT596WBQBRQ1 | WQFN         | BQB             | 16   | 3000 | 180.0              | 12.4               | 2.8     | 3.8     | 1.2     | 4.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT596PWRQ1   | TSSOP        | PW              | 16   | 3000 | 353.0       | 353.0      | 32.0        |
| SN74ACT596WBQBRQ1 | WQFN         | BQB             | 16   | 3000 | 210.0       | 185.0      | 35.0        |

## GENERIC PACKAGE VIEW

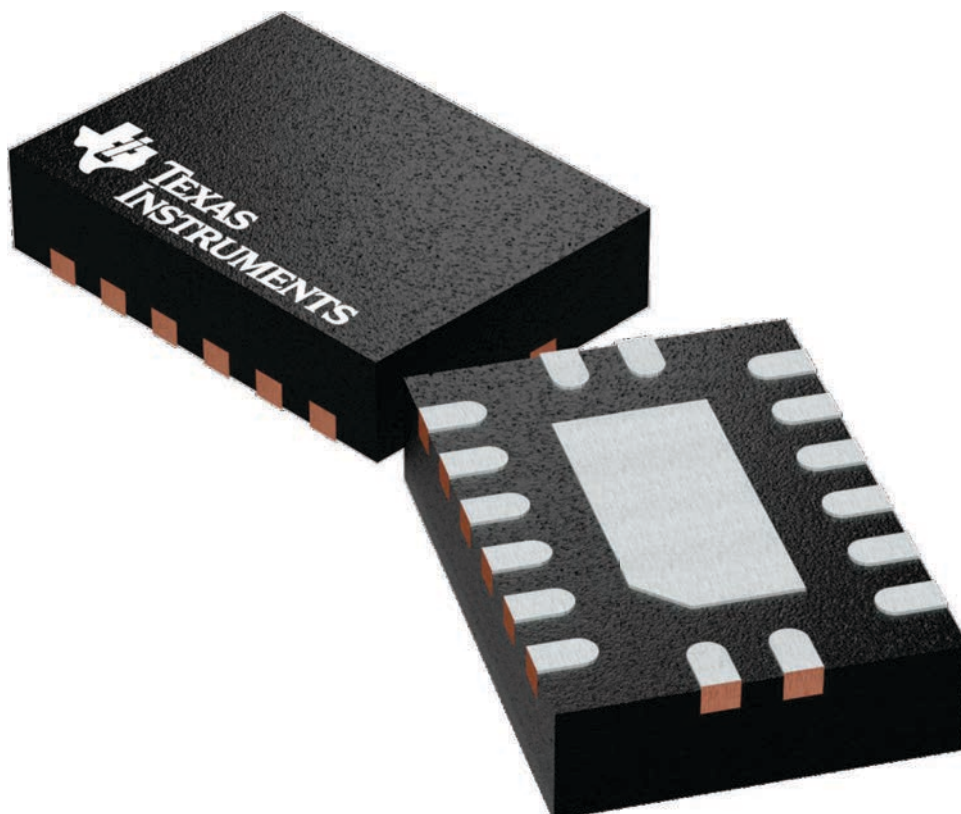
**BQB 16**

**WQFN - 0.8 mm max height**

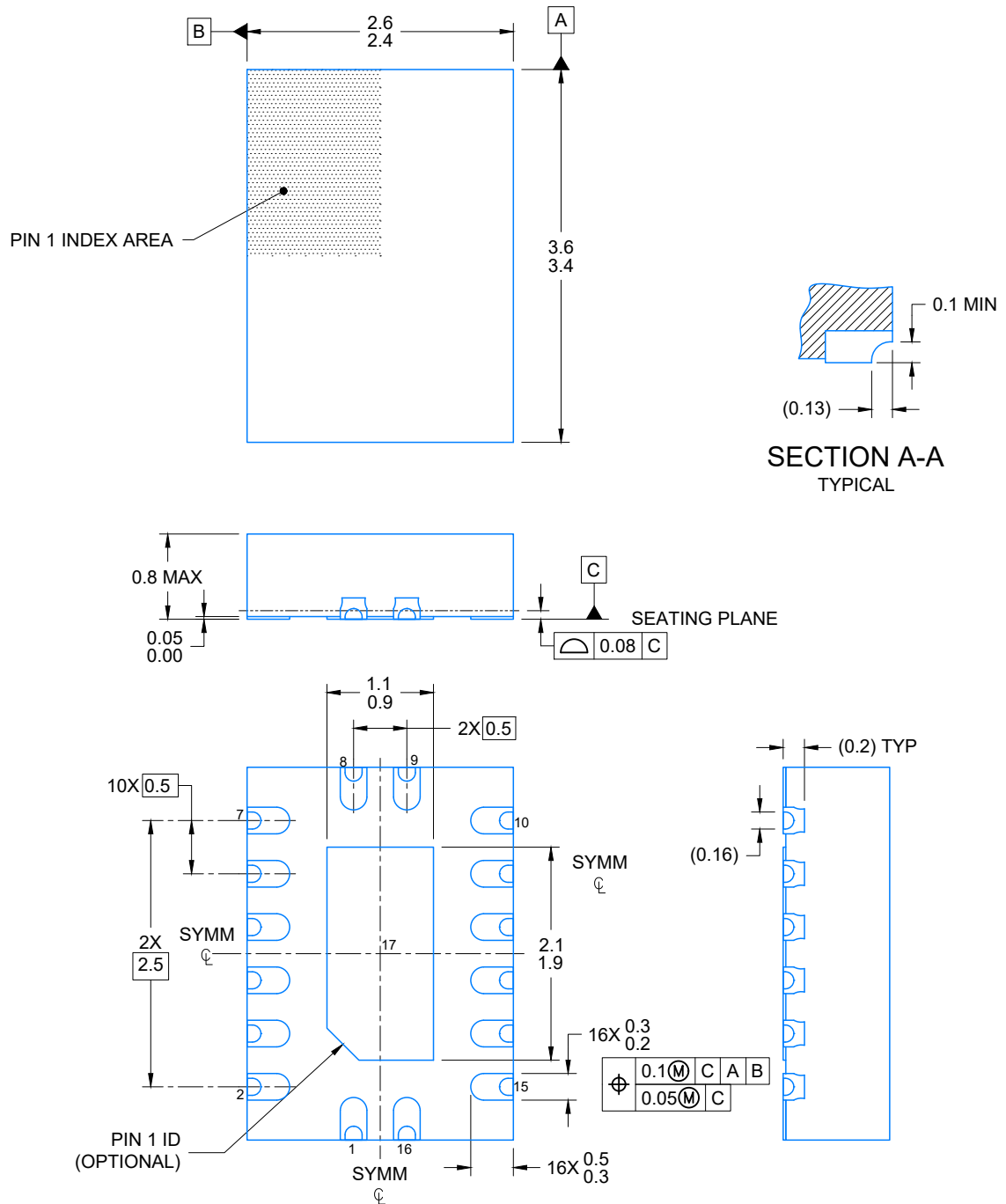
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



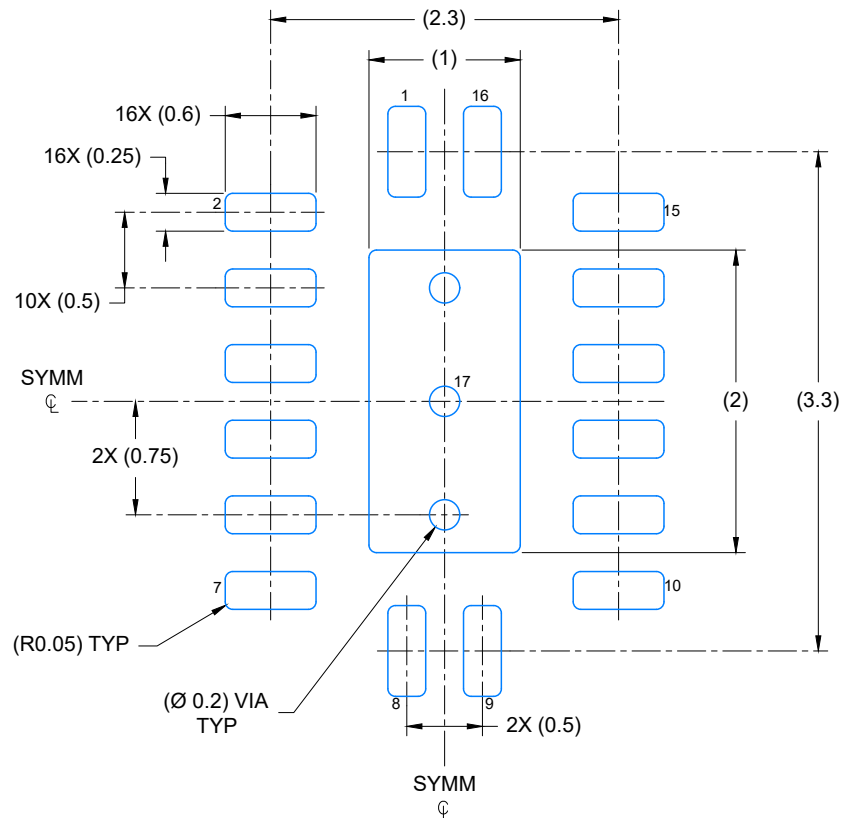
4226161/A



4226135/A 08/2020

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

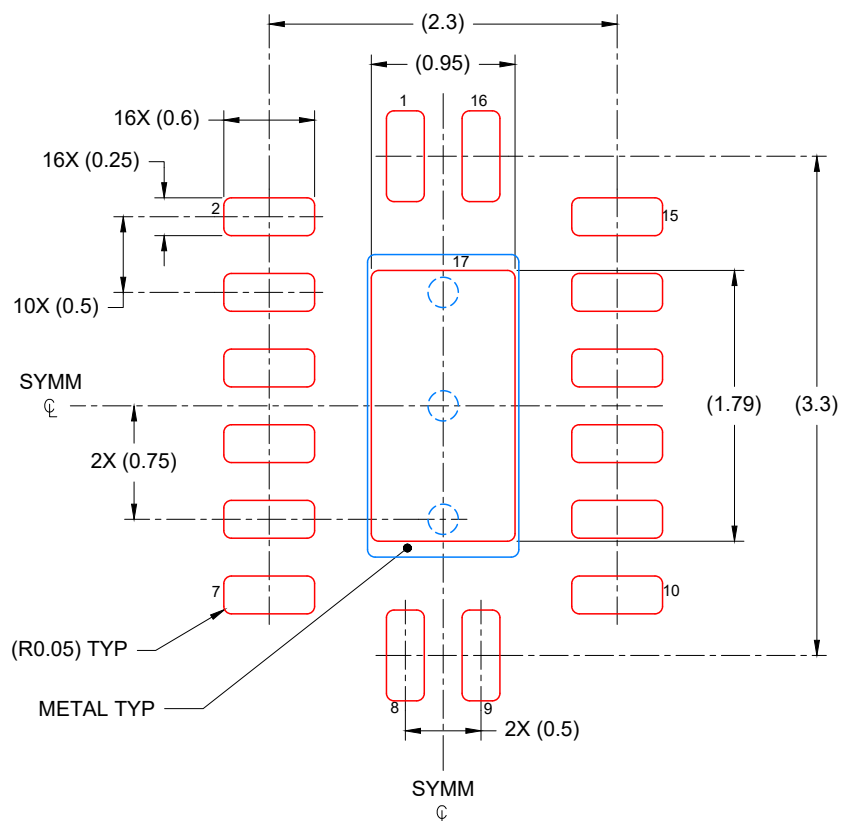


LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

4226135/A 08/2020

## NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



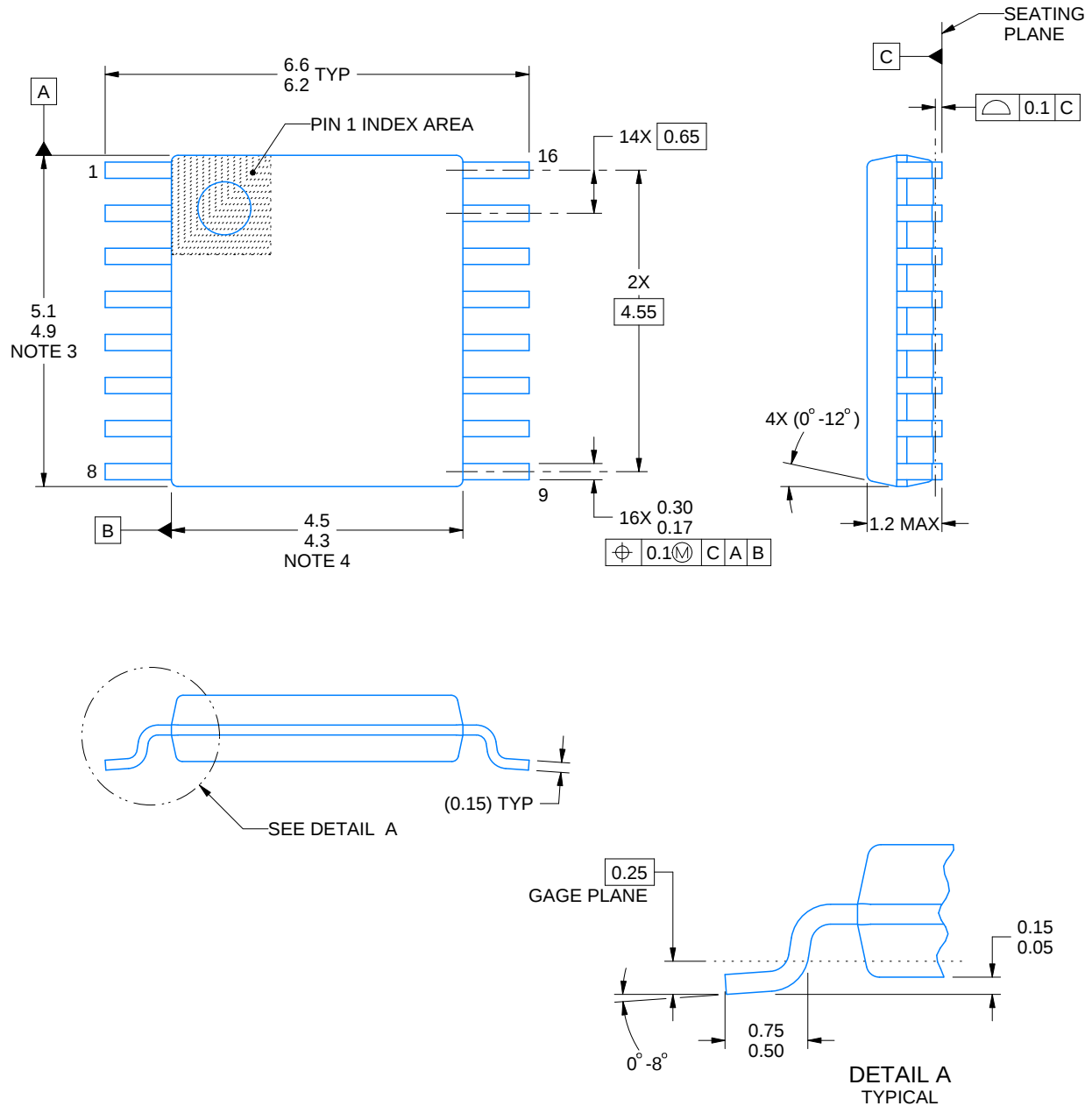
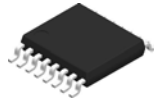
## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
85% PRINTED COVERAGE BY AREA  
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

## NOTES:

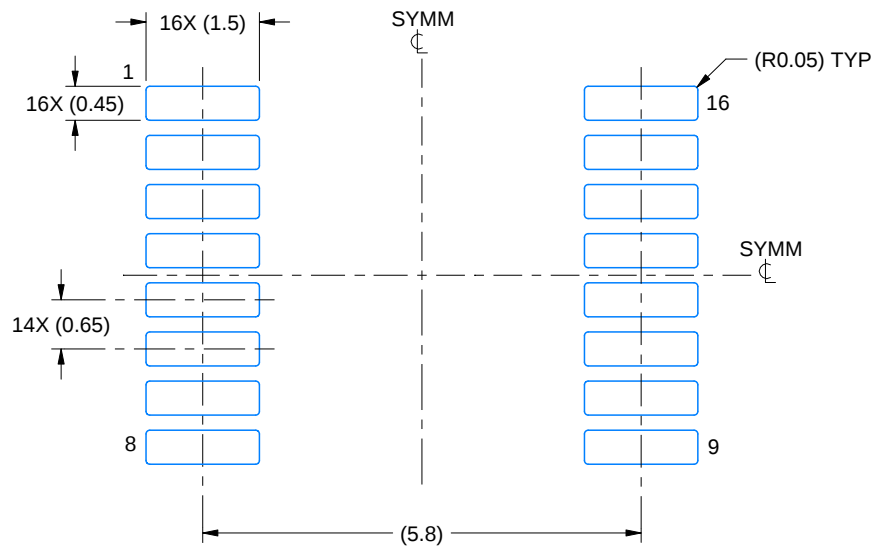
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

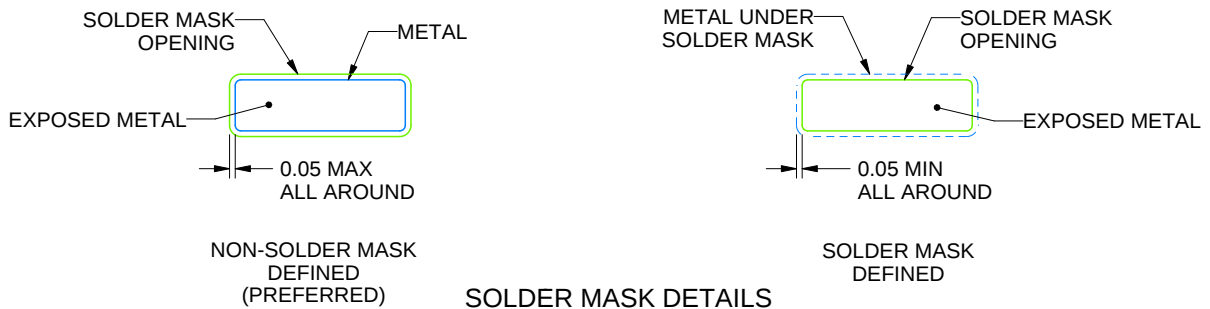
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

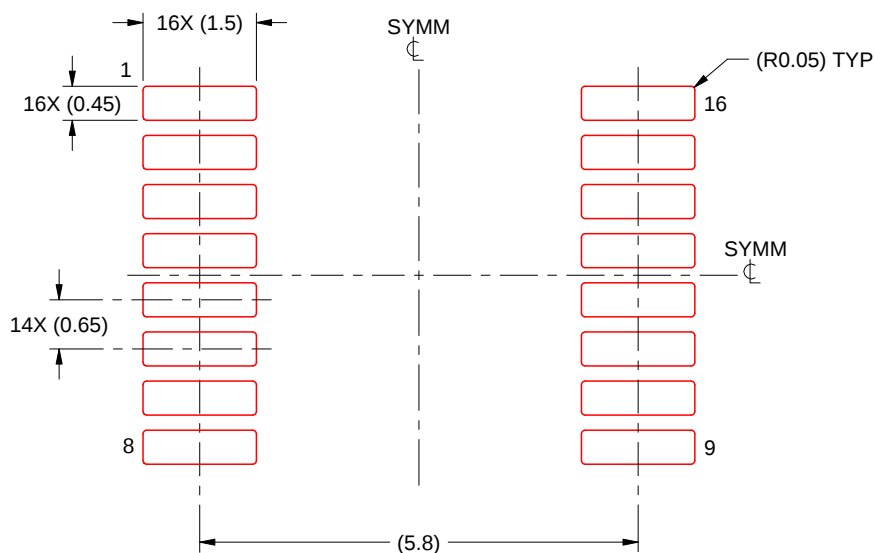
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025