

SNx4AHC04 HEX INVERTERS

1 Features

- Operating range of 2 V to 5.5 V
- Latch-up performance exceeds 250 mA per JESD 17

2 Description

The 'AHC04 devices contain six independent inverters. These devices perform the Boolean function $Y = \bar{A}$.

Device Information

| PART NUMBER | PACKAGE ¹ | BODY SIZE ² |
|-------------|----------------------|------------------------|
| SN54AHC04 | J (CDIP, 14) | 19.56 mm × 6.67 mm |
| | W (CFP, 14) | 13.1 mm × 6.92 mm |
| | FK (LCCC, 20) | 8.9 mm × 8.9 mm |
| SN74AHC04 | N (PDIP, 14) | 19.3 mm × 6.35 mm |
| | D (SOIC, 14) | 8.65 mm × 3.91 mm |
| | DB (SSOP, 14) | 6.20 mm × 5.30 mm |
| | NS (SOP, 14) | 12.60 mm × 5.30 mm |
| | PW (TSSOP, 14) | 5.00 mm × 4.40 mm |
| | DGV (TVSOP, 14) | 3.6 mm × 4.4 mm |
| | RGY (VQFN, 14) | 3.50 mm × 3.50 mm |
| | BQA (WQFN, 14) | 3 mm × 2.5 mm |

1. For all available packages, see the orderable addendum at the end of the data sheet.
2. The package size (length × width) is a nominal value and includes pins, where applicable.

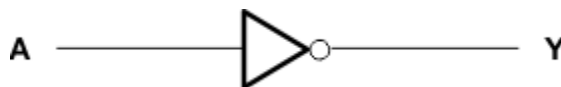


Figure 2-1. Logic Diagram, Each Gate (Positive Logic)



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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision O (May 2023) to Revision P (June 2023) | Page |
|--|-------------|
| • Added BQA package to <i>Device Information</i> table..... | 1 |
| • Added <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Updated thermal values for R θ JA: D = 86 to 124.5, PW = 113 to 147.7, all values in °C/W | 5 |
| • Added thermal value for R θ JA: BQA = 88.3, all values in °C/W..... | 5 |

| Changes from Revision N (May 2013) to Revision O (May 2023) | Page |
|---|-------------|
| • Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table..... | 1 |

4 Pin Configuration and Functions

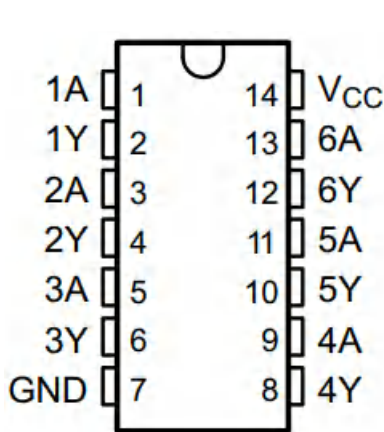


Figure 4-1. SN54AHC04 J or W Package SN74AHC04 D, DB, DGV, N, NS, or PW Package (Top View)

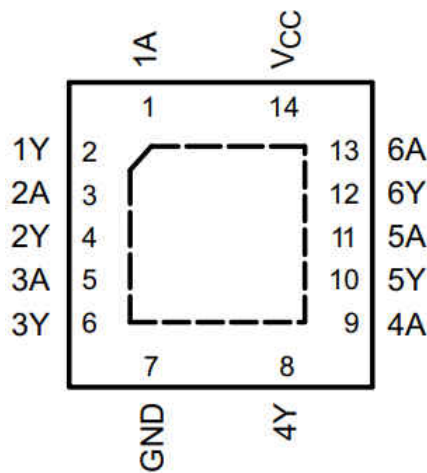


Figure 4-2. SN74AHC04 RGY or BQA Package (Top View)

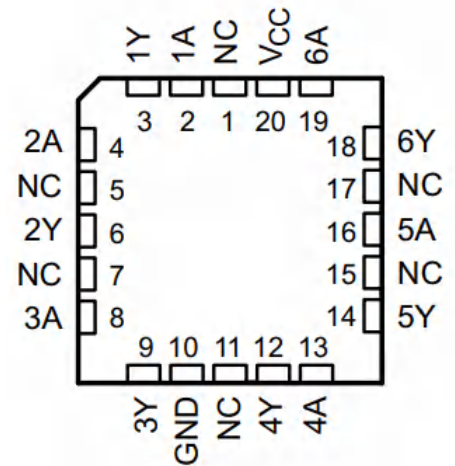


Figure 4-3. SN54AHC04 FK Package (Top View)

Table 4-1. Pin Functions

| NAME | PIN | | | | I/O | DESCRIPTION |
|-----------------|-----------------------|----------|-----------|----|-----|---------------|
| | SN74AHC04 | | SN54AHC04 | | | |
| | D, DB, DGV, N, NS, PW | RGY, BQA | J, W | FK | | |
| 1A | 1 | 1 | 1 | 2 | I | 1A Input |
| 1Y | 2 | 2 | 2 | 3 | O | 1Y Output |
| 2A | 3 | 3 | 3 | 4 | I | 2A Input |
| 2Y | 4 | 4 | 4 | 6 | O | 2Y Output |
| 3A | 5 | 5 | 5 | 8 | I | 3A Input |
| 3Y | 6 | 6 | 6 | 9 | O | 3Y Output |
| 4A | 9 | 9 | 9 | 13 | I | 4A Input |
| 4Y | 8 | 8 | 8 | 12 | O | 4Y Output |
| 5A | 11 | 11 | 11 | 16 | I | 5A Input |
| 5Y | 10 | 10 | 10 | 14 | I | 5Y Output |
| 6A | 13 | 13 | 13 | 19 | I | 6A Input |
| 6Y | 12 | 12 | 12 | 18 | O | 6Y Output |
| GND | 7 | 7 | 7 | 10 | — | Ground Pin |
| NC | — | — | — | 1 | — | No Connection |
| | | | | 5 | | |
| | | | | 7 | | |
| | | | | 11 | | |
| | | | | 15 | | |
| V _{CC} | 14 | 14 | 14 | 20 | — | Power Pin |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------------------------|---|---|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I ⁽²⁾ | Input voltage range | -0.5 | 7 | V |
| V _O ⁽²⁾ | Output voltage range | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | (V _I < 0) | -20 | mA |
| I _{OK} | Output clamp current | (V _O < 0 or V _O > V _{CC}) | ±20 | mA |
| I _{OK} | Continuous output current | (V _O = 0 to V _{CC}) | ±25 | mA |
| | Continuous current through V _{CC} or GND | | ±50 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

| | | SN54AHC04 | | SN74AHC04 | | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|-----------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | 1.5 | | V |
| | | V _{CC} = 3 V | 2.1 | 2.1 | | |
| | | V _{CC} = 5.5 V | 3.85 | 3.85 | | |
| V _{IL} | Low-level Input voltage | V _{CC} = 2 V | | 0.5 | 0.5 | V |
| | | V _{CC} = 3 V | | 0.9 | 0.9 | |
| | | V _{CC} = 5.5 V | | 1.65 | 1.65 | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | -50 | -50 | mA |
| | | V _{CC} = 3.3 V ± 0.3 V | | -4 | -4 | |
| | | V _{CC} = 5 V ± 0.5 V | | -8 | -8 | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | 50 | mA |
| | | V _{CC} = 3.3 V ± 0.3 V | | 4 | 4 | |
| | | V _{CC} = 5 V ± 0.5 V | | 8 | 8 | |
| Δt/Δv | Input Transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | | 100 | 100 | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | | 20 | 20 | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C |

5.4 Thermal Information

| THERMAL METRIC ¹ | | SNx4AHC04 | | | | | | | UNIT | |
|-----------------------------|--|-----------|----|-----|----|----|-------|-----|------|------|
| | | D | DB | DGV | N | NS | PW | RGY | | BQA |
| | | 14 PINS | | | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 124.5 | 96 | 127 | 80 | 76 | 147.7 | 47 | 88.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | T _A = -55°C TO 125°C | | T _A = -40°C TO 85°C | | T _A = -40°C TO 125°C | | UNIT |
|-----------------|---|-----------------|-----------------------|-----|---------------------------------|-----|--------------------------------|-----|---------------------------------|-----|------|
| | | | | | SN54AHC04 | | SN74AHC04 | | Recommended SN74AHC04 | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | 1.9 | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | 3 | 2.9 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | 4.4 | | 4.4 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | 2.48 | | 2.48 | | 2.48 | | |
| | | 4.5 V | 3.94 | | 3.8 | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | | |
| | I _{OH} = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | | |
| | | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1 ⁽¹⁾ | | ±1 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 2 | | 20 | | 20 | | μA |
| C _i | V _I = V _{CC} or GND | 5 V | | | 2 | | 10 | | 10 | | pF |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | T _A = -55°C TO 125°C | | T _A = -40°C TO 85°C | | T _A = -40°C TO 125°C | | UNIT |
|------------------|--------------|-------------|------------------------|-----------------------|--------------------|---------------------------------|---------------------|--------------------------------|------|---------------------------------|------|------|
| | | | | | | SN54AHC04 | | SN74AHC04 | | Recommended SN74AHC04 | | |
| | | | | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | 5 ⁽¹⁾ | 8.9 ⁽¹⁾ | 1 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 | 10.5 | 1 | 10.5 | ns |
| t _{PHL} | | | | 5 ⁽¹⁾ | 8.9 ⁽¹⁾ | 1 ⁽¹⁾ | 10.5 ⁽¹⁾ | 1 | 10.5 | 1 | 10.5 | |
| t _{PLH} | A | Y | C _L = 50 pF | 7.5 | 11.4 | 1 | 13 | 1 | 13 | 1 | 13 | ns |
| t _{PHL} | | | | 7.5 | 11.4 | 1 | 13 | 1 | 13 | 1 | 13 | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A = 25^\circ\text{C}$ | | $T_A = -55^\circ\text{C TO } 125^\circ\text{C}$ | | $T_A = -40^\circ\text{C TO } 85^\circ\text{C}$ | | $T_A = -40^\circ\text{C TO } 125^\circ\text{C}$ | | UNIT |
|-----------|--------------|-------------|----------------------|--------------------------|------------------|---|------------------|--|-----|---|-----|------|
| | | | | TYP | MAX | SN54AHC04 | | SN74AHC04 | | Recommended | | |
| | | | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{ pF}$ | 3.8 ¹ | 5.5 ¹ | 1 ¹ | 6.5 ¹ | 1 | 6.5 | 1 | 6.5 | ns |
| t_{PHL} | | | | 3.8 ¹ | 5.5 ¹ | 1 ¹ | 6.5 ¹ | 1 | 6.5 | 1 | 6.5 | |
| t_{PLH} | A | Y | $C_L = 50\text{ pF}$ | 5.3 | 7.5 | 1 | 8.5 | 1 | 8.5 | 1 | 8.5 | ns |
| t_{PHL} | | | | 5.3 | 7.5 | 1 | 8.5 | 1 | 8.5 | 1 | 8.5 | |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

| PARAMETER | | SN74AHC04 | | | UNIT |
|-------------|--|-----------|------|-----|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.4 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.4 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

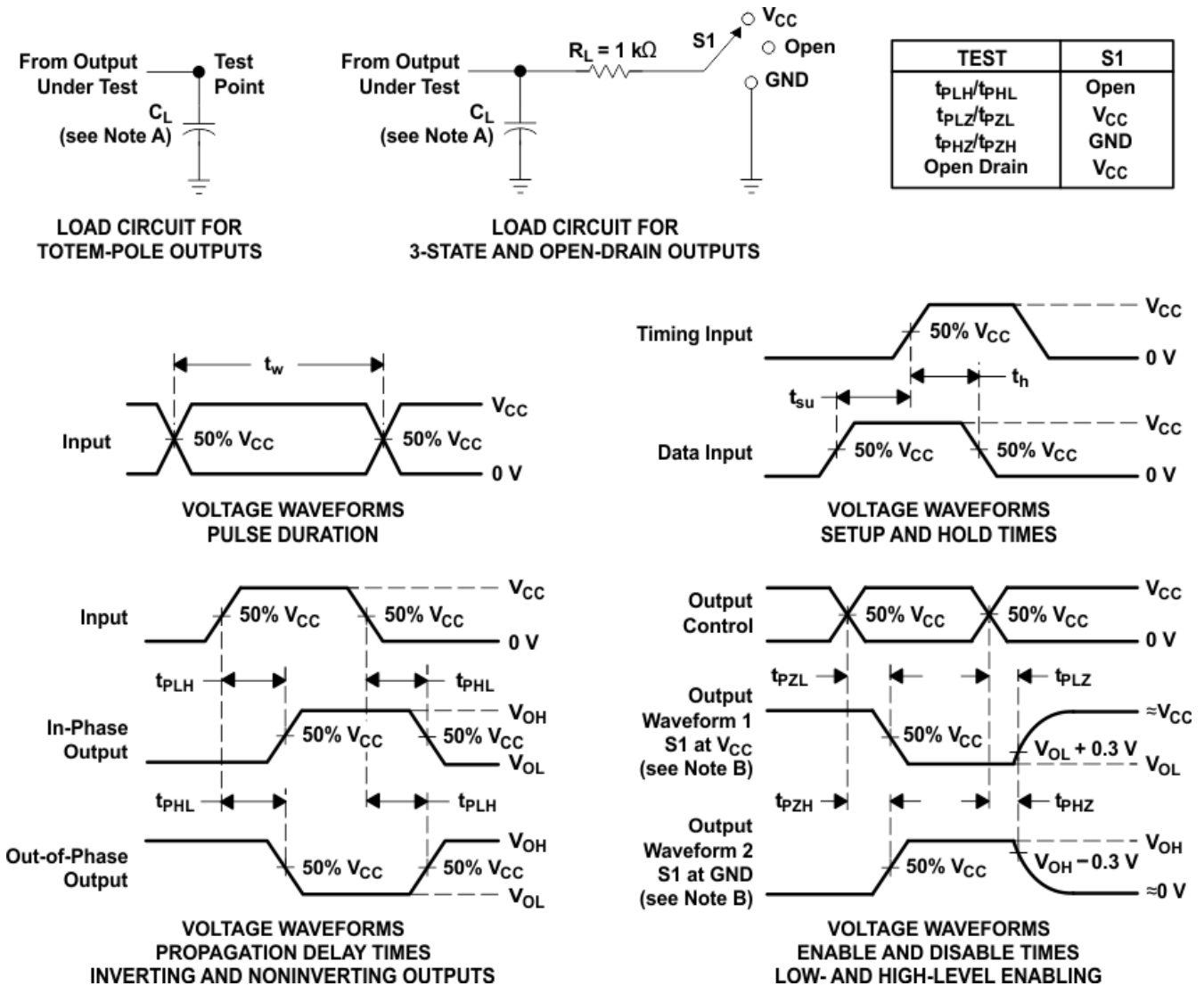
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|-----------|-------------------------------|-----------------|--------------------|-----|------|
| C_{pd} | Power dissipation capacitance | No load, | $f = 1\text{ MHz}$ | 12 | pF |

6 Parameter Measurement Information

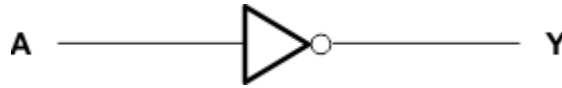


- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram



7.2 Device Functional Modes

**Table 7-1. Function Table
(Each Inverter)**

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | L |
| L | H |

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AHC04 | Click here | Click here | Click here | Click here | Click here |
| SN74AHC04 | Click here | Click here | Click here | Click here | Click here |

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|---------------------------------|-------------------------|
| 5962-9680501Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501Q2A SNJ54AHC04FK | Samples |
| 5962-9680501QCA | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501QCA SNJ54AHC04J | Samples |
| 5962-9680501QDA | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501QDA SNJ54AHC04W | Samples |
| SN74AHC04BQAR | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC04 | Samples |
| SN74AHC04D | OBSOLETE | SOIC | D | 14 | | TBD | Call TI | Call TI | -40 to 125 | AHC04 | |
| SN74AHC04DBR | ACTIVE | SSOP | DB | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA04 | Samples |
| SN74AHC04DGVR | ACTIVE | TVSOP | DGV | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA04 | Samples |
| SN74AHC04DR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC04 | Samples |
| SN74AHC04N | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHC04N | Samples |
| SN74AHC04NSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC04 | Samples |
| SN74AHC04PW | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI | -40 to 125 | HA04 | |
| SN74AHC04PWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA04 | Samples |
| SN74AHC04RGYR | ACTIVE | VQFN | RGY | 14 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | HA04 | Samples |
| SNJ54AHC04FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501Q2A SNJ54AHC04FK | Samples |
| SNJ54AHC04J | ACTIVE | CDIP | J | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501QCA SNJ54AHC04J | Samples |
| SNJ54AHC04W | ACTIVE | CFP | W | 14 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9680501QDA SNJ54AHC04W | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| | | | | | | | | | | SNJ54AHC04W | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC04, SN74AHC04 :

- Catalog : [SN74AHC04](#)

- Automotive : [SN74AHC04-Q1](#), [SN74AHC04-Q1](#)
- Enhanced Product : [SN74AHC04-EP](#), [SN74AHC04-EP](#)
- Military : [SN54AHC04](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC04BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74AHC04DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74AHC04DGVR | TVSOP | DGV | 14 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC04DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74AHC04NSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC04PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC04RGYR | VQFN | RGY | 14 | 3000 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC04BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74AHC04DBR | SSOP | DB | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC04DGVR | TVSOP | DGV | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC04DR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| SN74AHC04NSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC04PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC04RGYR | VQFN | RGY | 14 | 3000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9680501Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9680501QDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC04N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AHC04N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC04FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC04W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

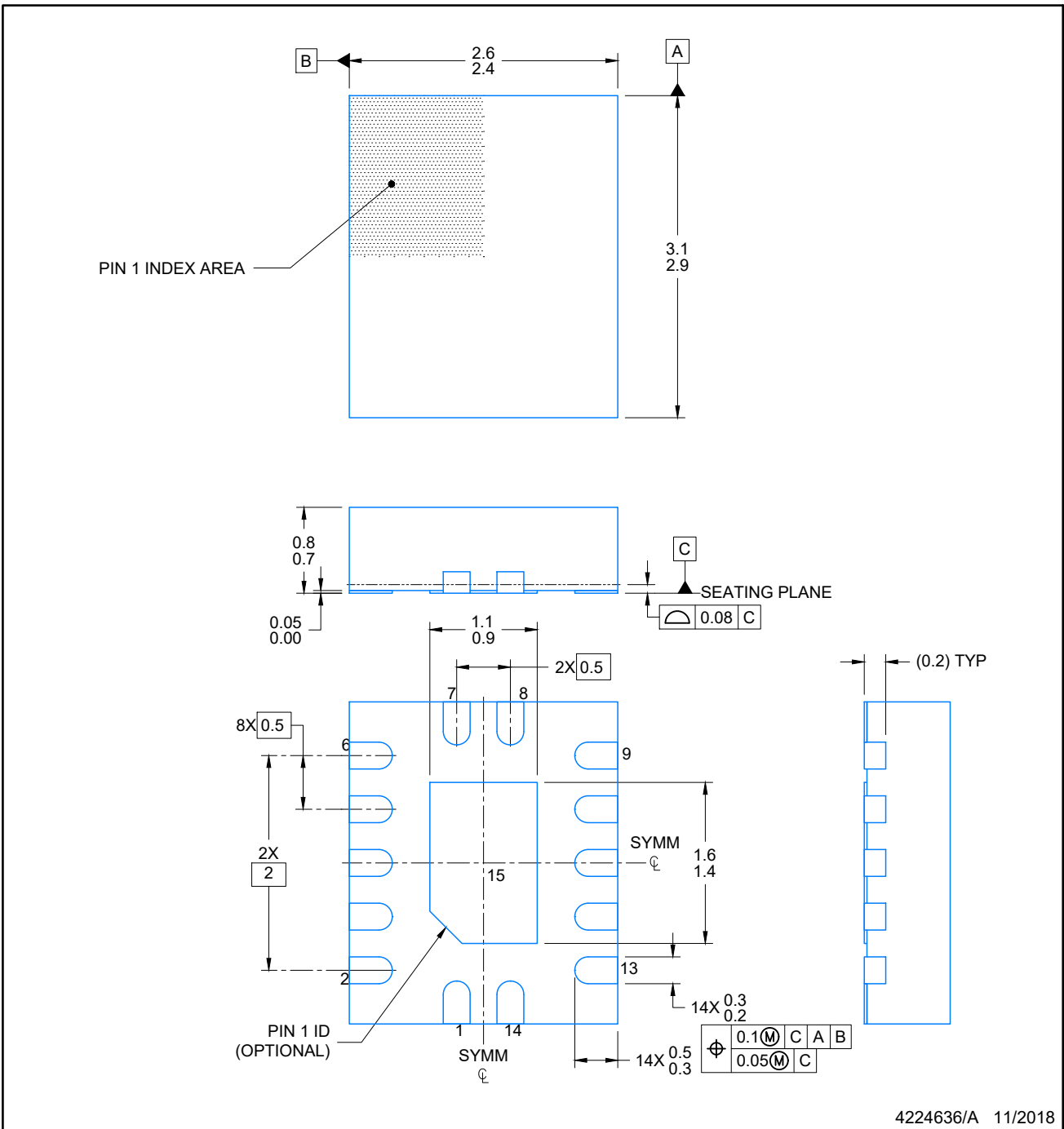
2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



4224636/A 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW
CDIP - 5.08 mm max height
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A



PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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