SN74AHC240-Q1 Automotive Octal Buffers/Drivers With 3-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: -40°C to +125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Operating range 2V to 5.5V V_{CC}
- Low delay, 6ns typ (25°C, 5V)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Handset: smartphone
- Network switch
- Health fitness and wearables

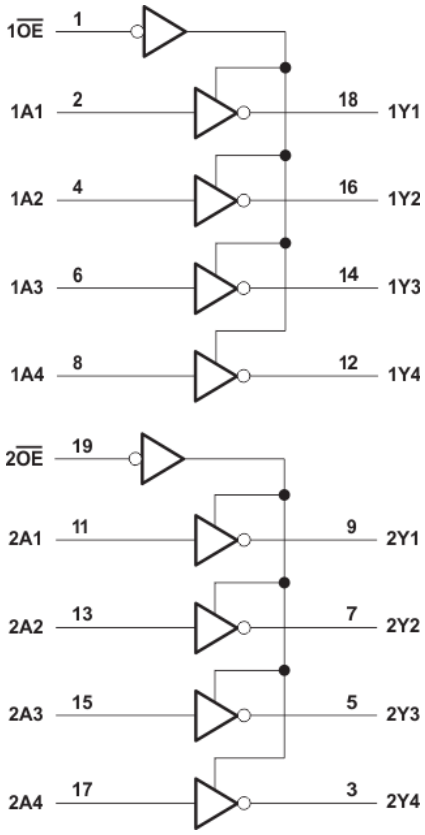
3 Description

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)(3)
SN74AHC240-Q1	PW (TSSOP, 20)	6.5mm × 6.4mm	6.5mm × 4.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins..



Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

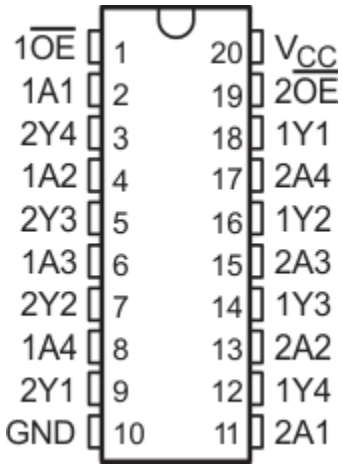


Figure 4-1. SN74AHC240-Q1 PW Package (Top View)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OE	1	O	Output enable 1
1A1	2	I	1A1 input
2Y4	3	O	2Y4 output
1A2	4	I	1A2 input
2Y3	5	O	2Y3 output
1A3	6	I	1A3 input
2Y2	7	O	2Y2 output
1A4	8	I	1A4 input
2Y1	9	O	2Y1 output
GND	10	G	Ground pin
2A1	11	I	2A1 input
1Y4	12	O	1Y4 output
2A2	13	I	2A2 input
1Y3	14	O	1Y3 output
2A3	15	I	2A3 input
1Y2	16	O	1Y2 output
2A4	17	I	2A4 input
1Y1	18	O	1Y1 output
2OE	19	O	Output enable 2
VCC	20	P	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < -0.5V		-20	mA
I_{OK}	Output clamp current	V_O < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous output current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 3V	2.1		
		V_{CC} = 5.5V	3.85		
V_{IL}	Low-Level input voltage	V_{CC} = 2V		0.5	V
	Low-Level input voltage	V_{CC} = 3V		0.9	
	Low-Level input voltage	V_{CC} = 5.5V		1.65	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2V		-50	µA
		V_{CC} = 3.3V ± 0.3V		-4	mA
		V_{CC} = 5V ± 0.5V		-8	mA
I_{OL}	Low-level output current	V_{CC} = 2V		50	µA
		V_{CC} = 3.3V ± 0.3V		4	mA
		V_{CC} = 5V ± 0.5V		8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3V ± 0.3V		100	ns/V
		V_{CC} = 5V ± 0.5V		20	ns/V
T_A	Operating free-air temperature		–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = –50µA	2V to 5.5V	V_{CC}-0.1	V_{CC}		V_{CC}-0.1	V_{CC}		V
	I_{OH} = –4mA	3V	2.58			2.48			
	I_{OH} = –8mA	4.5V	3.94			3.8			
V_{OL}	I_{OL} = 50µA	2V to 5.5V			0.1			0.1	V
	I_{OL} = 4mA	3V			0.36			0.44	
	I_{OL} = 8mA	4.5V			0.36			0.44	
I_I	V_I = 5.5V or GND and V_{CC} = 0V to 5.5V	0V to 5.5V			±0.1			±1	µA
I_{OZ}	V_O = V_{CC} or GND and V_{CC} = 5.5V	5.5V			±0.25			±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0, and V_{CC} = 5.5V	5.5V			4			40	µA
C_I	V_I = V_{CC} or GND	5V		2	10			10	pF
C_O	Vo = V_{CC} or GND	5V		5					pF
C_{PD}	No load, F = 1MHz	5V		15					pF

5.6 Switching Characteristics

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A	Y	C_L = 15pF	2V			19.5	1		23	ns
t_{PHL}							19.5	1		23	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	2V			25.5	1		30	ns
t_{PZL}							25.5	1		30	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	2V			25.5	1		30	ns
t_{PLZ}							25.5	1		30	ns
t_{PLH}	A	Y	C_L = 15pF	3.3V		5.3	7.5	1		9	ns
t_{PHL}						5.3	7.5	1		9	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	3.3V		6.6	10.6	1		12.5	ns
t_{PZL}						6.6	10.6	1		12.5	ns

5.6 Switching Characteristics (continued)

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	3.3V		7.8	11.5	1		12.5	ns
t_{PLZ}						7.8	11.5	1		12.5	ns
t_{PLH}	A	Y	C_L = 15pF	5V		3.6	5.5	1		6.5	ns
t_{PHL}						3.6	5.5	1		6.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	5V		4.7	7.3	1		8.5	ns
t_{PZL}						4.7	7.3	1		8.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	5V		5.2	7.2	1		8.5	ns
t_{PLZ}						5.2	7.2	1		8.5	ns
t_{PLH}	A	Y	C_L = 50pF	2V			26.5	1		30	ns
t_{PHL}							26.5	1		30	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	2V			32.5	1		36.5	ns
t_{PZL}							32.5	1		36.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	2V			32	1		36.5	ns
t_{PLZ}							32	1		36.5	ns
t_{PLH}	A	Y	C_L = 50pF	3.3V		7.8	11	1		12.5	ns
t_{PHL}						7.8	11	1		12.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	3.3V		9.1	14.1	1		16	ns
t_{PZL}						9.1	14.1	1		16	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	3.3V		10.3	14	1		16	ns
t_{PLZ}						10.3	14	1		16	ns
t_{PLH}	A	Y	C_L = 50pF	5V		5.1	7.5	1		8.5	ns
t_{PHL}						5.1	7.5	1		8.5	ns
t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	5V		6.2	9.3	1		10.5	ns
t_{PZL}						6.2	9.3	1		10.5	ns
t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	5V		6.7	9.2	1		10.5	ns
t_{PLZ}						6.7	9.2	1		10.5	ns
$t_{sk(o)}$			C_L = 50pF	2V			2			2	ns
$t_{sk(o)}$			C_L = 50pF	3.3V			1.5			1.5	ns
$t_{sk(o)}$			C_L = 50pF	5V			1			1	ns

5.7 Noise Characteristics

VCC = 5V, CL = 50pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}				V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}				V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}				V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

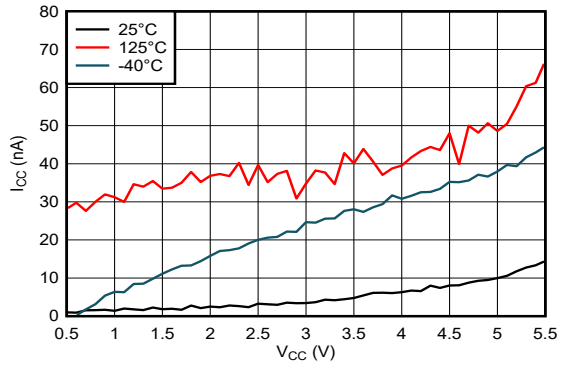


Figure 5-1. Supply Current Across Supply Voltage

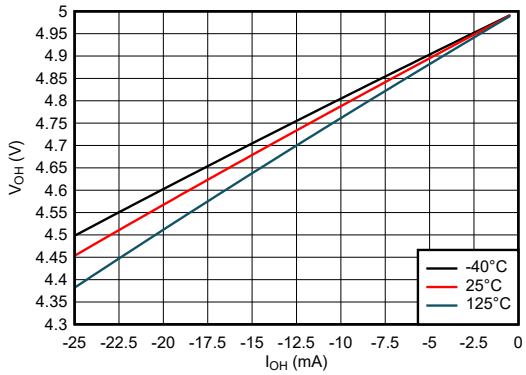


Figure 5-2. Output Voltage vs Current in HIGH State; 5V Supply

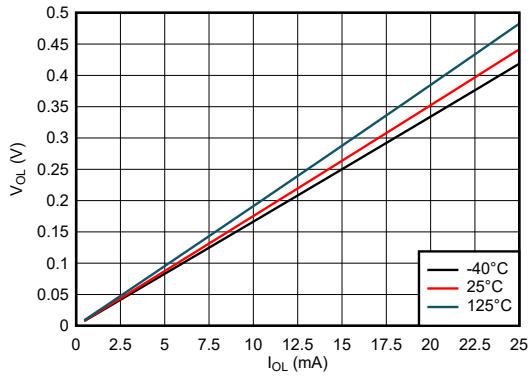


Figure 5-3. Output Voltage vs Current in LOW State; 5V Supply

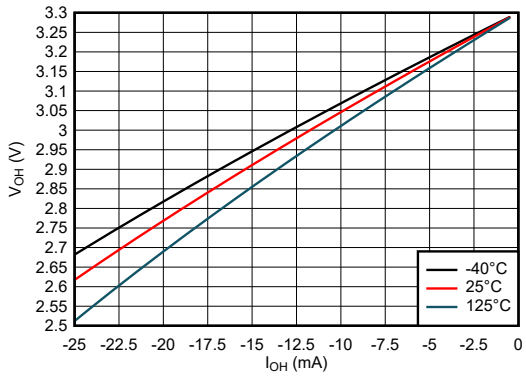


Figure 5-4. Output Voltage vs Current in HIGH State; 3.3V Supply

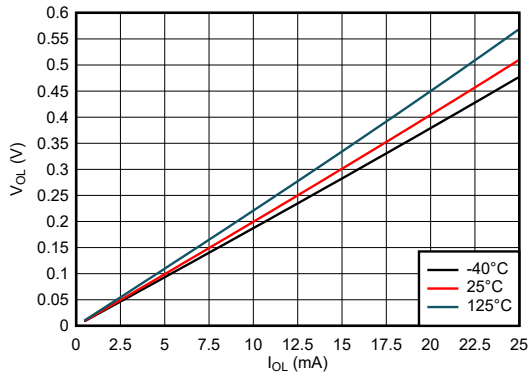


Figure 5-5. Output Voltage vs Current in LOW State; 3.3V Supply

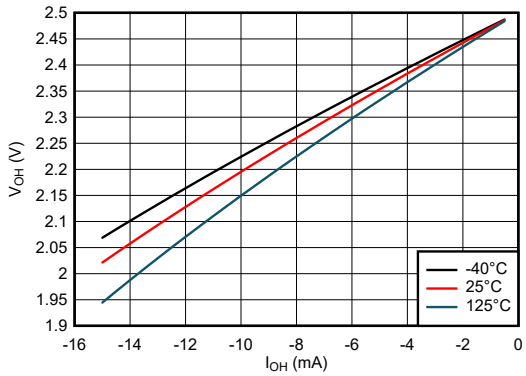


Figure 5-6. Output Voltage vs Current in HIGH State; 2.5V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

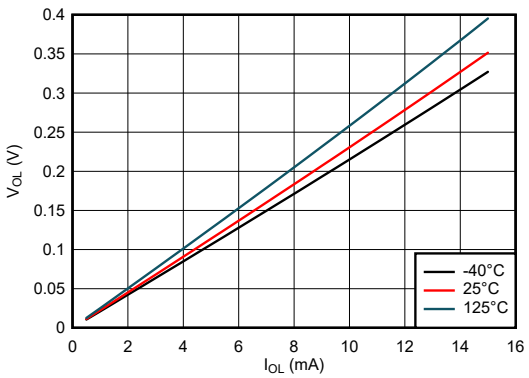


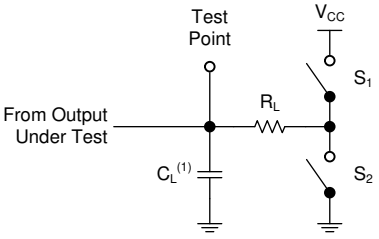
Figure 5-7. Output Voltage vs Current in LOW State; 2.5V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

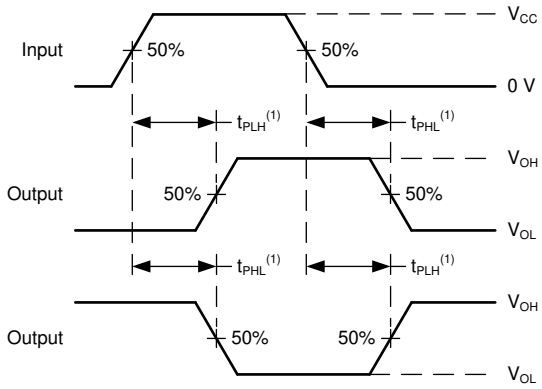
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R_L	C_L	ΔV	V_{CC}
t_{PLH}, t_{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.15V	≤ 2.5V
t_{PLZ}, t_{PZL}	CLOSED	OPEN	1kΩ	15pF, 50pF	0.3V	> 2.5V
t_{PHZ}, t_{PZH}	OPEN	CLOSED	1kΩ	15pF, 50pF	0.3V	> 2.5V



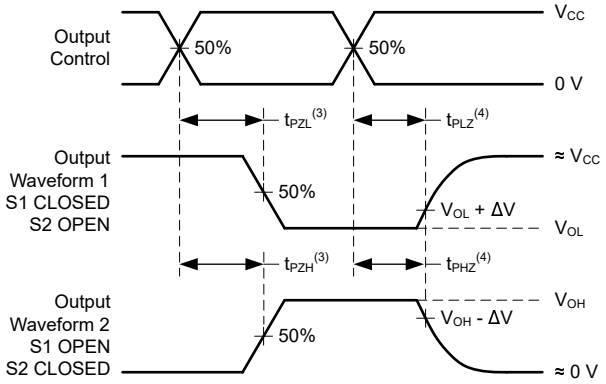
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

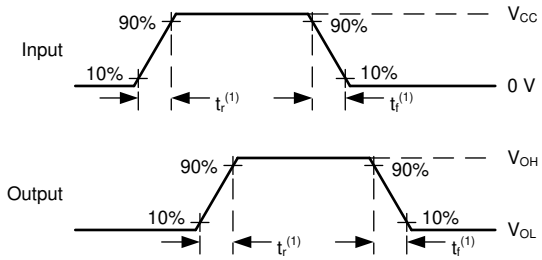
Figure 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AHC240-Q1 devices are organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To place the device in the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

7.2 Functional Block Diagram

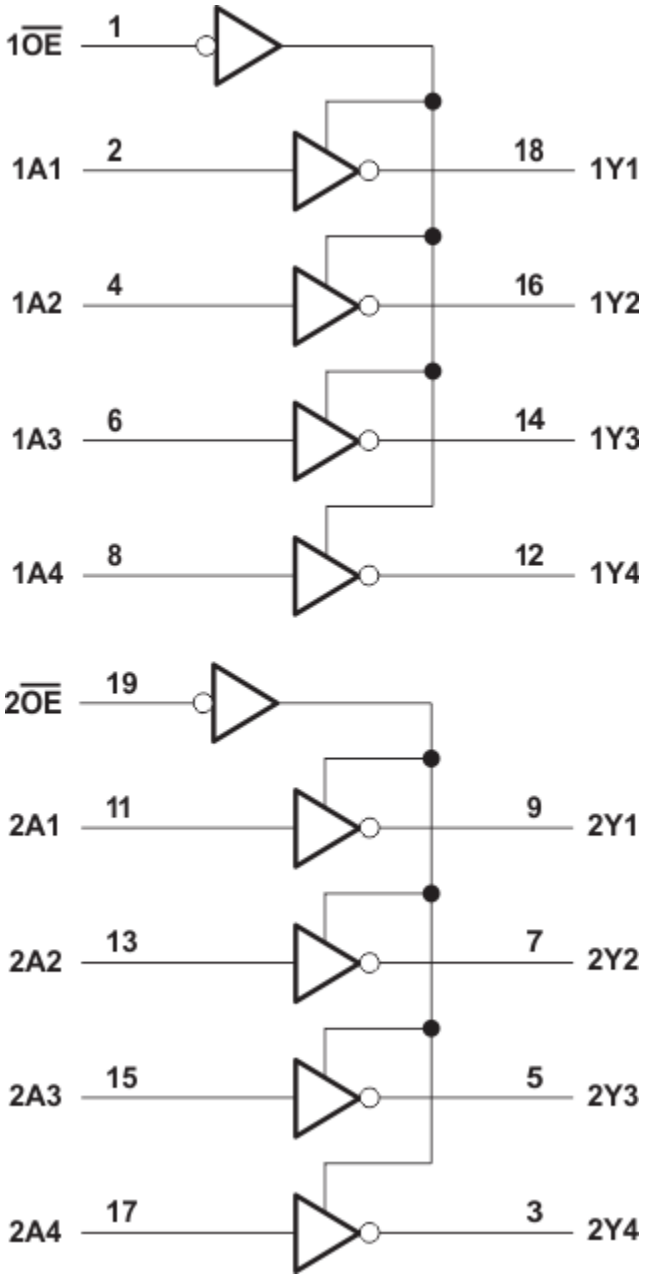


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As Figure 7-2 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

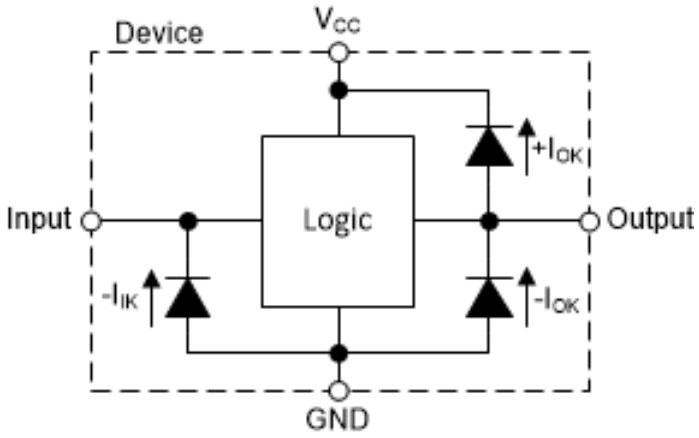


Figure 7-2. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table
(Each Buffer)

INPUTS(1)		OUTPUT(2)
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AHC240-Q1 device is a high drive CMOS device that can be used for a multitude of bus-interface type applications where the data needs to be retained or latched. It can produce 24mA of drive current at 3.3V making it ideal for driving multiple outputs and also good for high-speed applications up to 100MHz. The inputs are 5.5V tolerant allowing it to translate down to V_{CC}.

8.2 Typical Application

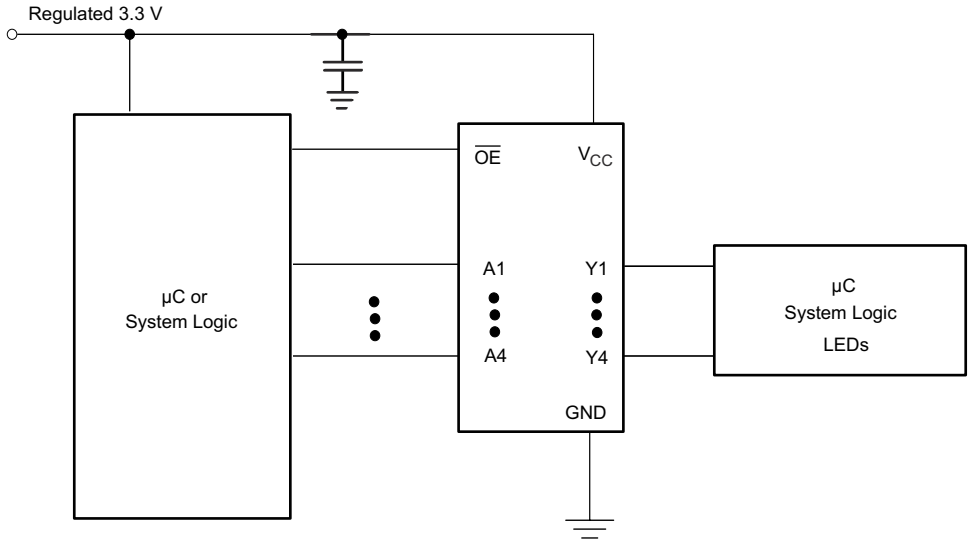


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - Rise time and fall time specs: See (Δt/ΔV) in the *Recommended Operating Conditions* table.
   - Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC}.
2. Recommend Output Conditions
   - Load currents should not exceed 25mA per output and 50mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

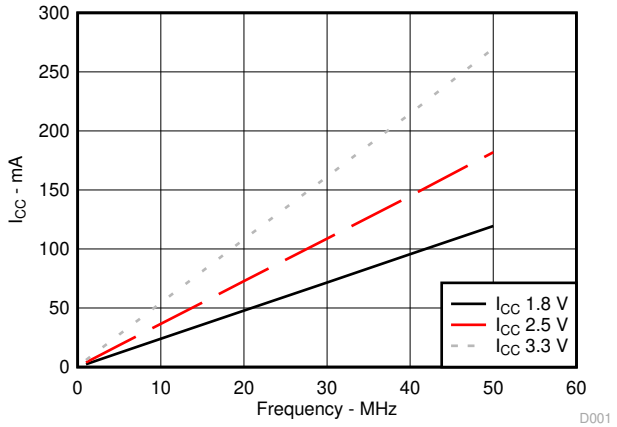


Figure 8-2. I_{CC} vs Frequency

8.3 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 5.3*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1µF and if there are multiple V_{CC} terminals, then TI recommends .01µF or .022µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1µF and 1µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following rules specify what must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever makes more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs, so they cannot float when disabled.

8.4.2 Layout Example

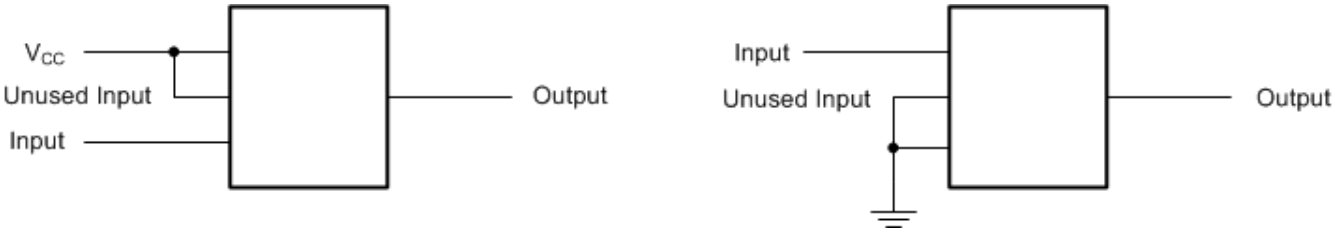


Figure 8-3. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *Understanding Schmitt Triggers*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision * (March 2024) to Revision A (December 2024)	Page
• Changed from Advance Information to Production Data	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC240QDGSRQ1	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA240Q
SN74AHC240QPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC240Q
SN74AHC240QPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC240Q
SN74AHC240QWRKSRQ1	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA240WQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN74AHC240-Q1 :

- Catalog : SN74AHC240
- Military : SN54AHC240

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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