

SN54AHCT158, SN74AHCT158 QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS348J – MAY 1996 – REVISED JULY 2003

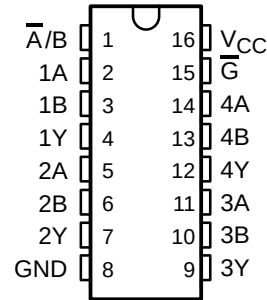
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

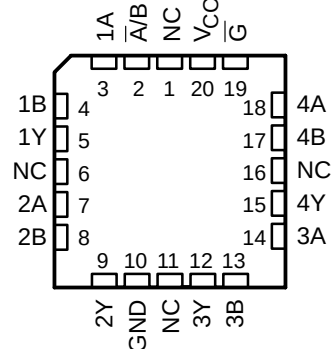
These quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5-V to 5.5-V V_{CC} operation.

The 'AHCT158 devices feature a common strobe ($\bar{G}$) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide inverted data.

SN54AHCT158 . . . J OR W PACKAGE
SN74AHCT158 . . . D, DB, DGV, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHCT158 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHCT158N	SN74AHCT158N
	SOIC – D	Tube	SN74AHCT158D	AHCT158
		Tape and reel	SN74AHCT158DR	
	SOP – NS	Tape and reel	SN74AHCT158NSR	AHCT158
	SSOP – DB	Tape and reel	SN74AHCT158DBR	HB158
	TSSOP – PW	Tube	SN74AHCT158PW	HB158
		Tape and reel	SN74AHCT158PWR	
	TVSOP – DGV	Tape and reel	SN74AHCT158DGVR	HB158
–55°C to 125°C	CDIP – J	Tube	SNJ54AHCT158J	SNJ54AHCT158J
	CFP – W	Tube	SNJ54AHCT158W	SNJ54AHCT158W
	LCCC – FK	Tube	SNJ54AHCT158K	SNJ54AHCT158FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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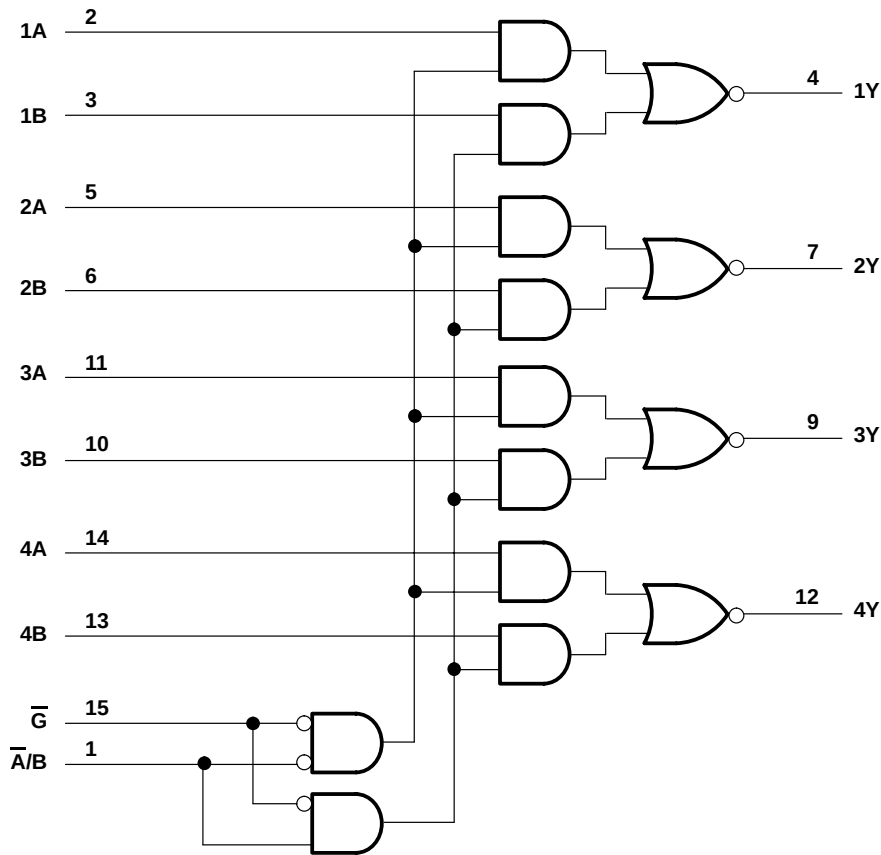
SN54AHCT158, SN74AHCT158
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS348J – MAY 1996 – REVISED JULY 2003

FUNCTION TABLE
(each data selector/multiplexer)

INPUTS				OUTPUT Y
$\overline{G}$	$\overline{A/B}$	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

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SCLS348J – MAY 1996 – REVISED JULY 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	73°C/W
DB package	82°C/W
DGV package	120°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	SN54AHCT158		SN74AHCT158		UNIT
	MIN	MAX	MIN	MAX	
V_{CC} Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH} High-level input voltage	2		2		V
V_{IL} Low-level input voltage		0.8		0.8	V
V_I Input voltage	0	5.5	0	5.5	V
V_O Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH} High-level output current		–8		–8	mA
I_{OL} Low-level output current		8		8	mA
$\Delta t/\Delta v$ Input transition rise or fall time		20		20	ns/V
T_A Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54AHCT158, SN74AHCT158

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS348J – MAY 1996 – REVISED JULY 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHCT158		SN74AHCT158		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	4.5 V	4.4	4.5		4.4		4.4		V
	I _{OH} = –8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	4.5 V			0.1		0.1		0.1	V
	I _{OL} = 8 mA				0.36		0.44		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			2		20		20	µA
ΔI _{CC} [†]	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.5	mA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			SN54AHCT158		SN74AHCT158		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	4.1**	6.4**		1**	7.5**	1	7.5	ns
t _{PHL}				4.1**	6.4**		1**	7.5**	1	7.5	
t _{PLH}	$\overline{A/B}$	Y	C _L = 15 pF	5.3**	8.1**		1**	9.5**	1	9.5	ns
t _{PHL}				5.3**	8.1**		1**	9.5**	1	9.5	
t _{PLH}	$\overline{G}$	Y	C _L = 15 pF	5.6**	8.6**		1**	10**	1	10	ns
t _{PHL}				5.6**	8.6**		1**	10**	1	10	
t _{PLH}	A or B	Y	C _L = 50 pF	5.6	8.7		1	10.8	1	9.8	ns
t _{PHL}				5.6	8.7		1	10.8	1	9.8	
t _{PLH}	$\overline{A/B}$	Y	C _L = 50 pF	6.8	10.4		1	13.2	1	12	ns
t _{PHL}				6.8	10.4		1	13.2	1	12	
t _{PLH}	$\overline{G}$	Y	C _L = 50 pF	7.1	11		1	13.5	1	12	ns
t _{PHL}				7.1	11		1	13.5	1	12	

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

PARAMETER		SN74AHCT158			UNIT
		MIN	TYP	MAX	
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}			0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}			–0.8	V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}		4.8		V
V _{IH(D)}	High-level dynamic input voltage	2			V
V _{IL(D)}	Low-level dynamic input voltage		0.8		V

NOTE 4: Characteristics are for surface-mount packages only.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54AHCT158, SN74AHCT158

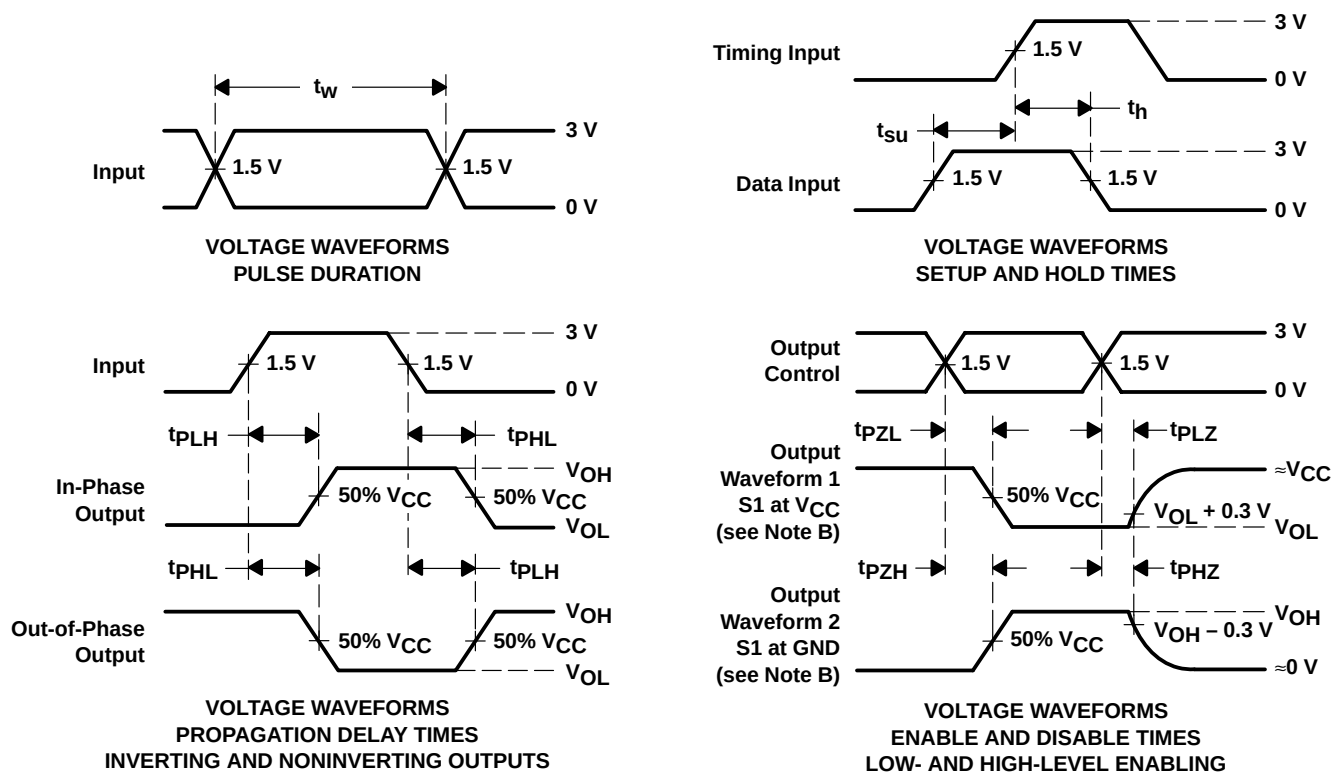
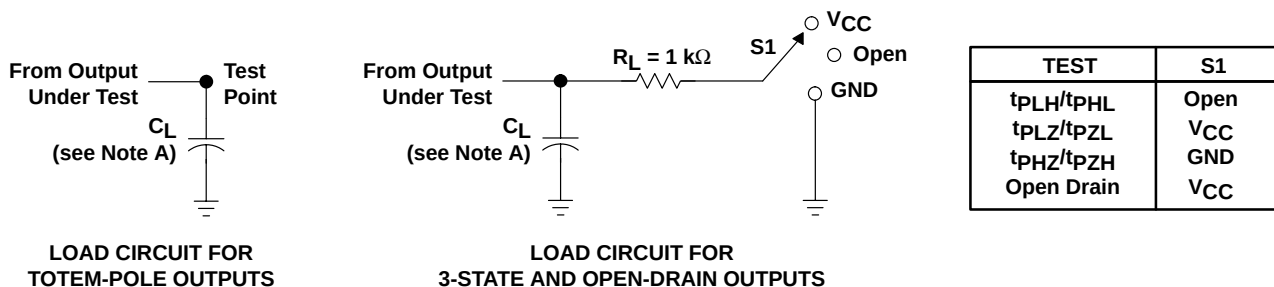
QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

SCLS348J – MAY 1996 – REVISED JULY 2003

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	11	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHCT158D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT158
SN74AHCT158D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHCT158
SN74AHCT158PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-40 to 85	HB158
SN74AHCT158PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB158
SN74AHCT158PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HB158

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

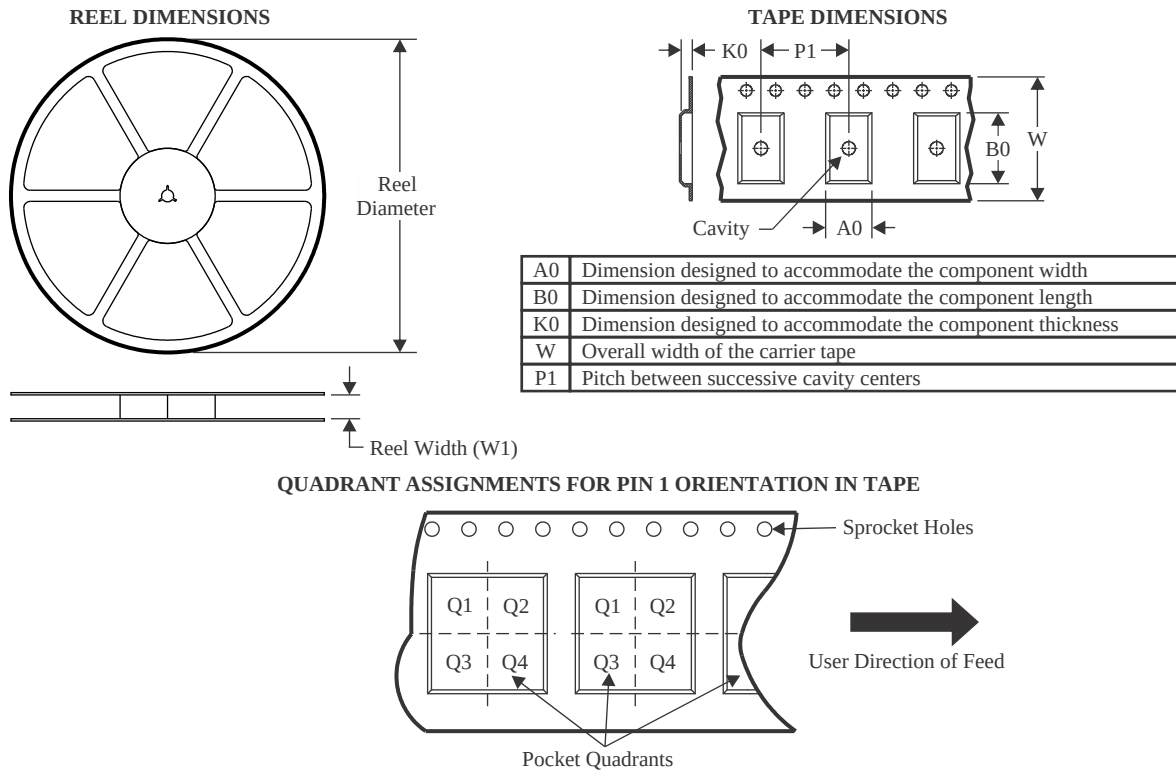
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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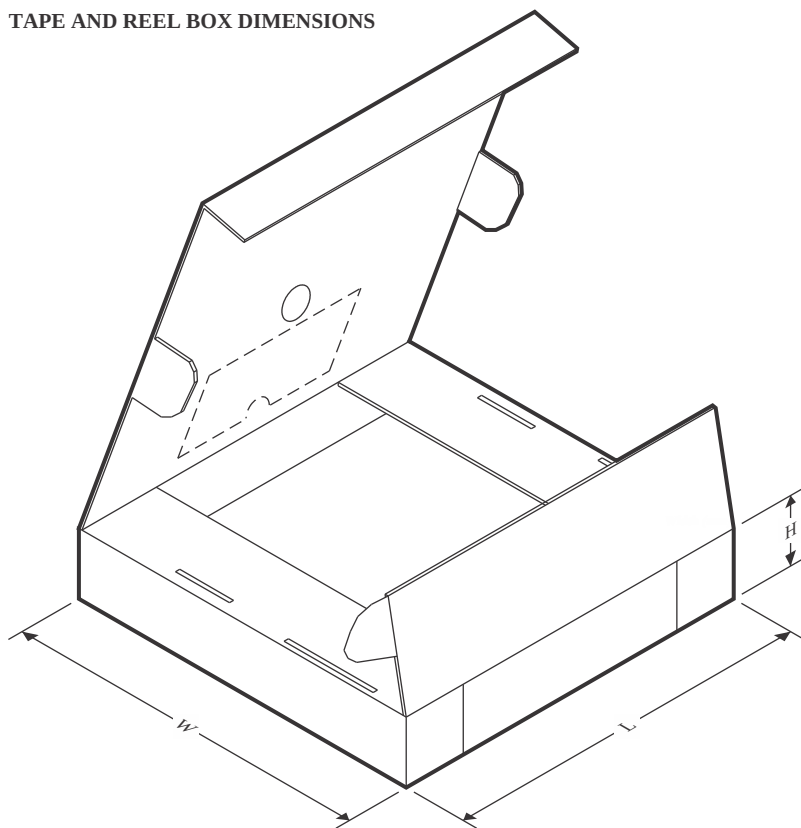
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT158PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

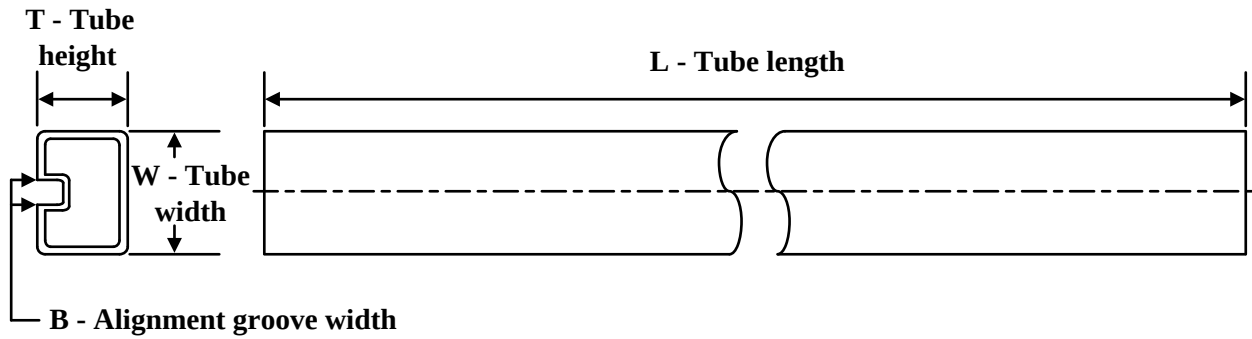
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT158PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE

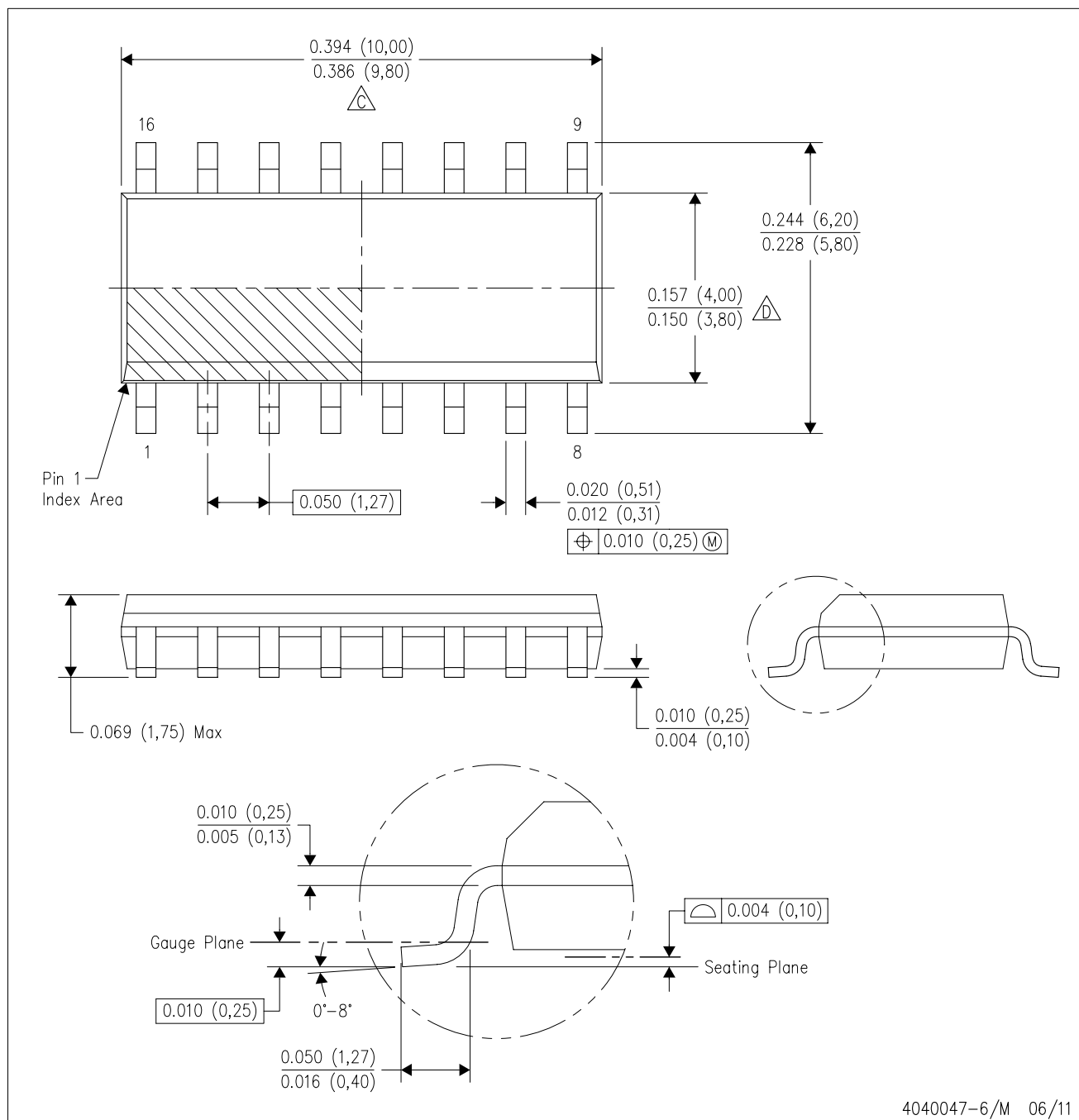


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT158D	D	SOIC	16	40	507	8	3940	4.32
SN74AHCT158D.A	D	SOIC	16	40	507	8	3940	4.32

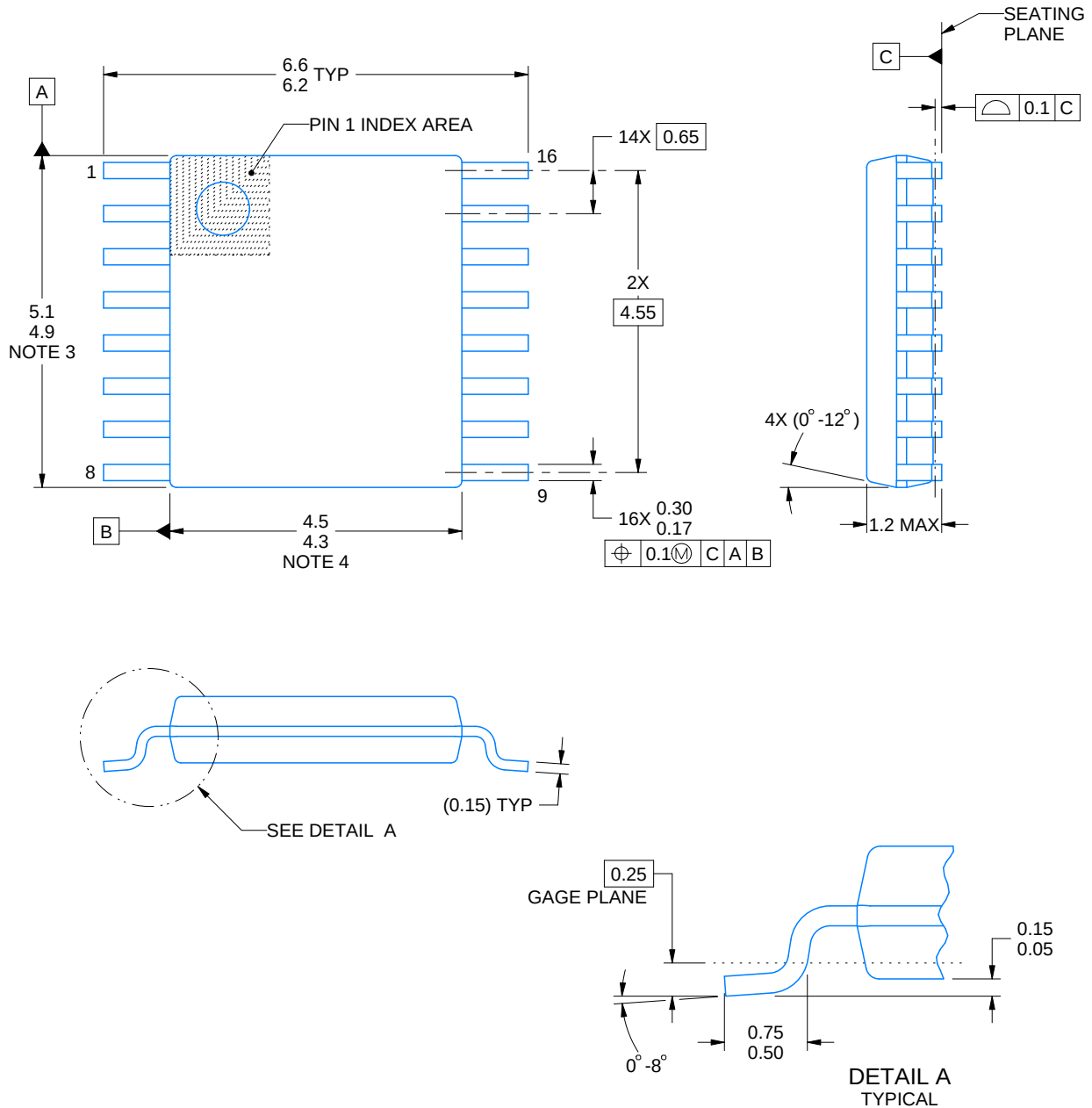
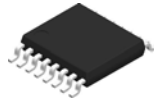
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.



4220204/B 12/2023

NOTES:

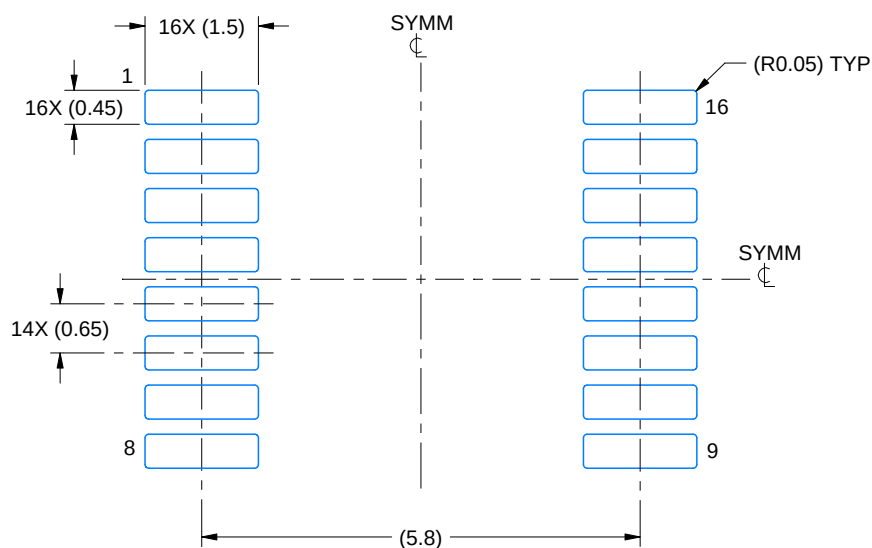
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

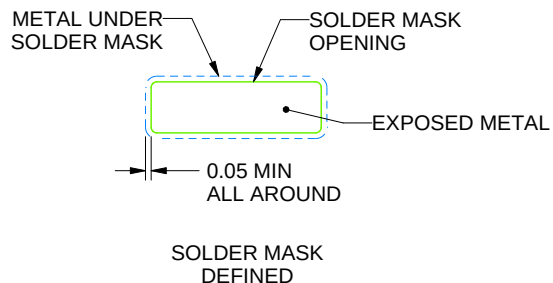
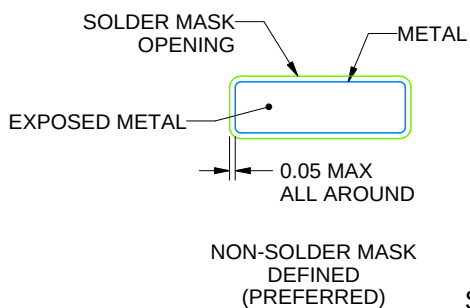
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

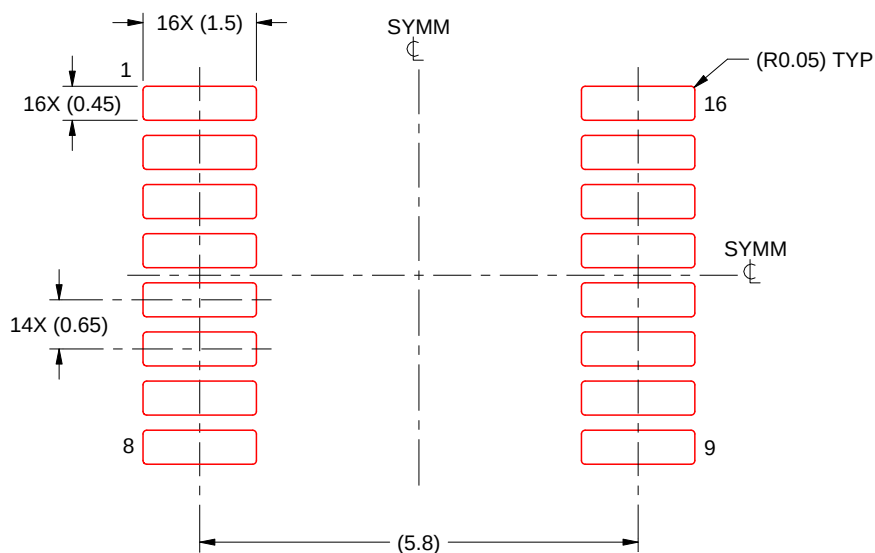
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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