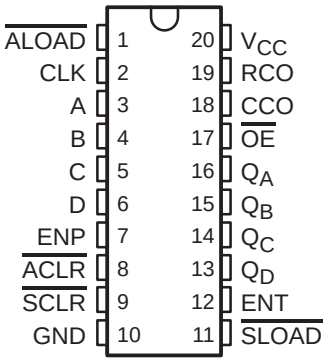
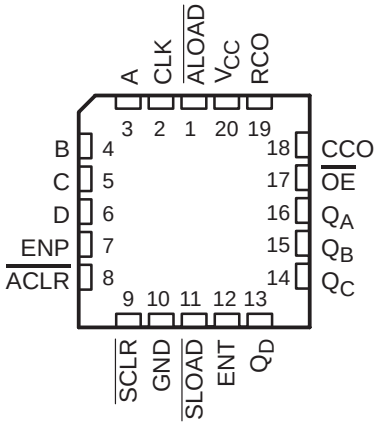
- **Carry Output for n-Bit Cascading**
- **Buffer-Type Outputs Drive Bus Lines Directly**
- **Choice of Asynchronous or Synchronous Clearing and Loading**
- **Internal Look-Ahead Circuitry for Fast Cascading**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54ALS561A . . . J PACKAGE
SN74ALS561A . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS561A . . . FK PACKAGE
(TOP VIEW)



description

These binary counters are programmable and offer synchronous and asynchronous clearing as well as synchronous and asynchronous loading. All synchronous functions are executed on the positive-going edge of the clock.

The clear function is initiated by applying a low level to either asynchronous clear ($\overline{\text{ACLR}}$) or synchronous clear ($\overline{\text{SCLR}}$). $\overline{\text{ACLR}}$ (direct clear) overrides all other functions of the device, while $\overline{\text{SCLR}}$ overrides only the other synchronous functions. Data is loaded from the A, B, C, and D inputs by applying a low level to asynchronous load ($\overline{\text{ALOAD}}$) or by the combination of a low level at synchronous load ($\overline{\text{SLOAD}}$) and a positive-going clock transition. The counting function is enabled only when enable P (ENP), enable T (ENT), $\overline{\text{ACLR}}$, $\overline{\text{ALOAD}}$, $\overline{\text{SCLR}}$, and $\overline{\text{SLOAD}}$ are all high.

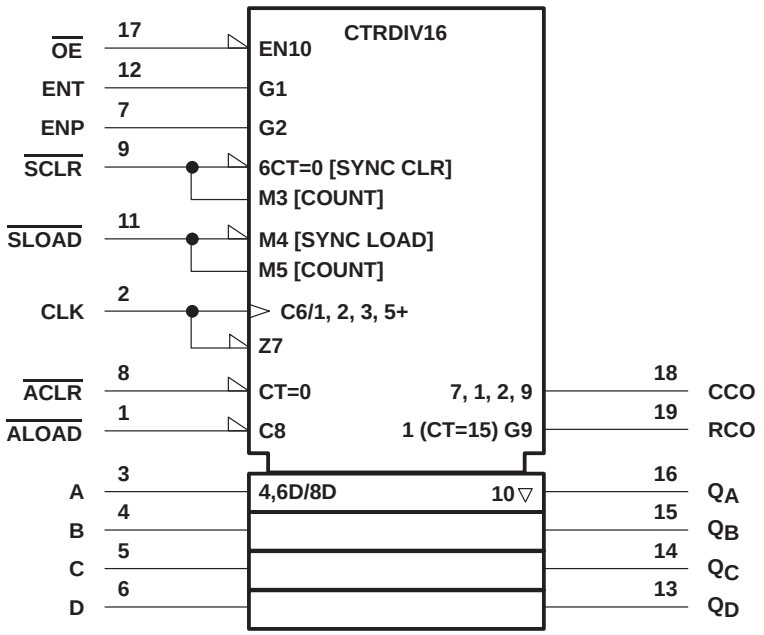
A high level at the output-enable ($\overline{\text{OE}}$) input forces the Q outputs into the high-impedance state, and a low level enables those outputs. Counting is independent of $\overline{\text{OE}}$. ENT is fed forward to enable the ripple-carry output (RCO) to produce a high-level pulse while the count is maximum (15). The clocked carry output (CCO) produces a high-level pulse for a duration equal to that of the low level of the clock when RCO is high and the counter is enabled (ENP and ENT are high); otherwise, CCO is low. CCO does not have the glitches commonly associated with a ripple-carry output. Cascading is normally accomplished by connecting RCO or CCO of the first counter to ENT of the next counter. However, for very high-speed counting, RCO should be used for cascading because CCO does not become active until the clock returns to the low level.

The SN54ALS561A is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS561A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

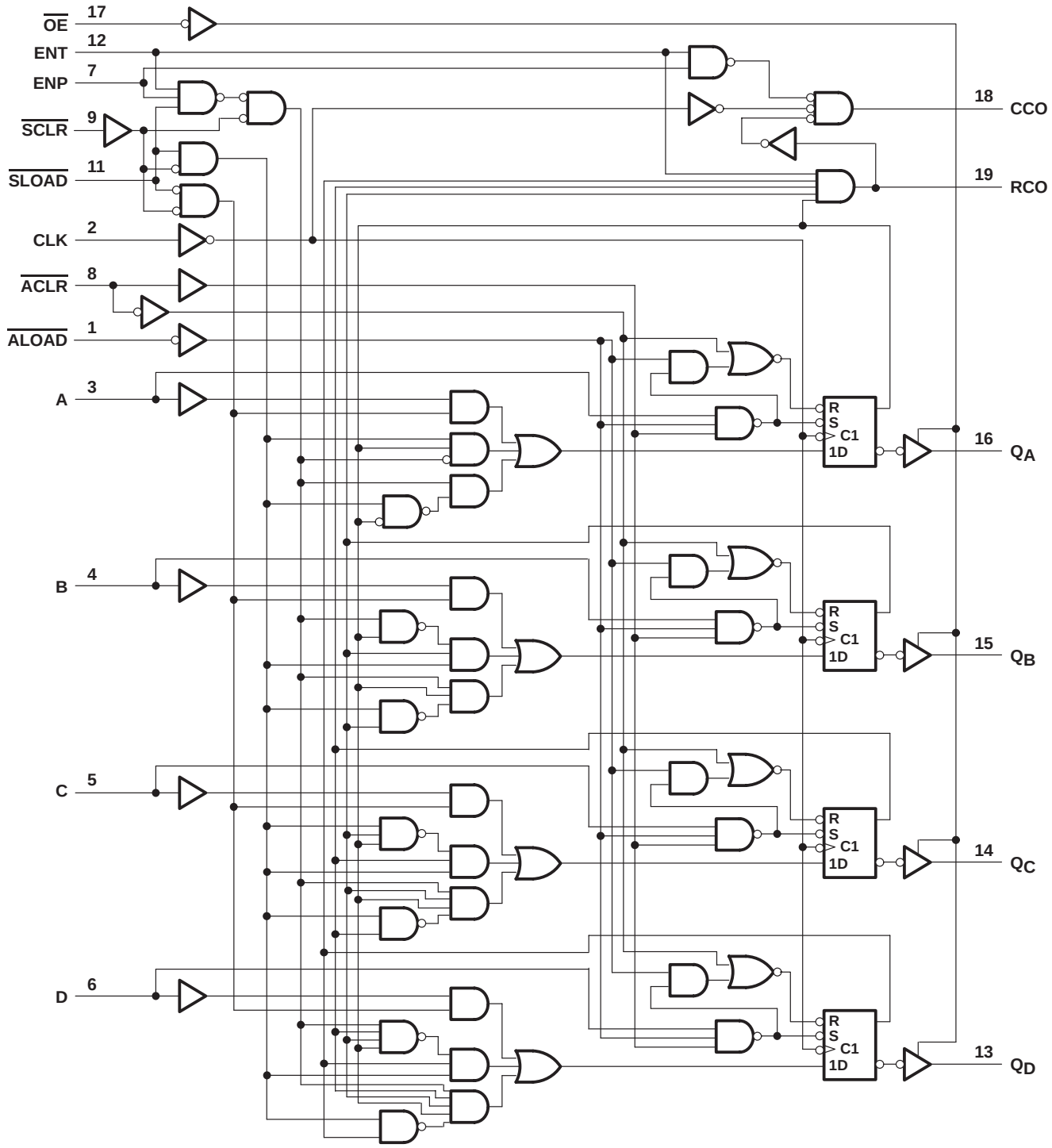
INPUTS								OPERATION
$\overline{OE}$	$\overline{ACLR}$	$\overline{ALOAD}$	$\overline{SCLR}$	$\overline{SLOAD}$	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

logic symbol†

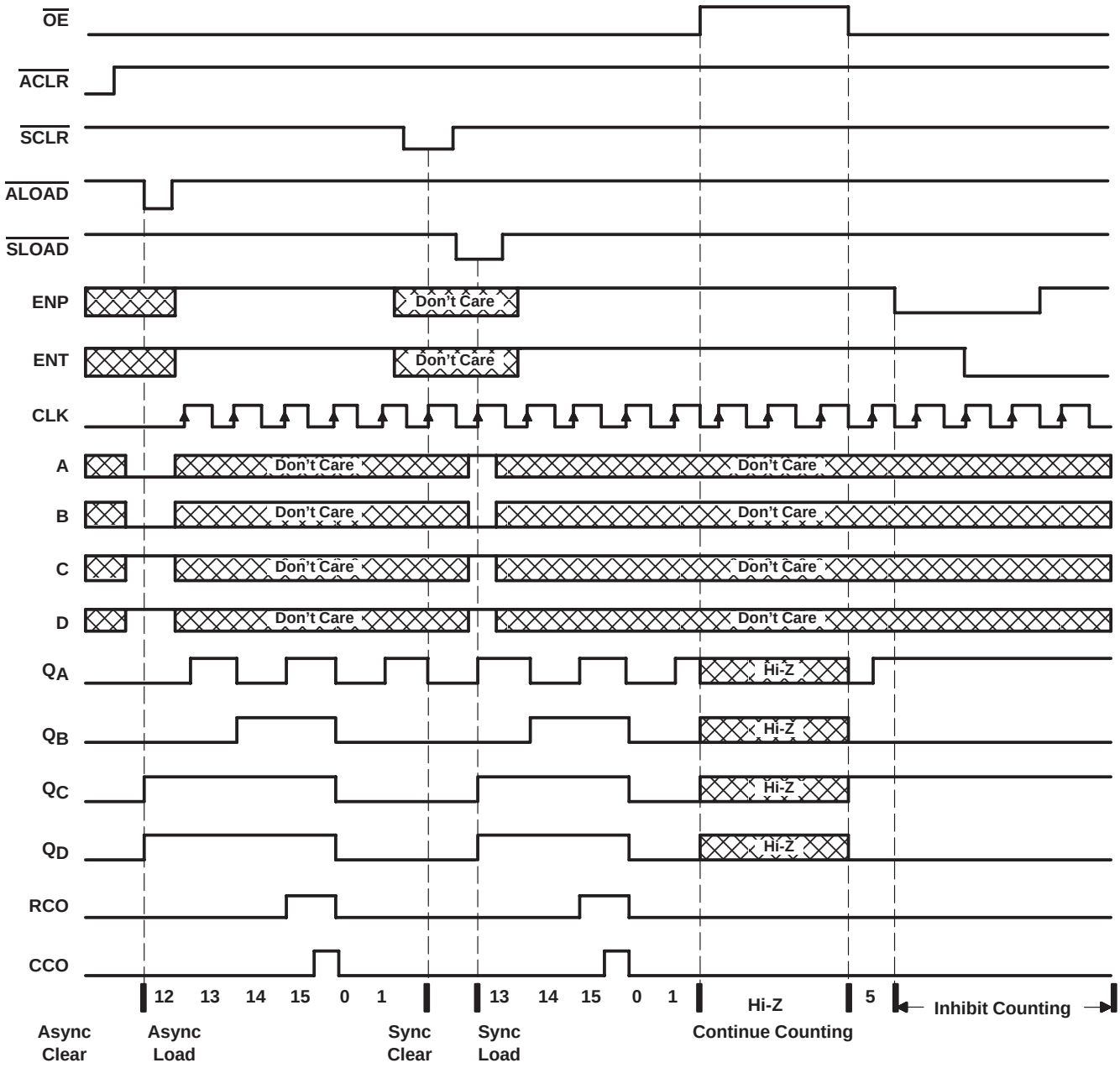


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



typical load, count, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54ALS561A . . . . . –55°C to 125°C
SN74ALS561A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

				SN54ALS561A			SN74ALS561A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
I_{OH}	High-level output current	Q outputs				–1			–2.6	mA
		CCO and RCO				–0.4			–0.4	
I_{OL}	Low-level output current	Q outputs				12			24	mA
		CCO and RCO				4			8	
f_{clock}	Clock frequency			0		20	0		30	MHz
t_w	Pulse duration	$\overline{ACLR}$ or $\overline{ALOAD}$ low		20			15			ns
		CLK high		20			16.5			
		CLK low		25			16.5			
t_{su}	Setup time before CLK↑	ENP, ENT	High	25			20			ns
			Low	25			20			
		Data at A, B, C, D		25			20			
		$\overline{SCLR}$	Low	21			15			
			High (inactive)	35			30			
		$\overline{SLOAD}$	Low	20			15			
			High (inactive)	35			30			
		$\overline{ACLR}$ or $\overline{ALOAD}$ inactive		12			10			
t_h	Hold time after CLK↑ for data, ENP, ENT, $\overline{SCLR}$, or $\overline{SLOAD}$			0			0			ns
T_A	Operating free-air temperature			–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS561A			SN74ALS561A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V_{CC} –2			V
	Q outputs	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3					
			I_{OH} = –2.6 mA				2.4	3.2		
V_{OL}	Q outputs	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
	CCO and RCO	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I	ENP and ENT	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	Other inputs					0.1			0.1	
I_{IH}	ENP and ENT	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	µA
	Other inputs					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2			–0.2	mA
I_O‡	CCO and RCO	V_{CC} = 5.5 V,	V_O = 2.25 V	–15		–70	–15		–70	mA
	Q			–20		–112	–30		–112	
I_{CC}		V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		21	33		21	33	
			Outputs disabled		22	36		22	36	

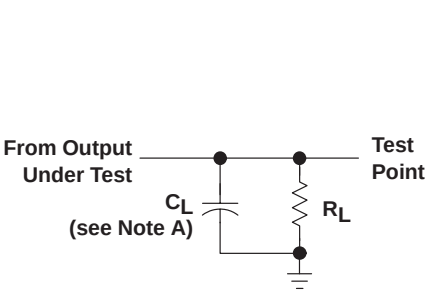
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

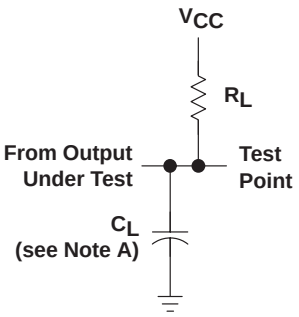
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			SN54ALS561A		SN74ALS561A		
			MIN	MAX	MIN	MAX	
f_{max}			20		30		MHz
t_{PLH}	CLK	Any Q	4	15	4	12	ns
t_{PHL}			5	21	5	18	
t_{PLH}	CLK	RCO	9	35	9	29	ns
t_{PHL}			8	29	8	24	
t_{PLH}	CLK	CCO	8	35	8	26	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{\text{ALOAD}}$	Any Q	10	38	10	35	ns
t_{PHL}			7	27	7	23	
t_{PLH}	$\overline{\text{ALOAD}}$	RCO	15	50	15	40	ns
t_{PHL}			12	35	12	30	
t_{PLH}	$\overline{\text{ALOAD}}$	CCO	25	65	25	55	ns
t_{PHL}			12	42	12	33	
t_{PLH}	A, B, C, or D	Any Q	8	35	8	30	ns
t_{PHL}			7	27	7	22	
t_{PLH}	ENT	RCO	5	20	5	16	ns
t_{PHL}			4	18	4	14	
t_{PLH}	ENT	CCO	12	35	12	32	ns
t_{PHL}			4	15	4	12	
t_{PLH}	ENP	CCO	5	22	5	18	ns
t_{PHL}			4	14	4	12	
t_{PHL}	$\overline{\text{ACLR}}$	Any Q	7	28	7	22	ns
t_{PZH}	$\overline{\text{OE}}$	Any Q	5	24	5	19	ns
t_{PZL}			8	28	8	23	
t_{PHZ}	$\overline{\text{OE}}$	Any Q	2	12	2	10	ns
t_{PLZ}			2	20	4	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

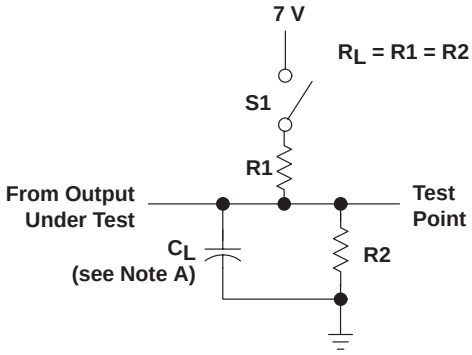
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



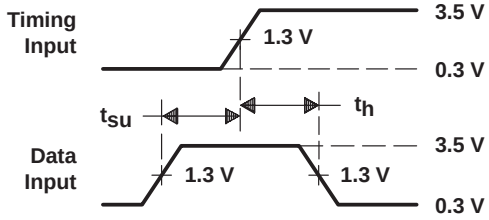
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



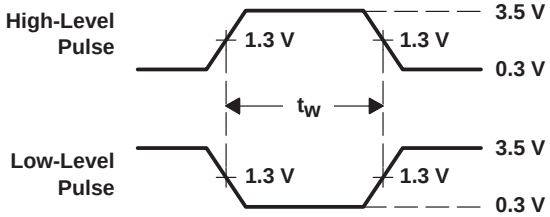
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



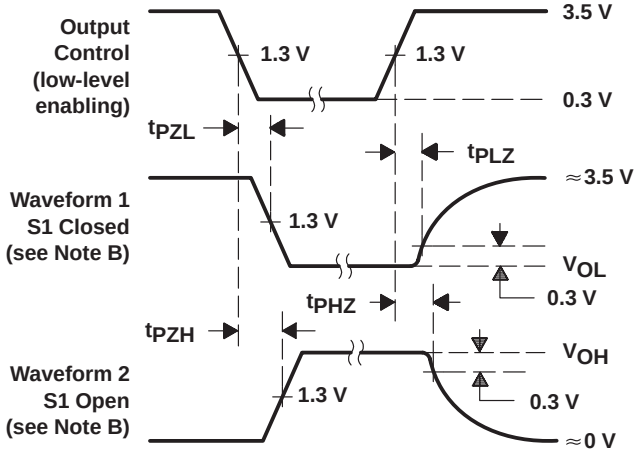
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



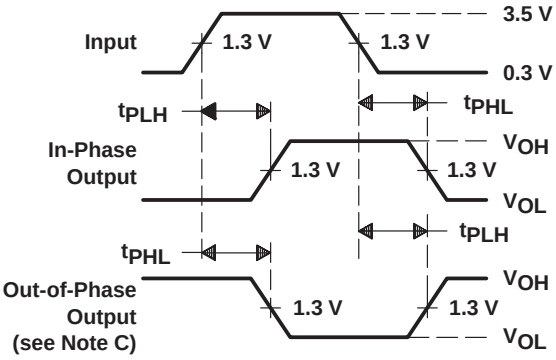
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS561AN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS561AN
SN74ALS561AN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS561AN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

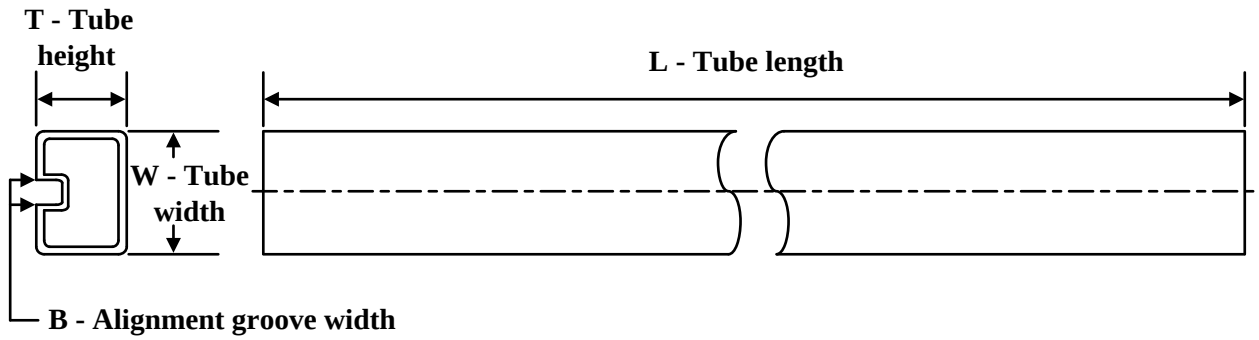
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TUBE



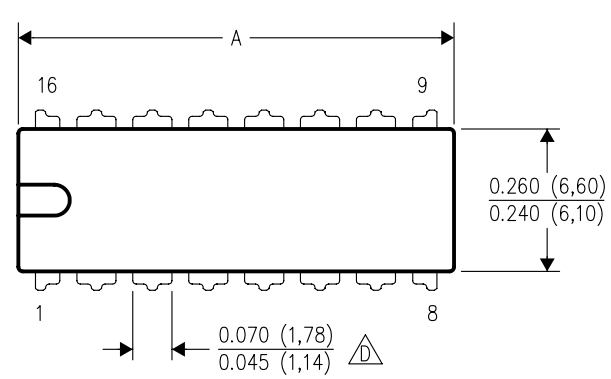
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74ALS561AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS561AN.A	N	PDIP	20	20	506	13.97	11230	4.32

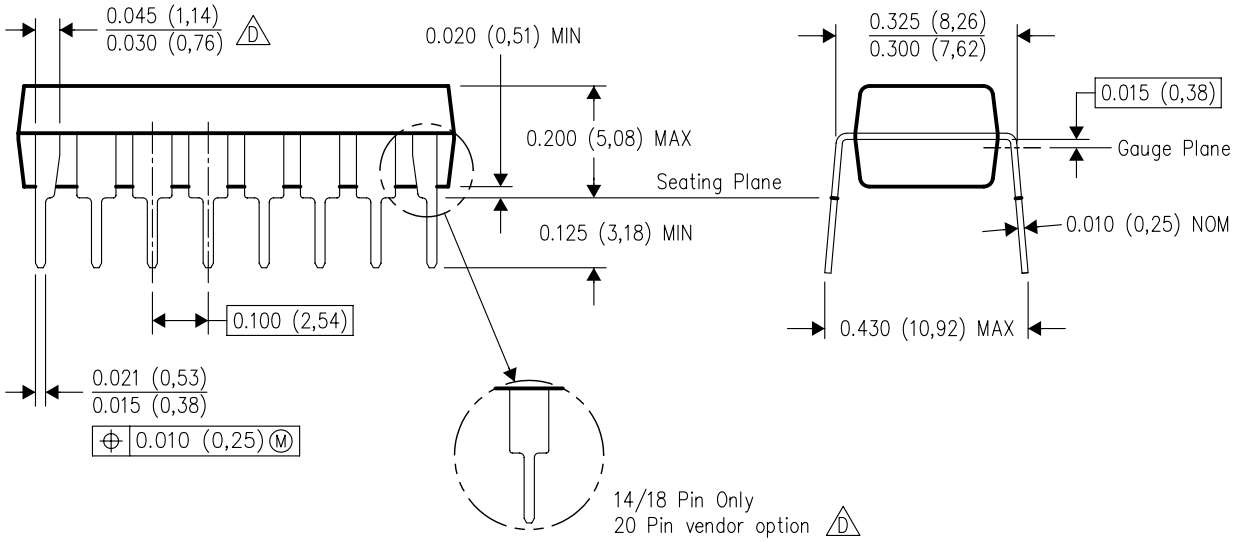
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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