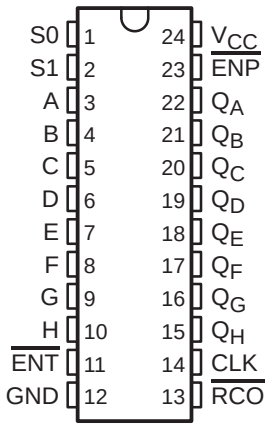
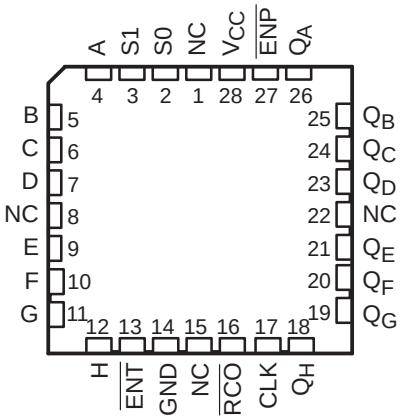
- **Fully Programmable With Synchronous Counting and Loading**
- **SN74ALS867A and ′AS867 Have Asynchronous Clear; SN74ALS869 and ′AS869 Have Synchronous Clear**
- **Fully Independent Clock Circuit Simplifies Use**
- **Ripple-Carry Output for n-Bit Cascading**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

**SN54AS867, SN54AS869 . . . JT PACKAGE**
**SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869 . . . DW OR NT PACKAGE**
**(TOP VIEW)**




**SN54AS867, SN54AS869 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These synchronous, presettable, 8-bit up/down counters feature internal-carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable ($\overline{ENP}$, $\overline{ENT}$) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; they may be preset to any number between 0 and 255. The load-input circuitry allows parallel loading of the cascaded counters. Because loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Two count-enable ($\overline{ENP}$ and $\overline{ENT}$) inputs and a ripple-carry ($\overline{RCO}$) output are instrumental in accomplishing this function. Both $\overline{ENP}$ and $\overline{ENT}$ must be low to count. The direction of the count is determined by the levels of the select (S0, S1) inputs as shown in the function table. $\overline{ENT}$ is fed forward to enable $\overline{RCO}$. $\overline{RCO}$ thus enabled produces a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{ENP}$ and $\overline{ENT}$ are allowed regardless of the level of CLK. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the SN74ALS867A and ′AS867, changes at S0 and S1 that modify the operating mode have no effect on the Q outputs until clocking occurs. For the ′AS867 and ′AS869, any time $\overline{ENP}$ and/or $\overline{ENT}$ is taken high, $\overline{RCO}$ either goes or remains high. For the SN74ALS867A and SN74ALS869, any time $\overline{ENT}$ is taken high, $\overline{RCO}$ either goes or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description (continued)

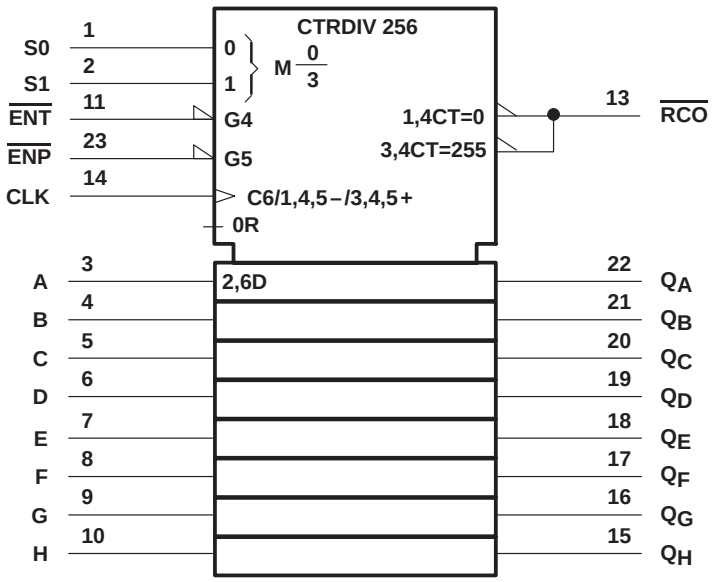
The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS867A, SN74ALS869, SN74AS867, and SN74AS869 are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

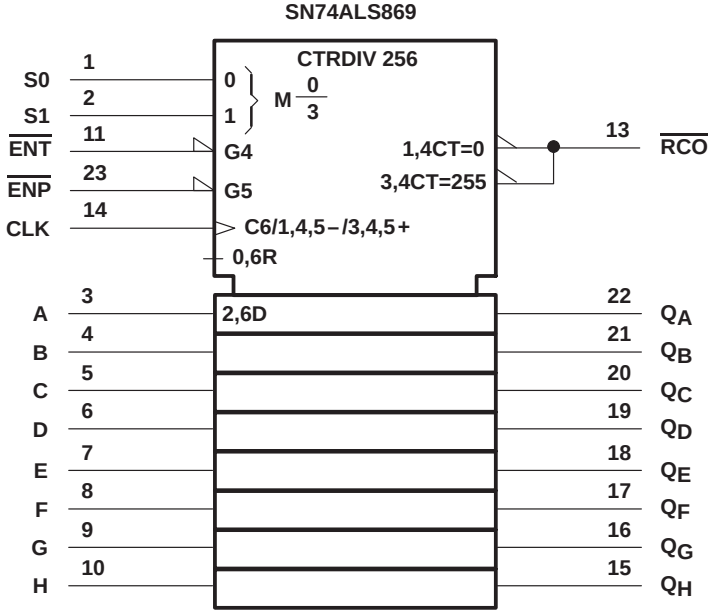
| S1 | S0 | FUNCTION |
|---|---|---|
| L | L | Clear |
| L | H | Count down |
| H | L | Load |
| H | H | Count up |

## logic symbols†

SN74ALS867A

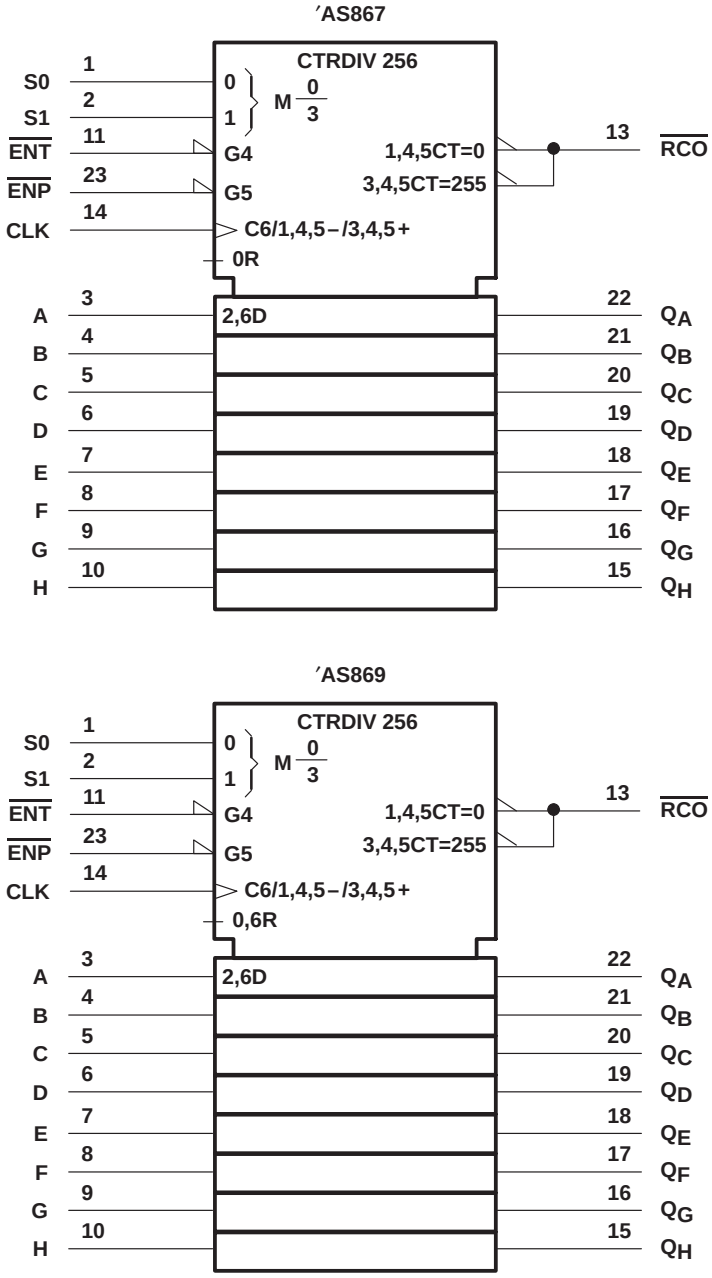



SN74ALS869




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

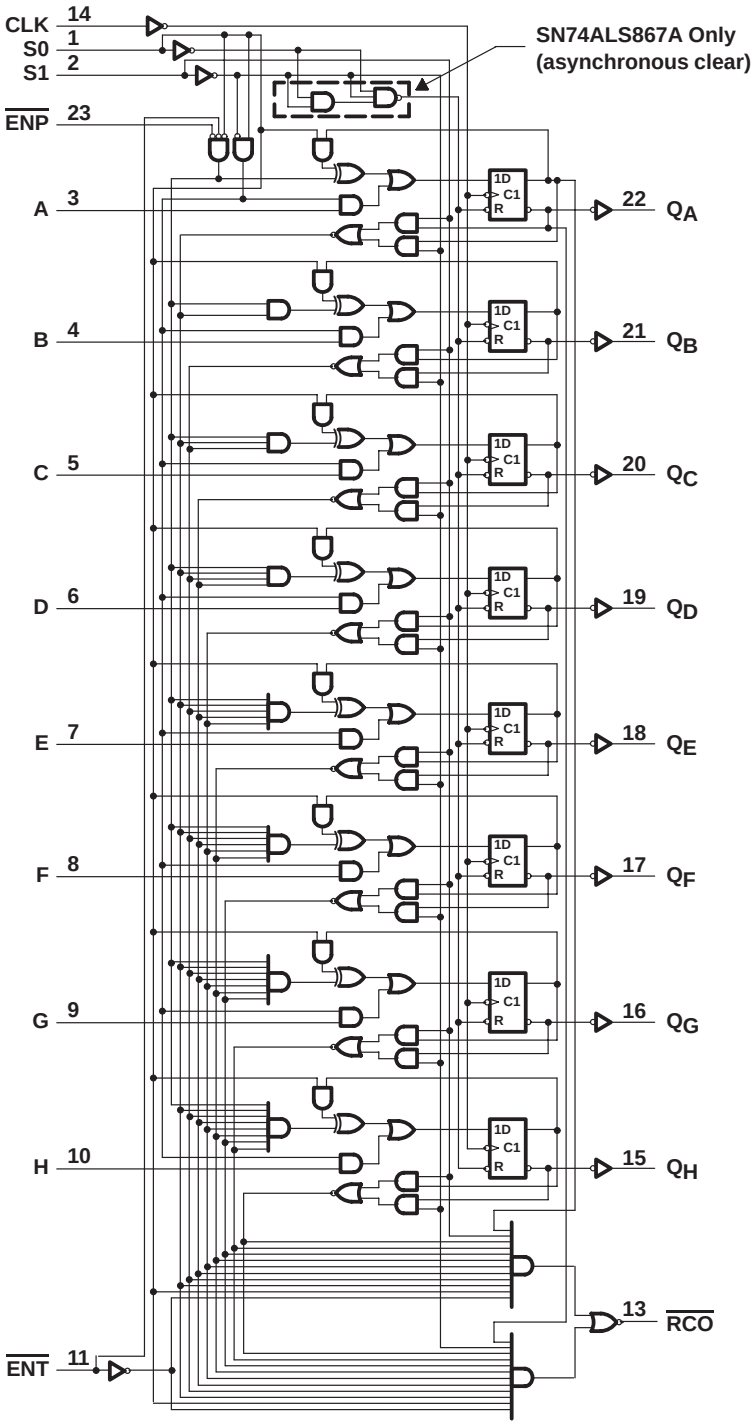
## logic symbols (continued)†




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

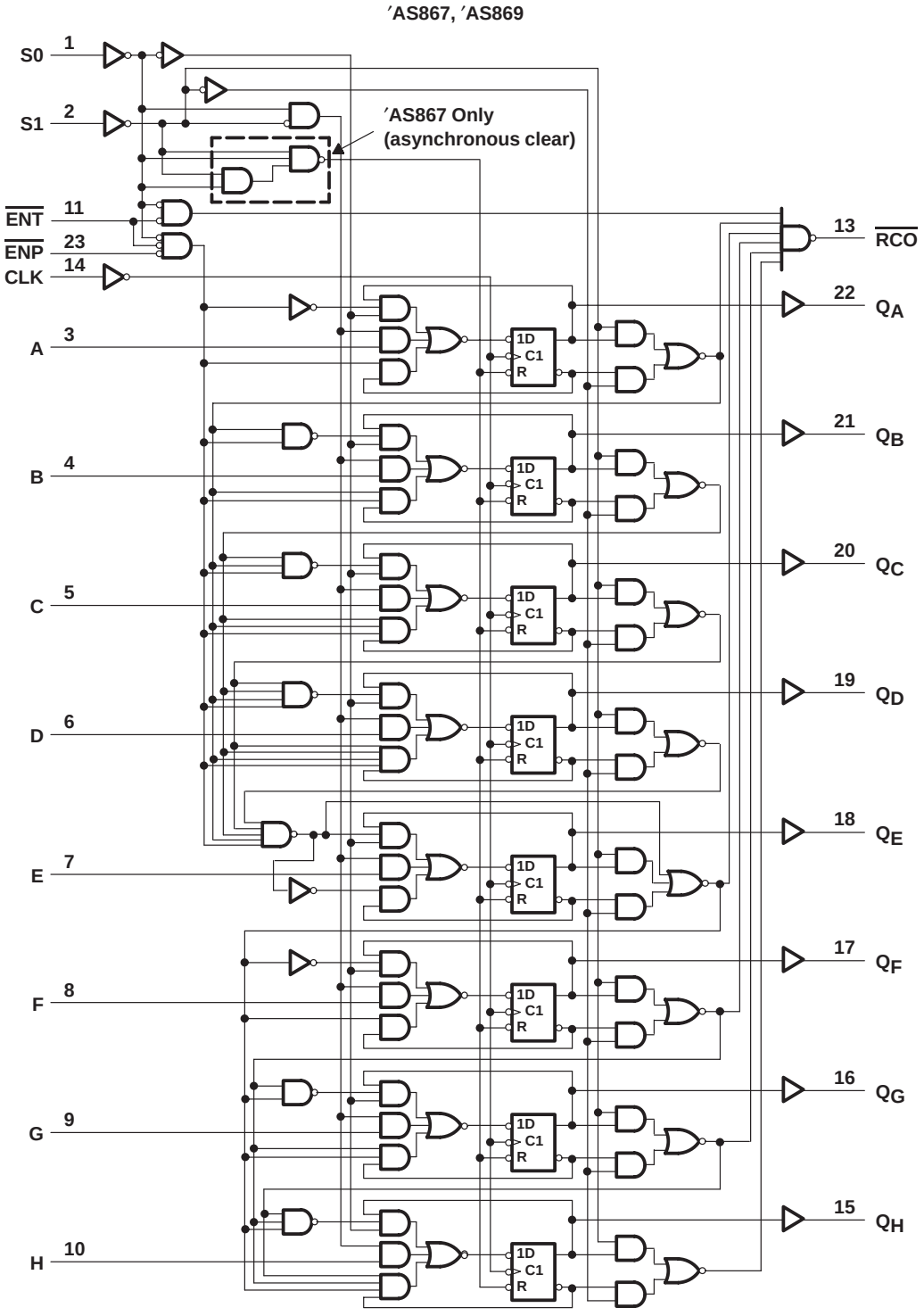
## logic diagram (positive logic)

**SN74ALS867A, SN74ALS869**




Pin numbers shown are for the DW, JT, and NT packages.

## logic diagram (positive logic)

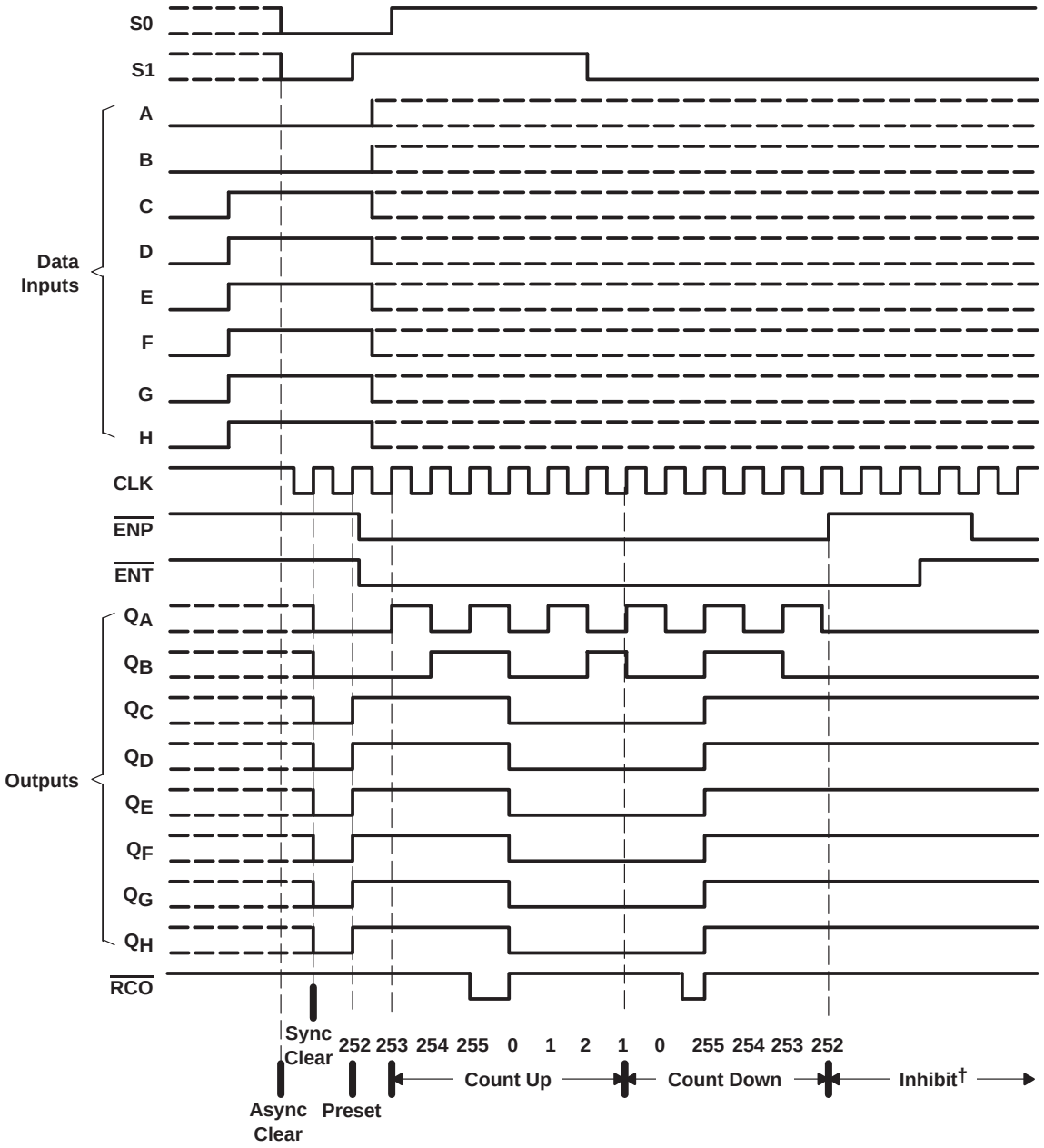



Pin numbers shown are for the DW, JT, and NT packages.

## typical clear, preset, count, and inhibit sequences

The following sequence is illustrated below:

1. Clear outputs to zero (SN74ALS867A and ′AS867 are asynchronous; SN74ALS869 and ′AS869 are synchronous.)
2. Preset to binary 252
3. Count up to 253, 254, 255, 0, 1, and 2
4. Count down to 1, 0, 255, 254, 253, and 252
5. Inhibit




† $\overline{\text{ENT}}$ and $\overline{\text{ENP}}$ both must be low for counting to occur.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN74ALS867A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN74ALS867A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 35 | MHz |
| $t_{w(clock)}$ | Pulse duration, CLK high or low | | 14 | | | ns |
| $t_{w(clear)}$ | Pulse duration of clear pulse, S0 and S1 low | | 10 | | | ns |
| $t_{su}$ | Setup time before CLK↑ | Data inputs A–H | 10 | | | ns |
| | | $\overline{ENP}$ or $\overline{ENT}$ | 15 | | | |
| | | S0 low and S1 high (load) | 12 | | | |
| | | S0 high and S1 low (count down) | 12 | | | |
| | | S0 and S1 high (count up) | 12 | | | |
| $t_h$ | Hold time after CLK↑ | S0 high after S1↑ or S1 high after S0↑ | 3 | | | ns |
| | | Data inputs A–H | 0 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN74ALS867A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.2 | mA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | | | 28 | 45 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | SN74ALS867A | | |
| | | | MIN | MAX | |
| $f_{max}$ | | | 35 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 4 | 14 | ns |
| $t_{PHL}$ | | | 4 | 14 | |
| $t_{PLH}$ | CLK | Any Q | 3 | 16 | ns |
| $t_{PHL}$ | | | 3 | 16 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 3 | 14 | ns |
| $t_{PHL}$ | | | 2 | 9 | |
| $t_{PHL}$ | S0 or S1 (clear mode) | Any Q | 8 | 26 | ns |
| $t_{PLH}$ | S0 or S1 (count up/down) | $\overline{RCO}$ | 4 | 16 | ns |
| $t_{PHL}$ | | | 4 | 16 | |
| $t_{PLH}$ | S0 or S1 (clear mode) | $\overline{RCO}$ | 4 | 16 | ns |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN74ALS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN74ALS869 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 35 | MHz |
| $t_{w(clock)}$ | Pulse duration, CLK high or low | | 14 | | | ns |
| $t_{su}$ | Setup time before CLK↑ | Data inputs A–H | 10 | | | ns |
| | | $\overline{ENP}$ or $\overline{ENT}$ | 15 | | | |
| | | S0 and S1 low (clear) | 13 | | | |
| | | S0 low and S1 high (load) | 13 | | | |
| | | S0 high and S1 low (count down) | 13 | | | |
| | | S0 and S1 high (count up) | 13 | | | |
| $t_h$ | Hold time after CLK↑ | S0 high after S1↑ or S1 high after S0↑ | 3 | | | ns |
| | | Data inputs A–H | 0 | | | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN74ALS869 | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | |
| $V_{IK}$ | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$ –2 | | | V |
| $V_{OL}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | V |
| | | $I_{OL}$ = 8 mA | | 0.35 | 0.5 | |
| $I_I$ | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | mA |
| $I_{IH}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.2 | mA |
| $I_O$§ | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | mA |
| $I_{CC}$ | $V_{CC}$ = 5.5 V | | | 28 | 45 | mA |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | UNIT |
|---|---|---|---|---|---|
| | | | SN74ALS869 | | |
| | | | MIN | MAX | |
| $f_{max}$ | | | 35 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 4 | 14 | ns |
| $t_{PHL}$ | | | 4 | 14 | |
| $t_{PLH}$ | CLK | Any Q | 3 | 16 | ns |
| $t_{PHL}$ | | | 3 | 16 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 3 | 14 | ns |
| $t_{PHL}$ | | | 2 | 9 | |
| $t_{PLH}$ | S1 (count up/down) | $\overline{RCO}$ | 4 | 15 | ns |
| $t_{PHL}$ | | | 4 | 15 | |
| $t_{PLH}$ | S0 (clear/load) | $\overline{RCO}$ | 4 | 16 | ns |
| $t_{PHL}$ | | | 4 | 12 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54AS867 . . . . . –55°C to 125°C
SN74AS867 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN54AS867 | | | SN74AS867 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –2 | | | –2 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | | | 20 | mA |
| $f_{clock}$* | Clock frequency | | 0 | | 40 | 0 | | 50 | MHz |
| $t_{w(clock)}$* | Pulse duration, CLK high or low | | 12.5 | | | 10 | | | ns |
| $t_{w(clear)}$* | Pulse duration of clear pulse, S0 and S1 low | | 12.5 | | | 10 | | | ns |
| $t_{su}$* | Setup time before CLK↑ | Data inputs A–H | 5 | | | 4 | | | ns |
| | | $\overline{ENP}$ or $\overline{ENT}$ | 9 | | | 8 | | | |
| | | S0 low and S1 high (load) | 11 | | | 10 | | | |
| | | S0 and S1 low (clear) | 11 | | | 10 | | | |
| | | S0 high and S1 low (count down) | 42 | | | 40 | | | |
| | | S0 and S1 high (count up) | 42 | | | 40 | | | |
| $t_h$* | Hold time after CLK↑ | Data inputs A–H | 0 | | | 0 | | | ns |
| $t_{skew}$* | Skew time between S0 and S1 (maximum to avoid inadvertent clear) | | | | 8 | | | 7 | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS867 | | | SN74AS867 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –2 mA | $V_{CC}$ –2 | | | $V_{CC}$ –2 | | | V |
| $V_{OL}$ | $\overline{RCO}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA, $V_{IL}$ on $\overline{ENT}$ = 0.7 V | | 0.34 | 0.5 | | | | V |
| | Other outputs | | $I_{OL}$ = 20 mA | | | | | 0.34 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 40 | | | 40 | µA |
| | Other inputs | | | | | 20 | | | 20 | |
| $I_{IL}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –4 | | | –4 | mA |
| | Other inputs | | | | | –2 | | | –2 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 134 | 195 | | 134 | 195 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS867 | | SN74AS867 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$* | | | 40 | | 50 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 5 | 31 | 5 | 22 | ns |
| $t_{PHL}$ | | | 6 | 19 | 6 | 16 | |
| $t_{PLH}$ | CLK | Any Q | 3 | 12 | 3 | 11 | ns |
| $t_{PHL}$ | | | 4 | 16 | 4 | 15 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 3 | 19 | 3 | 10 | ns |
| $t_{PHL}$ | | | 5 | 21 | 5 | 17 | |
| $t_{PLH}$ | $\overline{ENP}$ | $\overline{RCO}$ | 5 | 16 | 5 | 14 | ns |
| $t_{PHL}$ | | | 5 | 21 | 5 | 17 | |
| $t_{PHL}$ | Clear (S0 or S1 low) | Any Q | 7 | 23 | 7 | 21 | ns |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Operating free-air temperature range, $T_A$: SN54AS869 . . . . . –55°C to 125°C
SN74AS869 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions

| | | | SN54AS869 | | | SN74AS869 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | –2 | | | –2 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | | | 20 | mA |
| $f_{clock}$* | Clock frequency | | | | 40 | | | 45 | MHz |
| $t_{w(clock)}$* | Pulse duration, CLK high or low | | 12.5 | | | 11 | | | ns |
| $t_{su}$* | Setup time before CLK↑ | Data inputs A–H | 6 | | | 5 | | | ns |
| | | $\overline{ENP}$ or $\overline{ENT}$ | 10 | | | 9 | | | |
| | | S0 low and S1 high (load) | 13 | | | 11 | | | |
| | | S0 and S1 low (clear) | 13 | | | 11 | | | |
| | | S0 high and S1 low (count down) | 52 | | | 50 | | | |
| | | S0 and S1 high (count up) | 52 | | | 50 | | | |
| $t_h$* | Hold time after CLK↑ | Data inputs A–H | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS869 | | | SN74AS869 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –2 mA | | | | $V_{CC}$ –2 | | | V |
| | | $V_{CC}$ = 4.5 V, | $I_{OH}$ = –2 mA | $V_{CC}$ –2* | | | | | | |
| $V_{OL}$ | $\overline{RCO}$ | $V_{CC}$ = 4.5 V | $I_{OL}$ = 20 mA, $V_{IL}$ on $\overline{ENT}$ = 0.7 V | | 0.34 | 0.5 | | | | V |
| | Other outputs | | $I_{OL}$ = 20 mA | | | | | 0.34 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 40 | | | 40 | µA |
| | Other inputs | | | | | 20 | | | 20 | |
| $I_{IL}$ | $\overline{ENT}$ | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –4 | | | –4 | mA |
| | Other inputs | | | | | –2 | | | –2 | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | | $V_{CC}$ = 5.5 V | | | 134 | 195 | | 134 | 195 | mA |

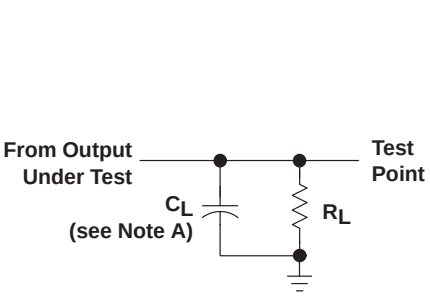
† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, $I_{OS}$.

## switching characteristics (see Figure 1)

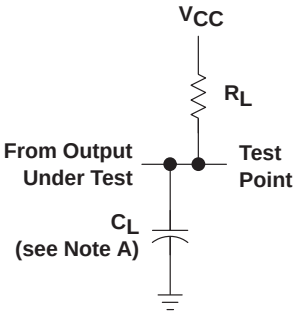
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS869 | | SN74AS869 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$* | | | 40 | | 45 | | MHz |
| $t_{PLH}$ | CLK | $\overline{RCO}$ | 6 | 35 | 6 | 35 | ns |
| $t_{PHL}$ | | | 6 | 20 | 6 | 18 | |
| $t_{PLH}$ | CLK | Any Q | 3 | 12 | 3 | 11 | ns |
| $t_{PHL}$ | | | 4 | 16 | 4 | 15 | |
| $t_{PLH}$ | $\overline{ENT}$ | $\overline{RCO}$ | 3 | 25 | 3 | 15 | ns |
| $t_{PHL}$ | | | 6 | 21 | 6 | 17 | |
| $t_{PLH}$ | $\overline{ENP}$ | $\overline{RCO}$ | 5 | 27 | 5 | 19 | ns |
| $t_{PHL}$ | | | 6 | 21 | 6 | 18 | |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

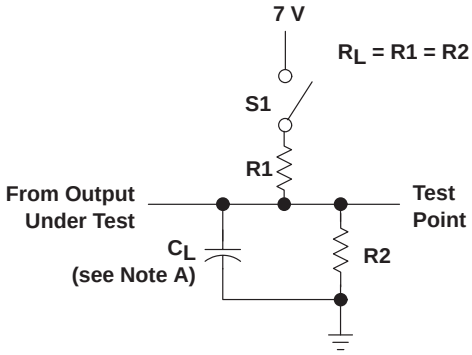
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



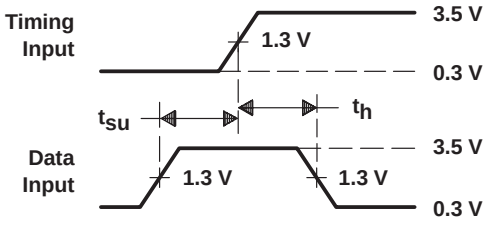

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



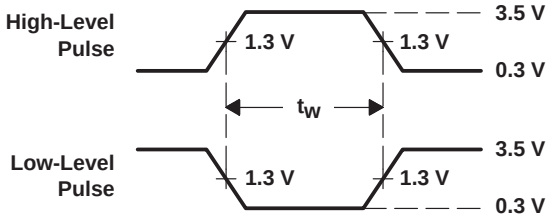

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



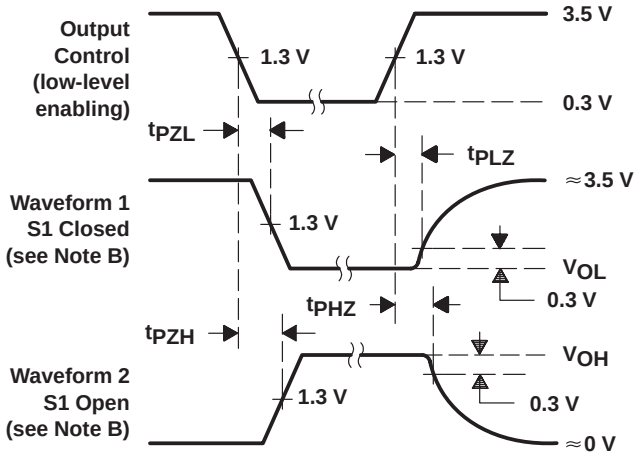

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



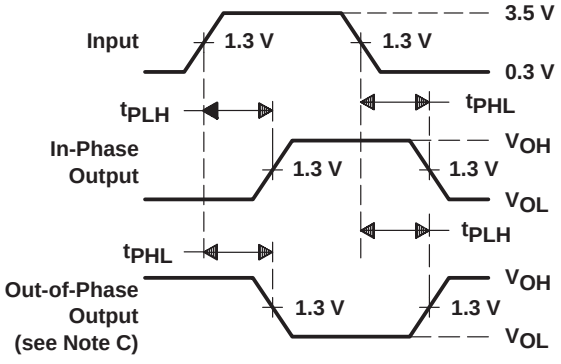

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8966801LA | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8966801LA SNJ54AS867JT |
| SN54AS867JT | Last Time Buy | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54AS867JT |
| SN54AS867JT.A | Last Time Buy | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54AS867JT |
| SN54AS869JT | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54AS869JT |
| SN54AS869JT.A | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54AS869JT |
| SN74ALS867ADW | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS867A |
| SN74ALS867ADW.A | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS867A |
| SN74ALS869DW | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS869 |
| SN74ALS869DW.A | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS869 |
| SN74ALS869DWE4 | Active | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS869 |
| SN74AS869DW | Last Time Buy | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS869 |
| SN74AS869DW.A | Last Time Buy | Production | SOIC (DW) \| 24 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS869 |
| SNJ54AS867JT | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8966801LA SNJ54AS867JT |
| SNJ54AS867JT.A | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8966801LA SNJ54AS867JT |
| SNJ54AS869JT | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8952601LA SNJ54AS869JT |
| SNJ54AS869JT.A | Active | Production | CDIP (JT) \| 24 | 15 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8952601LA SNJ54AS869JT |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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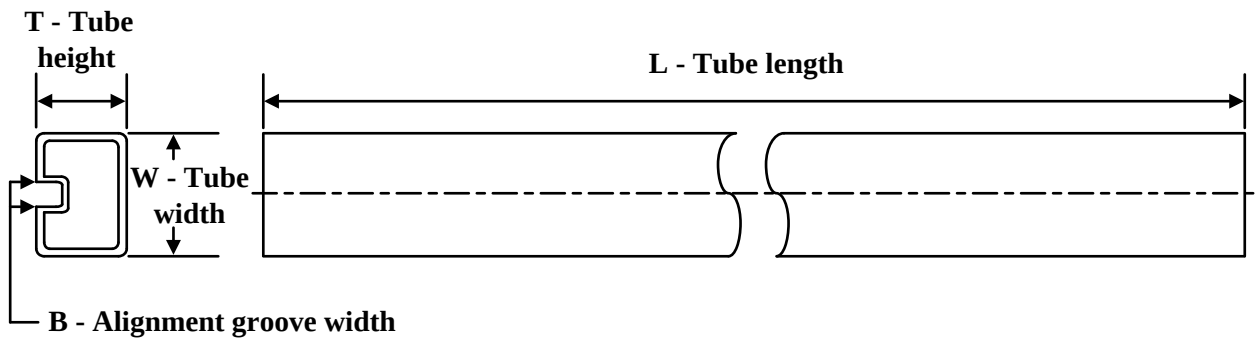
**OTHER QUALIFIED VERSIONS OF SN54AS869, SN74AS869 :**

- Catalog : SN74AS869
- Military : SN54AS869

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TUBE



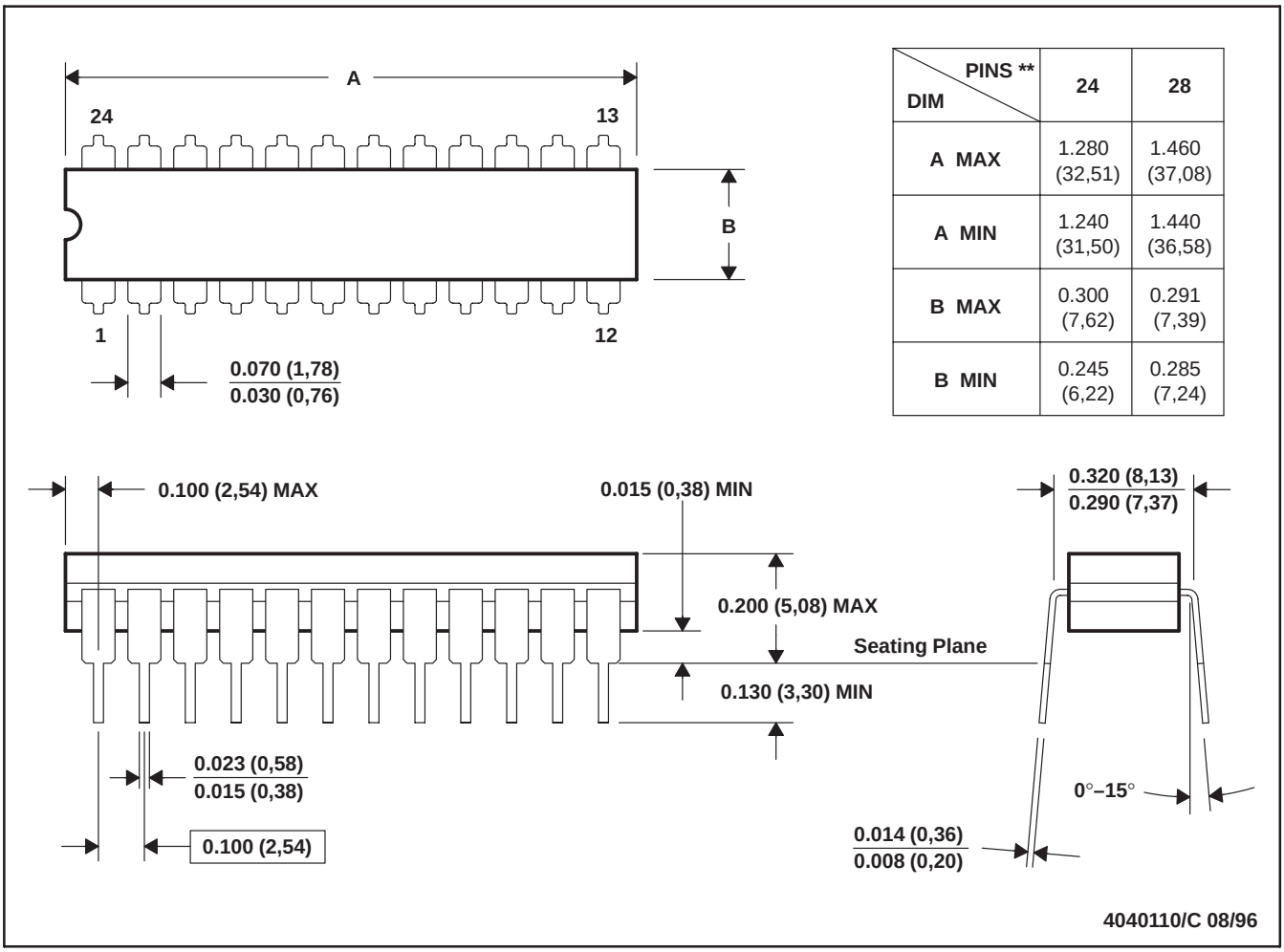

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ALS867ADW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74ALS867ADW.A | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74ALS869DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74ALS869DW.A | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74ALS869DWE4 | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74AS869DW | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN74AS869DW.A | DW | SOIC | 24 | 25 | 506.98 | 12.7 | 4826 | 6.6 |

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

**JT (R-GDIP-T**)** **CERAMIC DUAL-IN-LINE**

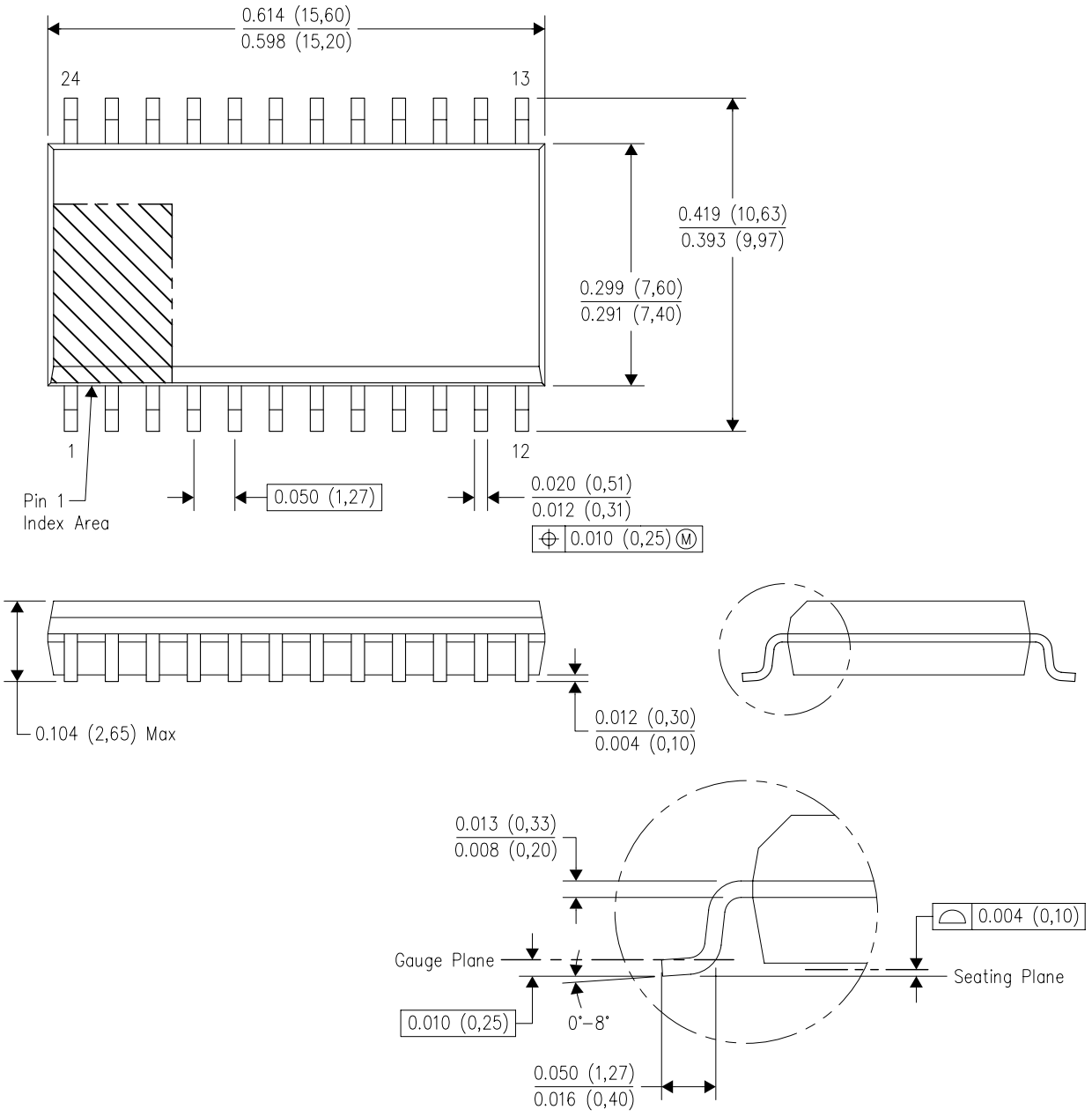
**24 LEADS SHOWN**




| DIM \ PINS ** | 24 | 28 |
|---|---|---|
| A MAX | 1.280 (32,51) | 1.460 (37,08) |
| A MIN | 1.240 (31,50) | 1.440 (36,58) |
| B MAX | 0.300 (7,62) | 0.291 (7,39) |
| B MIN | 0.245 (6,22) | 0.285 (7,24) |

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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