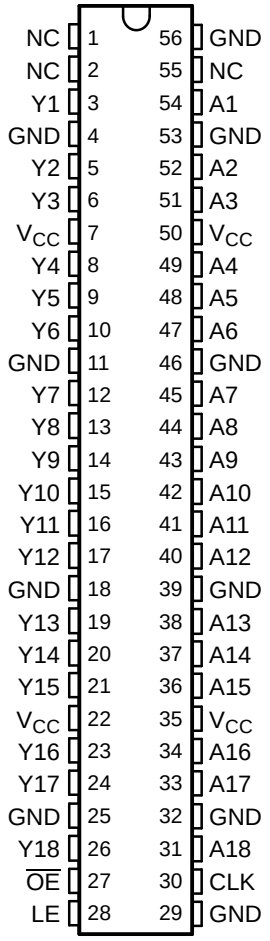
SN74ALVC162835
18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCES126H – FEBRUARY 1998 – REVISED SEPTEMBER 2004

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Max t_{pd} of 2 ns at 3.3 V**
- **±12-mA Output Drive at 3.3 V**
- **Ideal for Use in PC100 Register DIMM, Revision 1.1**
- **Output Port Has Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)



NC − No internal connection

DESCRIPTION/ORDERING INFORMATION

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V V_{CC} operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The output port includes equivalent 26-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP - DL	Tube	SN74ALVC162835DL	ALVC162835
		Tape and reel	SN74ALVC162835DLR	
	TSSOP - DGG	Tape and reel	SN74ALVC162835DGGR	ALVC162835
	TVSOP - DGV	Tape and reel	SN74ALVC162835DGVR	VC2835

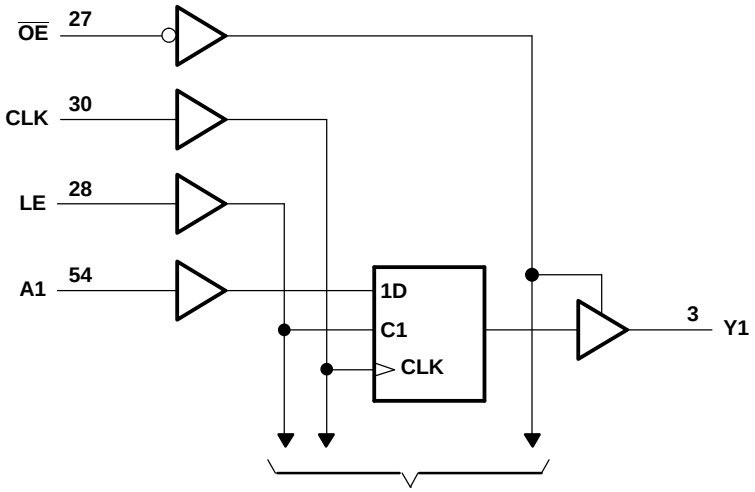
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y_0 (1)

(1) Output level before the indicated steady-state input conditions were established

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range(2)		-0.5	4.6	V
V_O	Output voltage range(2)(3)		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		-50	mA
I_{OK}	Output clamp current	V_O < 0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DGG package		64	°C/W
		DGV package		48	
		DL package		56	
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-2	mA
		V_{CC} = 2.3 V		-6	
		V_{CC} = 2.7 V		-8	
		V_{CC} = 3 V		-12	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		2	mA
		V_{CC} = 2.3 V		6	
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -100 μA		1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -2 mA		1.65 V	1.2			
		I_{OH} = -4 mA		2.3 V	1.9			
		I_{OH} = -6 mA		2.3 V	1.7			
				3 V	2.4			
		I_{OH} = -8 mA		2.7 V	2			
		I_{OH} = -12 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 2 mA		1.65 V			0.45	
		I_{OL} = 4 mA		2.3 V			0.4	
		I_{OL} = 6 mA		2.3 V			0.55	
				3 V			0.55	
		I_{OL} = 8 mA		2.7 V			0.6	
		I_{OL} = 12 mA		3 V			0.8	
I_I		V_I = V_{CC} or GND		3.6 V			±5	μA
I_{OZ}		V_O = V_{CC} or GND		3.6 V			±10	μA
I_{CC}		V_I = V_{CC} or GND,	I_O = 0	3.6 V			40	μA
ΔI_{CC}		One input at V_{CC} - 0.6 V,	Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		3.5		pF
	Data inputs					5		
C_o	Outputs	V_O = V_{CC} or GND		3.3 V		7		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

				V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency				(1)		150		150		150	MHz
t_w	Pulse duration	LE high		(1)		3.3		3.3		3.3		ns
		CLK high or low		(1)		3.3		3.3		3.3		
t_{su}	Setup time	Data before CLK↑		(1)		2.2		2.1		1.7		ns
		Data before LE↓	CLK high	(1)		1.9		1.6		1.5		
			CLK low	(1)		1.3		1.1		1		
t_h	Hold time	Data after CLK↑		(1)		0.6		0.6		0.7		ns
		Data after LE↓	CLK high or low	(1)		1.4		1.7		1.4		

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		150		150		150		MHz
t_{pd}	A	Y		(1)	1	5		5	1	4.2	ns
	LE			(1)	1.3	5.9		5.8	1.3	5.1	
	CLK			(1)	1.4	6.3		6.1	1.4	5.4	
t_{en}	$\overline{OE}$	Y		(1)	1.4	6.3		6.5	1.1	5.5	ns
t_{dis}	$\overline{OE}$	Y		(1)	1	4.9		4.9	1.3	4.5	ns

(1) This information was not available at the time of publication.

SWITCHING CHARACTERISTICS

from 0°C to 85°C, C_L = 0 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}(1)	A	Y	0.9	2	ns
	CLK		1.4	2.9	

(1) Texas Instruments SPICE simulation data

SWITCHING CHARACTERISTICS

from 0°C to 65°C, C_L = 50 pF

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.15 V		UNIT
			MIN	MAX	
t_{pd}	A	Y	1	4	ns
	CLK		1.9	5	

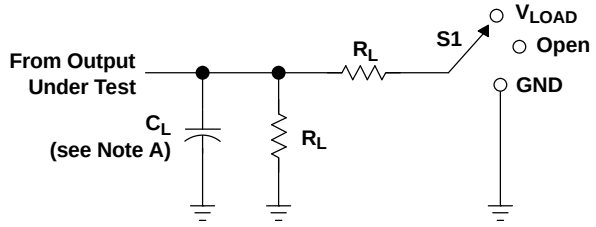
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 0, f = 10 MHz	(1)	35.5	40	pF
		Outputs disabled		(1)	12.5	14	

(1) This information was not available at the time of publication.

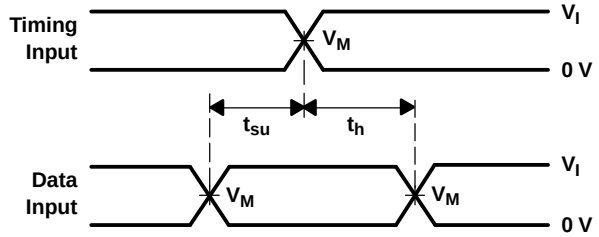
PARAMETER MEASUREMENT INFORMATION



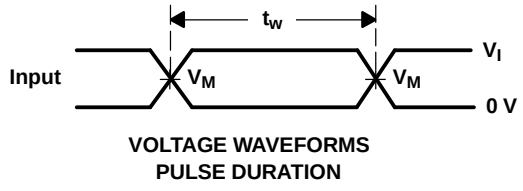
LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

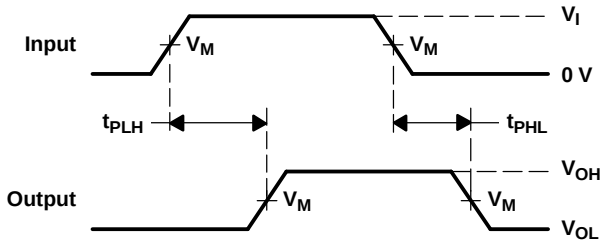
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



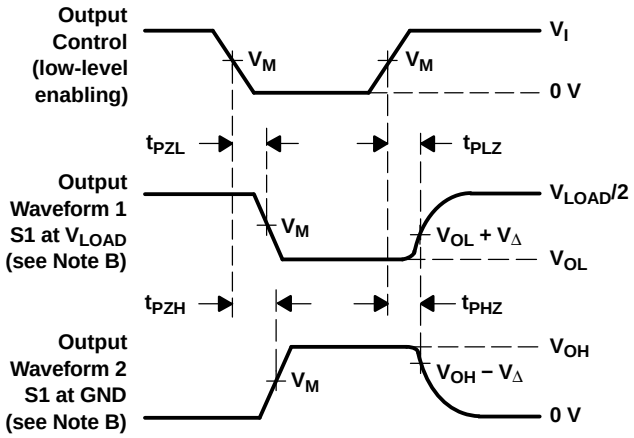
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

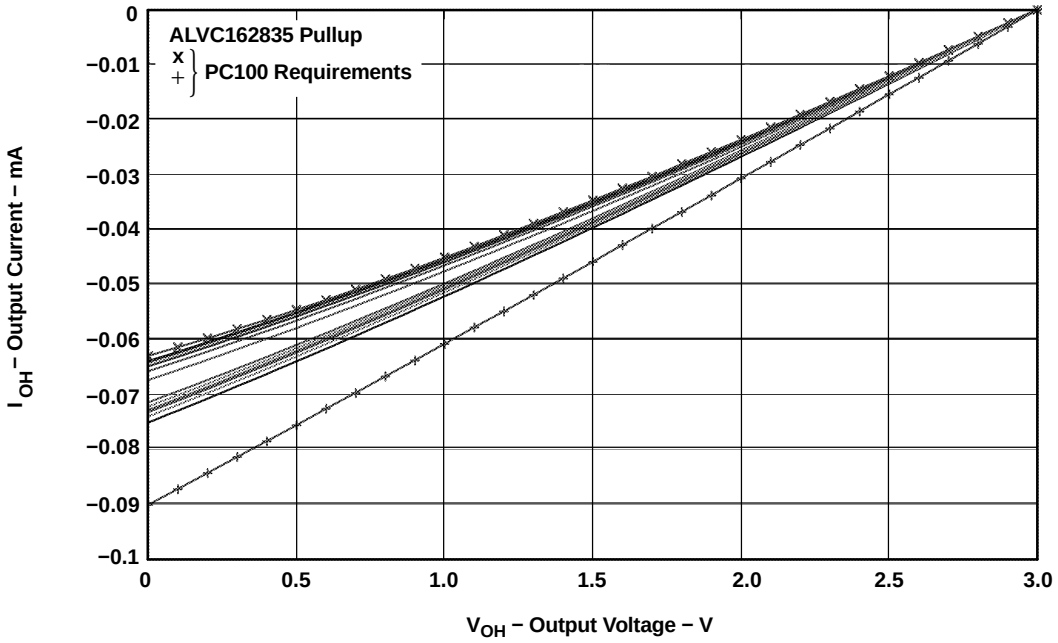


Figure 2. IV Characteristics - Pullup

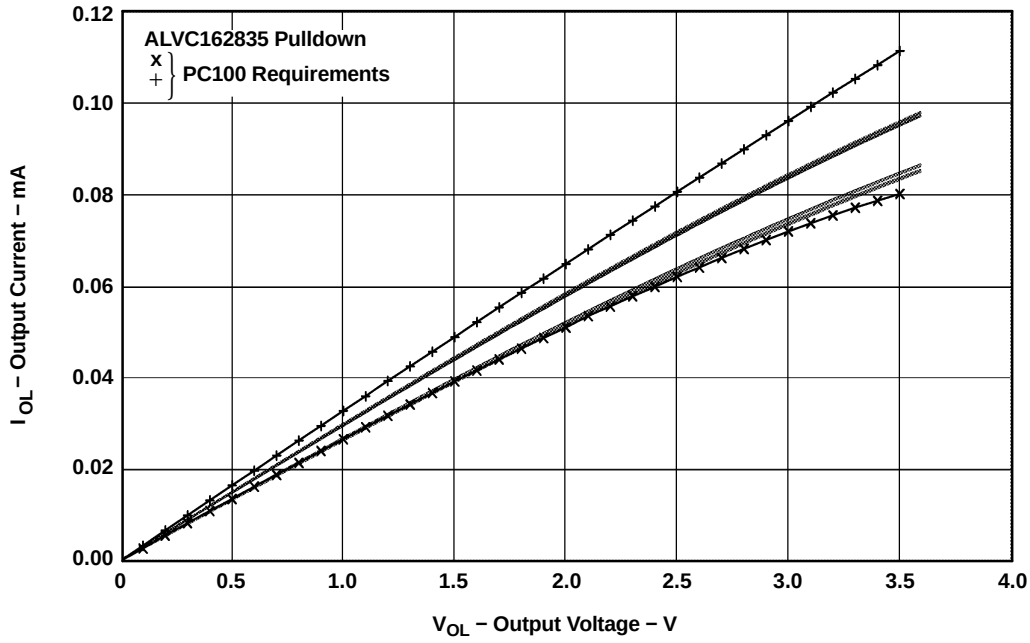


Figure 3. IV Characteristics - Pulldown

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74ALVC162835DGGRG4	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC162835
74ALVC162835DGGRG4.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC162835
SN74ALVC162835DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC162835
SN74ALVC162835DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVC162835

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

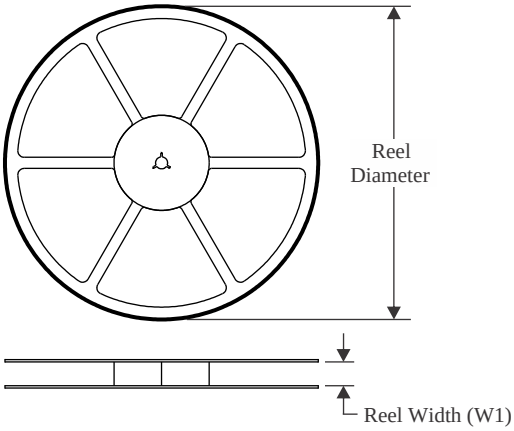
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

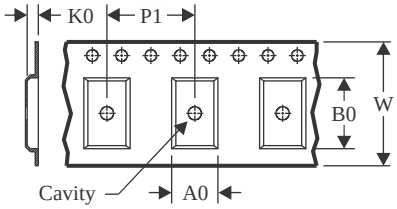
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

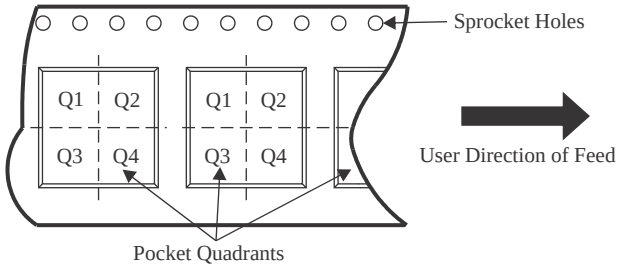


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

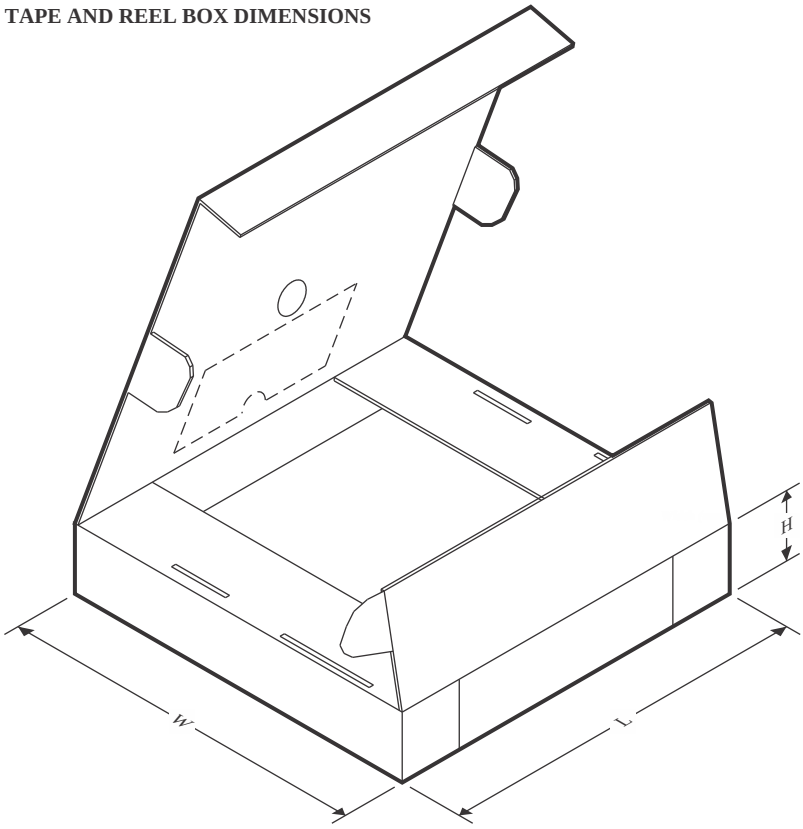
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVC162835DGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74ALVC162835DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

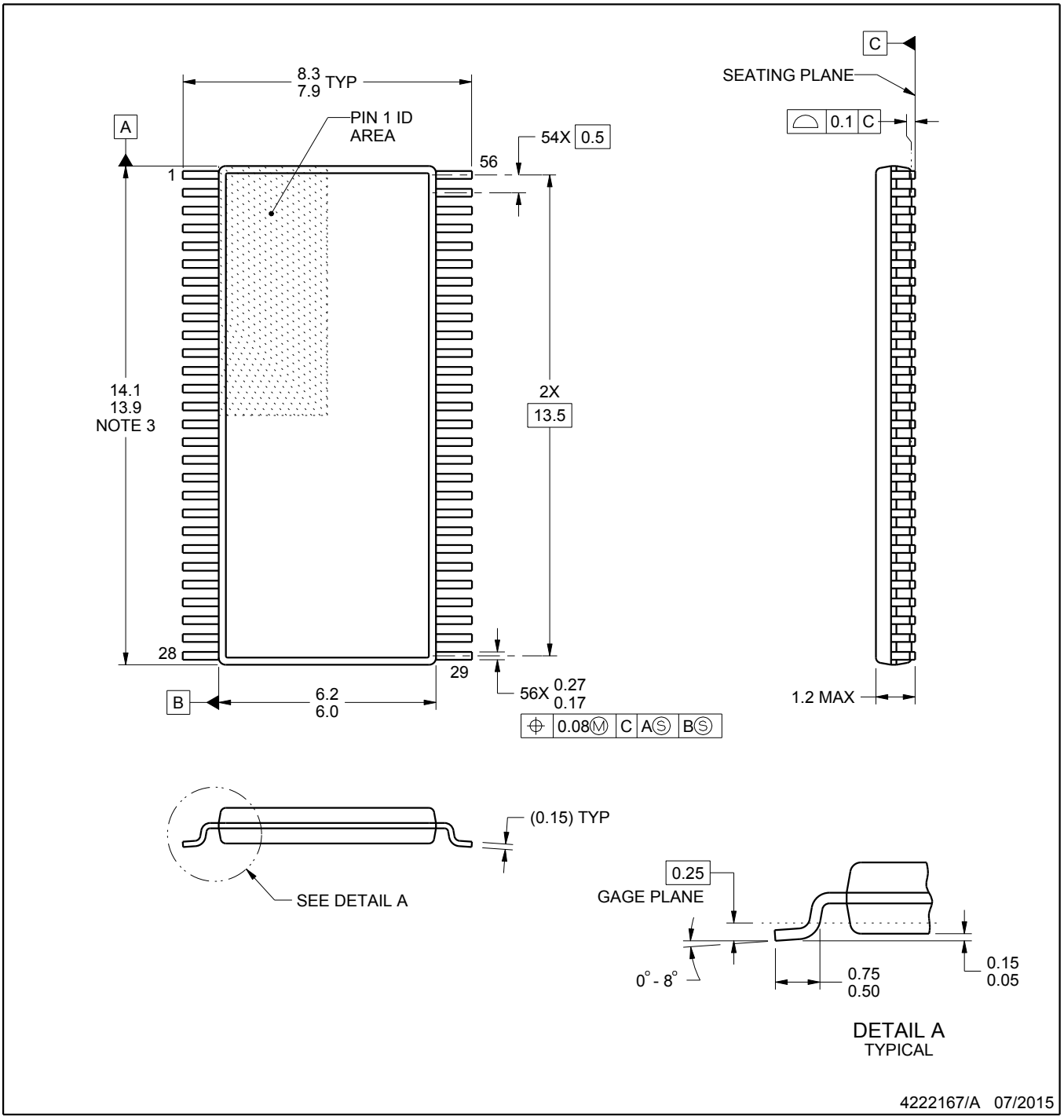
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ALVC162835DGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN74ALVC162835DGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0

PACKAGE OUTLINE

DGG0056A

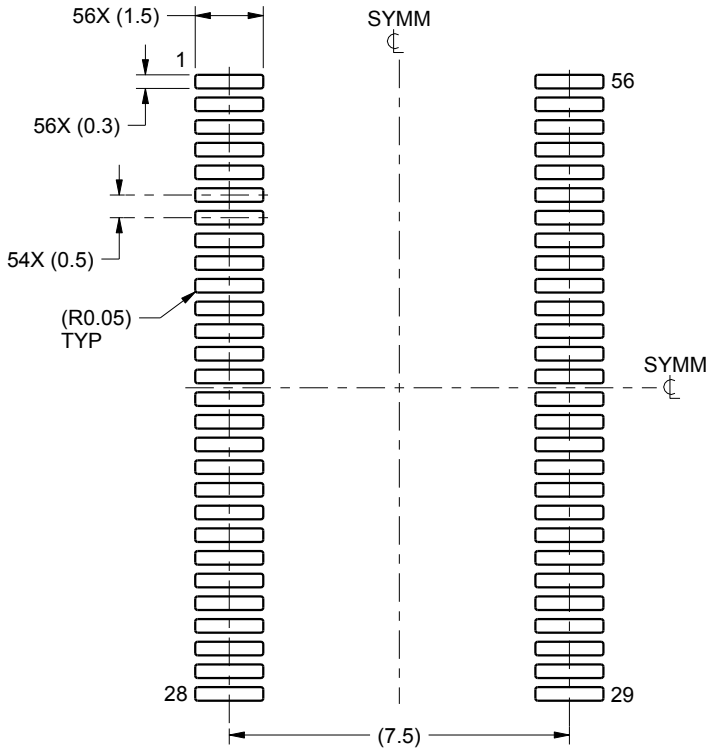
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

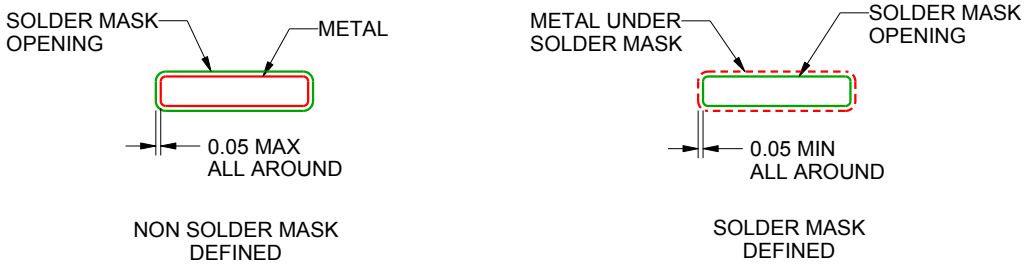


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

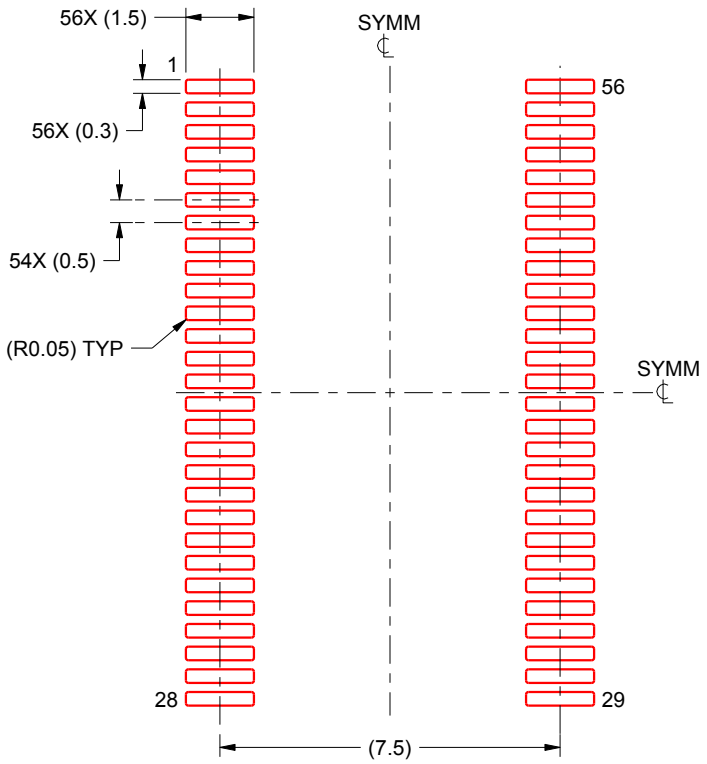


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025