

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

- Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

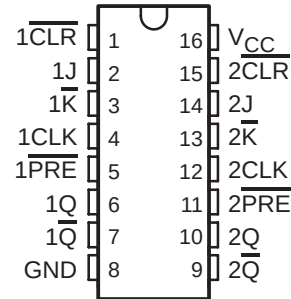
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (MHz)	TYPICAL POWER DISSIPATION PER FLIP-FLOP (mW)
'ALS109A	50	6
'AS109A	129	29

description

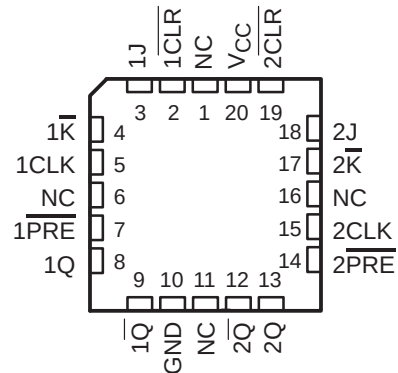
These devices contain two independent J-K positive-edge-triggered flip-flops. A low level at the preset ($\overline{\text{PRE}}$) or clear ($\overline{\text{CLR}}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are inactive (high), data at the J and $\overline{\text{K}}$ inputs meeting the setup-time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and $\overline{\text{K}}$ inputs can be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{\text{K}}$ and tying J high. They also can perform as D-type flip-flops if J and $\overline{\text{K}}$ are tied together.

The SN54ALS109A and SN54AS109A are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS109A and SN74AS109A are characterized for operation from 0°C to 70°C .

SN54ALS109A, SN54AS109A ... J PACKAGE
SN74ALS109A, SN74AS109A ... D OR N PACKAGE
(TOP VIEW)



SN54ALS109A, SN54AS109A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	J	$\overline{\text{K}}$	Q	$\overline{\text{Q}}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	$\text{H}^{\dagger}$	$\text{H}^{\dagger}$
H	H	$\uparrow$	L	L	L	H
H	H	$\uparrow$	H	L	Toggle	
H	H	$\uparrow$	L	H	Q0	$\overline{\text{Q}}0$
H	H	$\uparrow$	H	H	H	L
H	H	L	X	X	Q0	$\overline{\text{Q}}0$

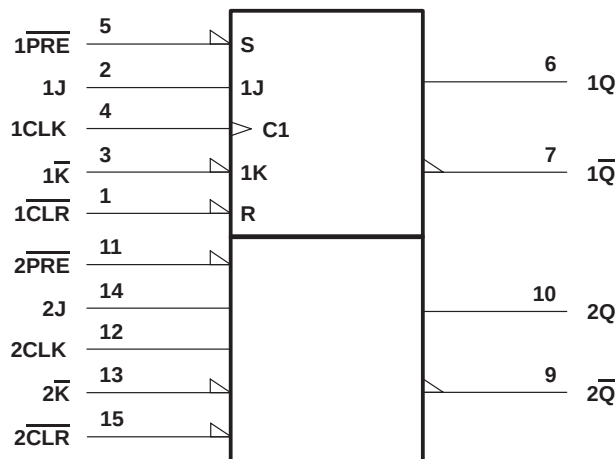
$\dagger$ The output levels in this configuration are not specified to meet the minimum levels for VOH if the lows at $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are near VIL maximum. Furthermore, this configuration is nonstable; that is, it does not persist when either $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ returns to its inactive (high) level.

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54ALS109A	–55°C to 125°C
SN74ALS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS109A			SN74ALS109A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			−0.4			−0.4	mA
I _{OL}	Low-level output current			4			8	mA
f _{clock}	Clock frequency	0		30	0		34	MHz
t _w	Pulse duration	PRE or CLR low		15	15		ns	
		CLK high		16.5	14.5			
		CLK low		16.5	14.5			
t _{su}	Setup time before CLK↑	Data		15	15		ns	
		PRE or CLR inactive		10	10			
t _h	Hold time after CLK↑	Data		0	0		ns	
T _A	Operating free-air temperature	−55		125	0		70	°C

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A		SN74ALS109A		UNIT
				MIN	TYP†	MAX	MIN	
V _{IK}		V _{CC} = 4.5 V, I _I = -18 mA		-1.5		-1.5		V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA		V _{CC} -2		V _{CC} -2		V
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 8 mA			0.35	0.5	
I _I	CLK, J, or $\overline{K}$	V _{CC} = 5.5 V, V _I = 7 V	0.1		0.1		mA	
	$\overline{PRE}$ or $\overline{CLR}$		0.2		0.2			
I _{IH}	CLK, J, or $\overline{K}$	V _{CC} = 5.5 V, V _I = 2.7 V	20		20		μA	
	$\overline{PRE}$ or $\overline{CLR}$		40		40			
I _{IL}	CLK, J, or $\overline{K}$	V _{CC} = 5.5 V, V _I = 0.4 V	-0.2		-0.2		mA	
	$\overline{PRE}$ or $\overline{CLR}$		-0.4		-0.4			
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112	mA	
I _{CC}		V _{CC} = 5.5 V, See Note 1	2.4	4	2.4	4	mA	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f _{max}			30		34		MHz
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$	3	17	3	13	ns
t _{PHL}			5	17	5	15	
t _{PLH}	CLK	Q or $\overline{\text{Q}}$	5	21	5	16	ns
t _{PHI}			5	20	5	18	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS109A	–55°C to 125°C
SN74AS109A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS109A			SN74AS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2			V
V _{IL}	Low-level input voltage		0.8			0.8			V
I _{OH}	High-level output current		−2			−2			mA
I _{OL}	Low-level output current		20			20			mA
f _{clock} *	Clock frequency		0	90		0	105		MHz
t _w *	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t _{su} *	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2			2			
t _h *	Hold time after CLK↑	Data	0			0			ns
T _A	Operating free-air temperature		−55	125		0	70		°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109A			SN74AS109A			UNIT
				MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$				–1.2			–1.2	V
V_{OH}		$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$		$V_{CC}-2$			$V_{CC}-2$			V
V_{OL}		$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$			0.25	0.5		0.25	0.5	V
I_I		$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$				0.1			0.1	mA
I_{IH}	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$				20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J, or $\overline{K}$	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$				–0.5			–0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					–1.8			–1.8	
$I_O^{\S}$		$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$		–30		–112	–30		–112	mA
I_{CC}		$V_{CC} = 5.5\text{ V}$, See Note 1			11.5	17		11.5	17	mA

[‡] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with J, K, CLK, and $\overline{PRE}$ grounded, then with J, K, CLK, and $\overline{CLR}$ grounded.

SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A

DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	VCC = 4.5 V to 5.5 V, CL = 50 pF, RL = 500 Ω, TA = MIN to MAX†				UNIT
			SN54AS109A		SN74AS109A		
			MIN	MAX	MIN	MAX	
fmax*			90		105		MHz
tPLH	PRE or CLR	Q or Q̄	2	9	2	8	ns
tPHL			3.5	11.5	3.5	10.5	
tPLH	CLK	Q or Q̄	2.5	10	2.5	9	ns
tPHL			3.5	10.5	3.5	9	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

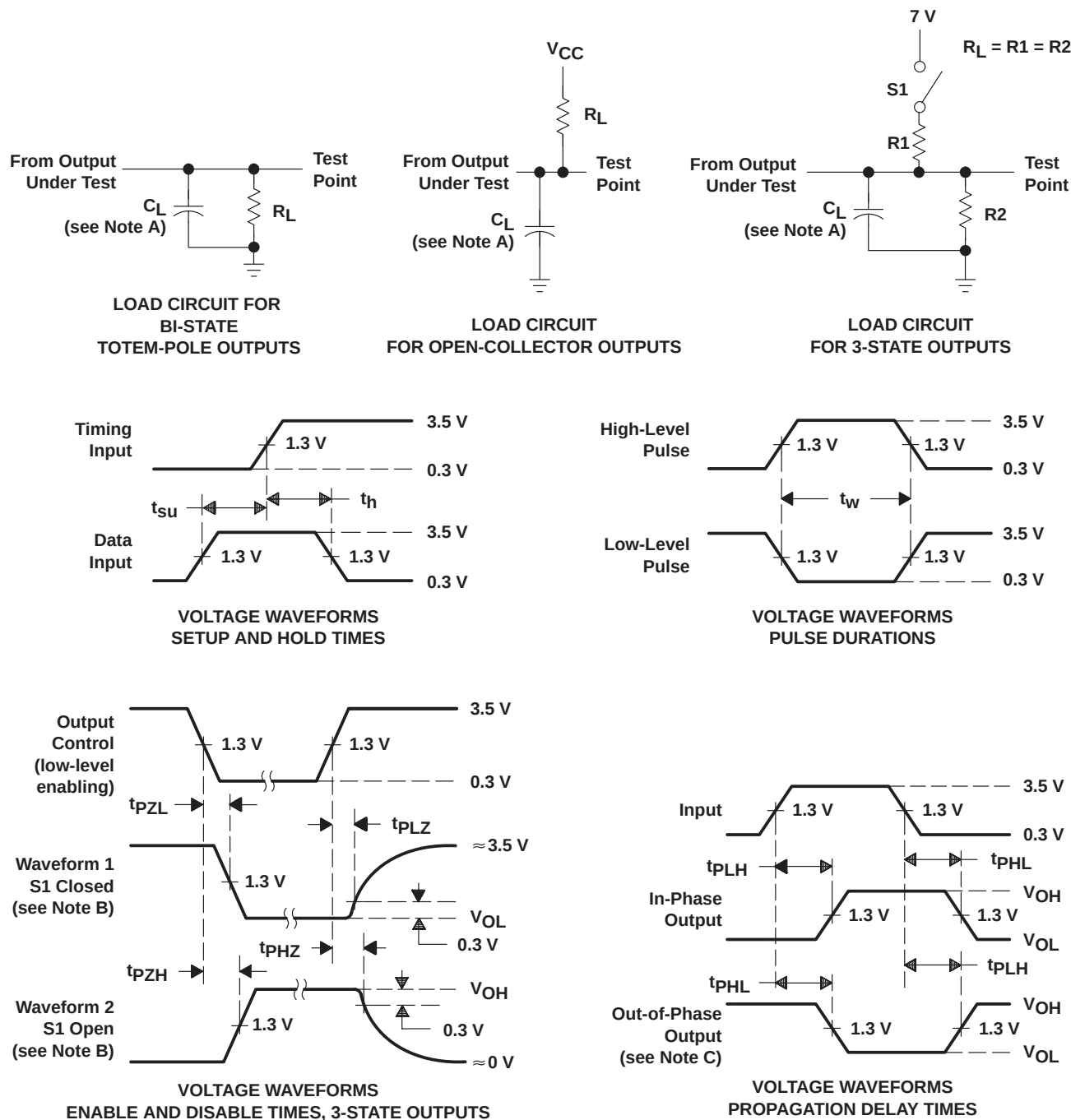
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



SN54ALS109A, SN54AS109A, SN74ALS109A, SN74AS109A DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET

SDAS198B – APRIL 1982 – REVISED AUGUST 1995

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84000012A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84000012A SNJ54ALS 109AFK
8400001EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400001EA SNJ54ALS109AJ
JM38510/37102B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102B2A
JM38510/37102B2A.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102B2A
JM38510/37102BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102BEA
JM38510/37102BEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102BEA
M38510/37102B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102B2A
M38510/37102BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37102BEA
SN54ALS109AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS109AJ
SN54ALS109AJ.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS109AJ
SN74ALS109AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A
SN74ALS109AD.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A
SN74ALS109AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS109AN
SN74ALS109AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS109AN
SN74ALS109ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A
SN74ALS109ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS109A
SN74AS109AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS109A
SN74AS109AD.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS109A
SN74AS109AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS109AN
SN74AS109AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS109AN
SN74AS109ANSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS109A
SN74AS109ANSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS109A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54ALS109AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84000012A SNJ54ALS 109AFK
SNJ54ALS109AFK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84000012A SNJ54ALS 109AFK
SNJ54ALS109AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400001EA SNJ54ALS109AJ
SNJ54ALS109AJ.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400001EA SNJ54ALS109AJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS109A, SN74ALS109A :

- Catalog : [SN74ALS109A](#)
- Military : [SN54ALS109A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

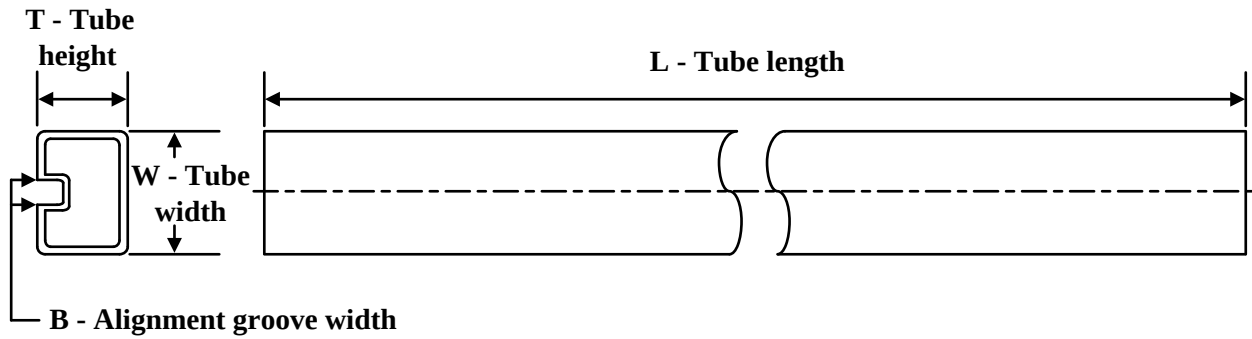
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS109ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AS109ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS109ANSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74AS109ANSR	SOP	NS	16	2000	353.0	353.0	32.0

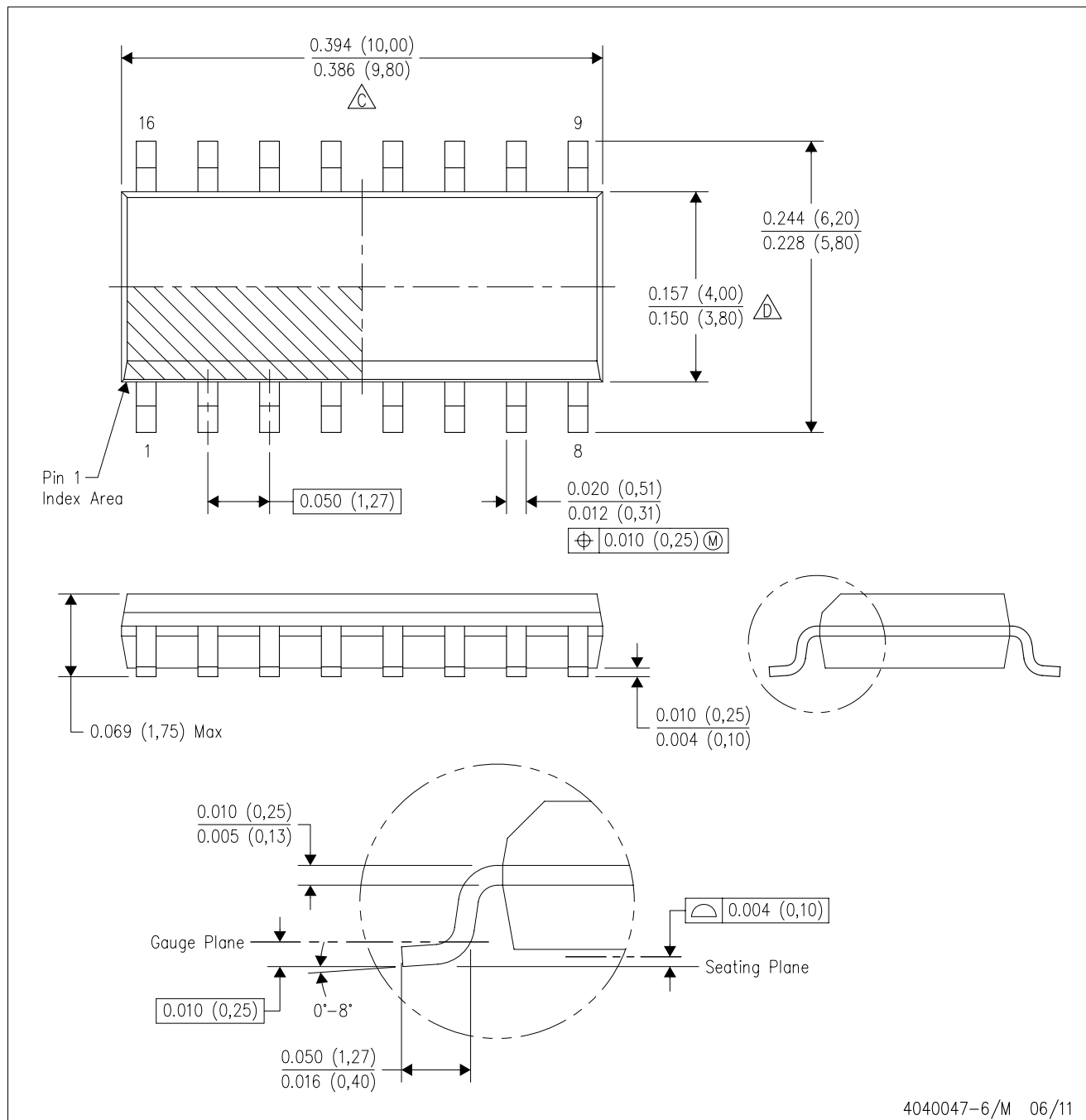
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
84000012A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37102B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37102B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS109AD	D	SOIC	16	40	507	8	3940	4.32
SN74ALS109AD.A	D	SOIC	16	40	507	8	3940	4.32
SN74ALS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS109AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74ALS109AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS109AD	D	SOIC	16	40	507	8	3940	4.32
SN74AS109AD.A	D	SOIC	16	40	507	8	3940	4.32
SN74AS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS109AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS109AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74AS109AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54ALS109AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS109AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

GENERIC PACKAGE VIEW

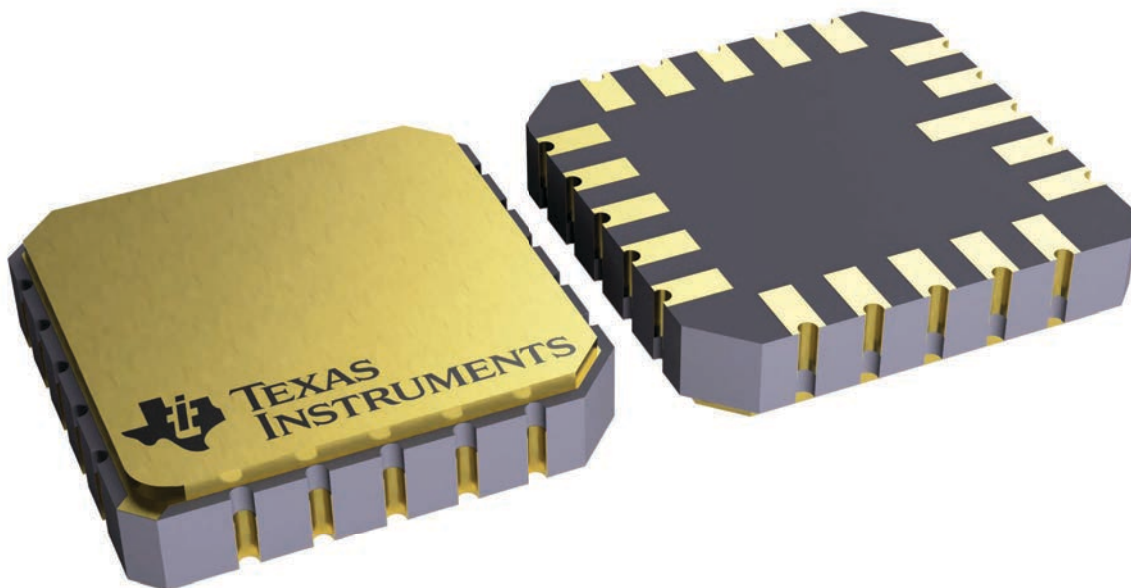
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

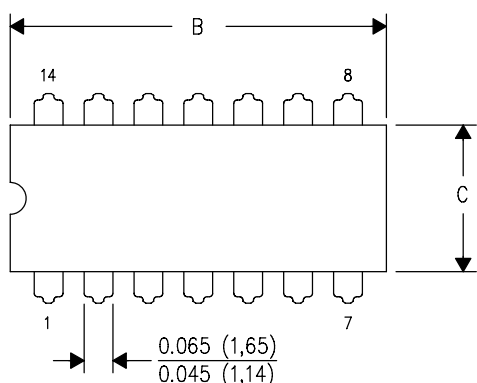


4229370VA\

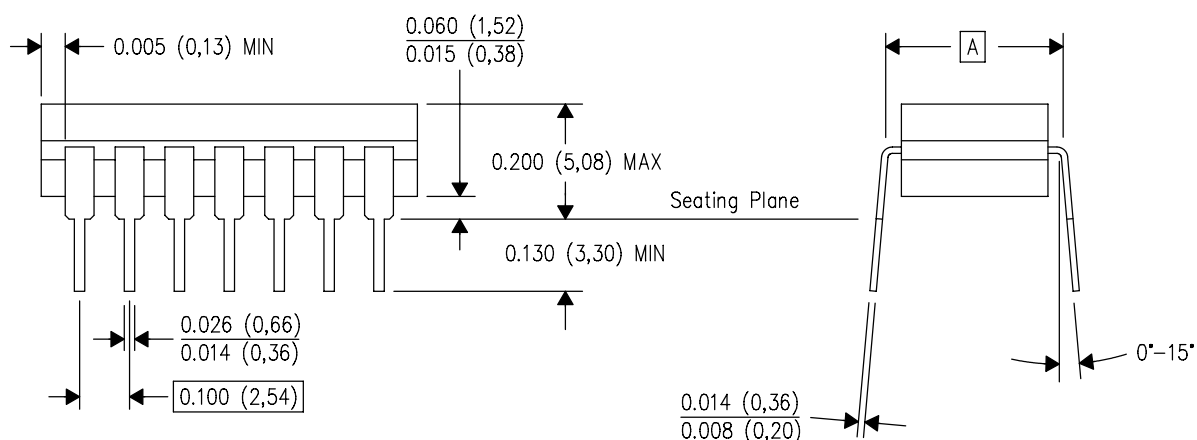
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



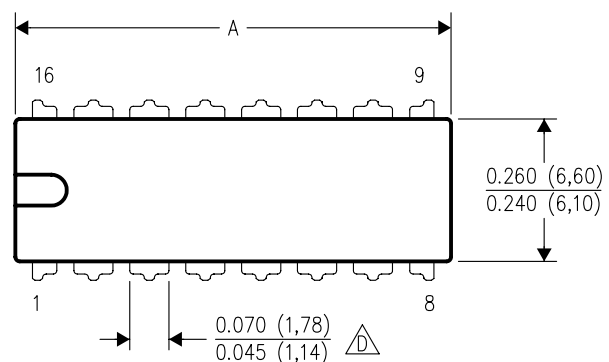
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

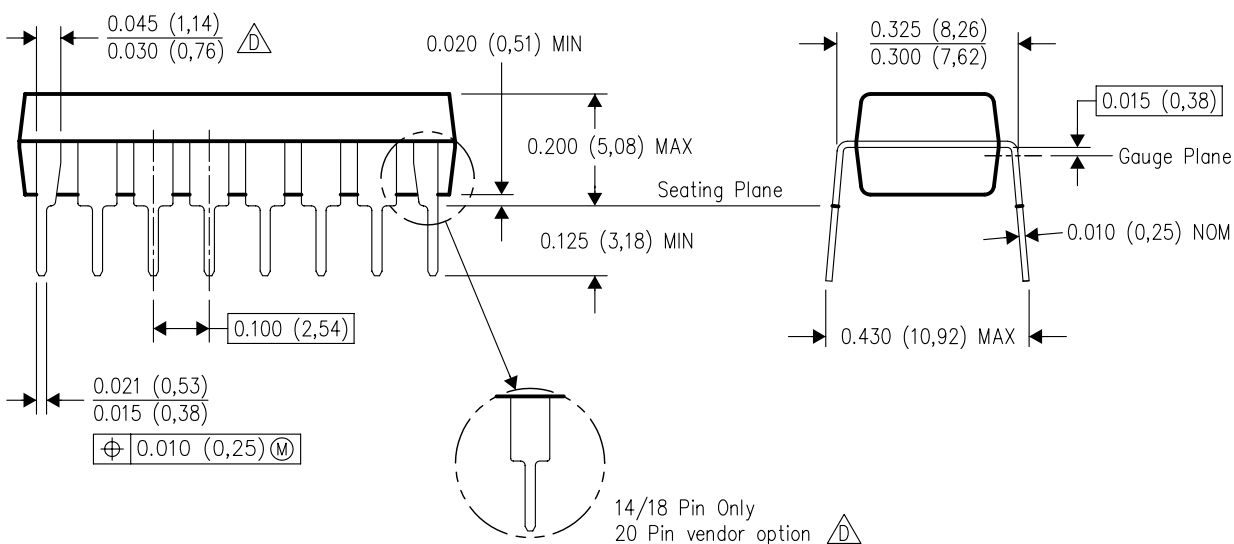
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

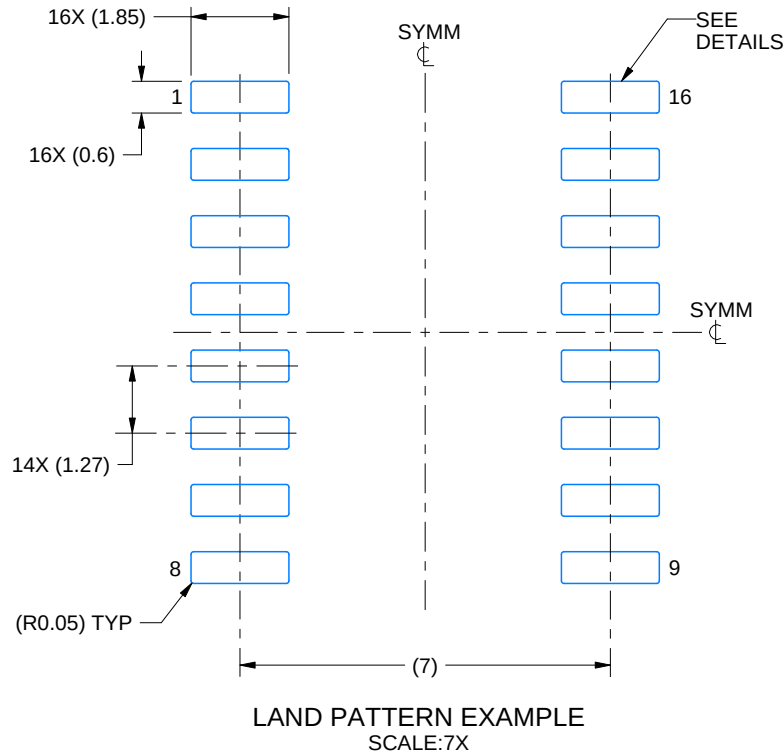
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

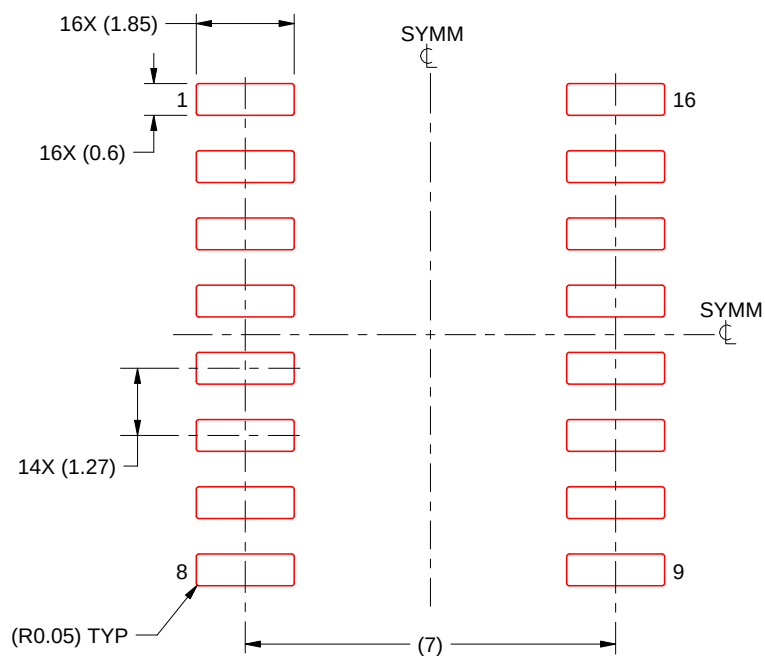
SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025