

# SN54AS194, SN74AS194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

SDAS212A – DECEMBER 1983 – REVISED DECEMBER 1994

- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts
- Parallel Synchronous Loading
- Direct Overriding Clear
- Temporary Data-Latching Capability
- Package Options Include Plastic Small-Outline Packages (D), Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

These 4-bit bidirectional universal shift registers feature parallel outputs, right-shift and left-shift serial (SR SER, SL SER) inputs, operating-mode-control (S<sub>0</sub>, S<sub>1</sub>) inputs, and a direct overriding clear ( $\overline{\text{CLR}}$ ) line. The registers have four distinct modes of operation:

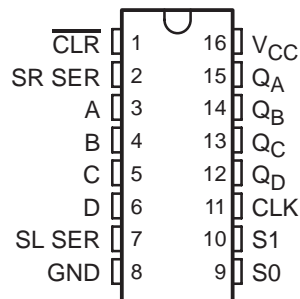
- Inhibit clock (temporary data latch/do nothing)
- Shift right (in the direction Q<sub>A</sub> toward Q<sub>D</sub>)
- Shift left (in the direction Q<sub>D</sub> toward Q<sub>A</sub>)
- Parallel (broadside) load

Parallel synchronous loading is accomplished by applying the four bits of data and taking both S<sub>0</sub> and S<sub>1</sub> high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.

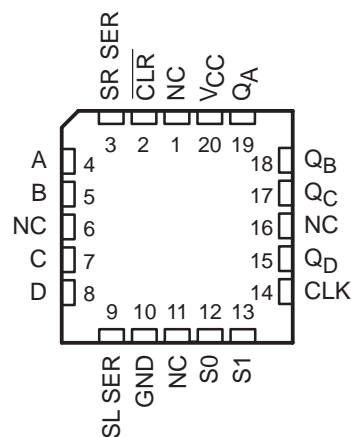
Shift right is accomplished synchronously with the rising edge of the clock pulse when S<sub>0</sub> is high and S<sub>1</sub> is low. Serial data for this mode is entered at the shift-right data input. When S<sub>0</sub> is low and S<sub>1</sub> is high, data shifts left synchronously and new data is entered at the shift-left serial inputs. Clocking of the flip-flop is inhibited when both mode-control inputs are low.

The SN54AS194 is characterized for operation over the full military temperature range of -55°C to 125°C. The SN74AS194 is characterized for operation from 0°C to 70°C.

SN54AS194 . . . J PACKAGE  
SN74AS194 . . . D OR N PACKAGE  
(TOP VIEW)



SN54AS194 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

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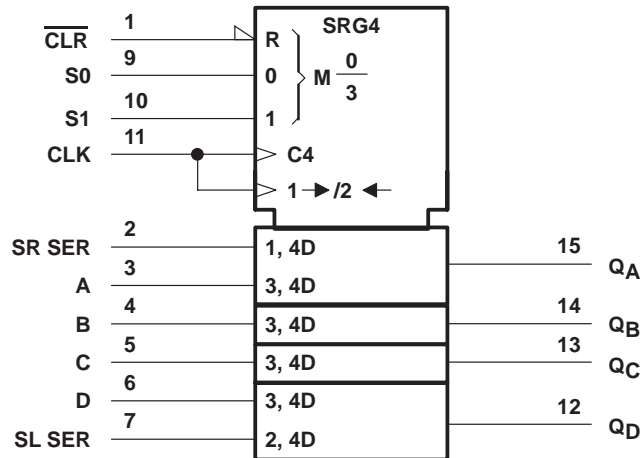
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FUNCTION TABLE

$\overline{\text{CLR}}$	MODE		CLK	SERIAL		PARALLEL				OUTPUTS			
	S1	S0		LEFT	RIGHT	A	B	C	D	QA	QB	QC	QD
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

H = high level (steady state); L = low level (steady state); X = irrelevant (any input, including transitions); ↑ = transition from low to high level; a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively; QA0, QB0, QC0, QD0 = the level of QA, QB, QC, or QD, respectively, before the indicated steady-state input conditions were established; QAn, QBn, QCn, QDn = the level of QA, QB, QC, respectively, before the most recent ↑ transition of the clock.

## logic symbol†

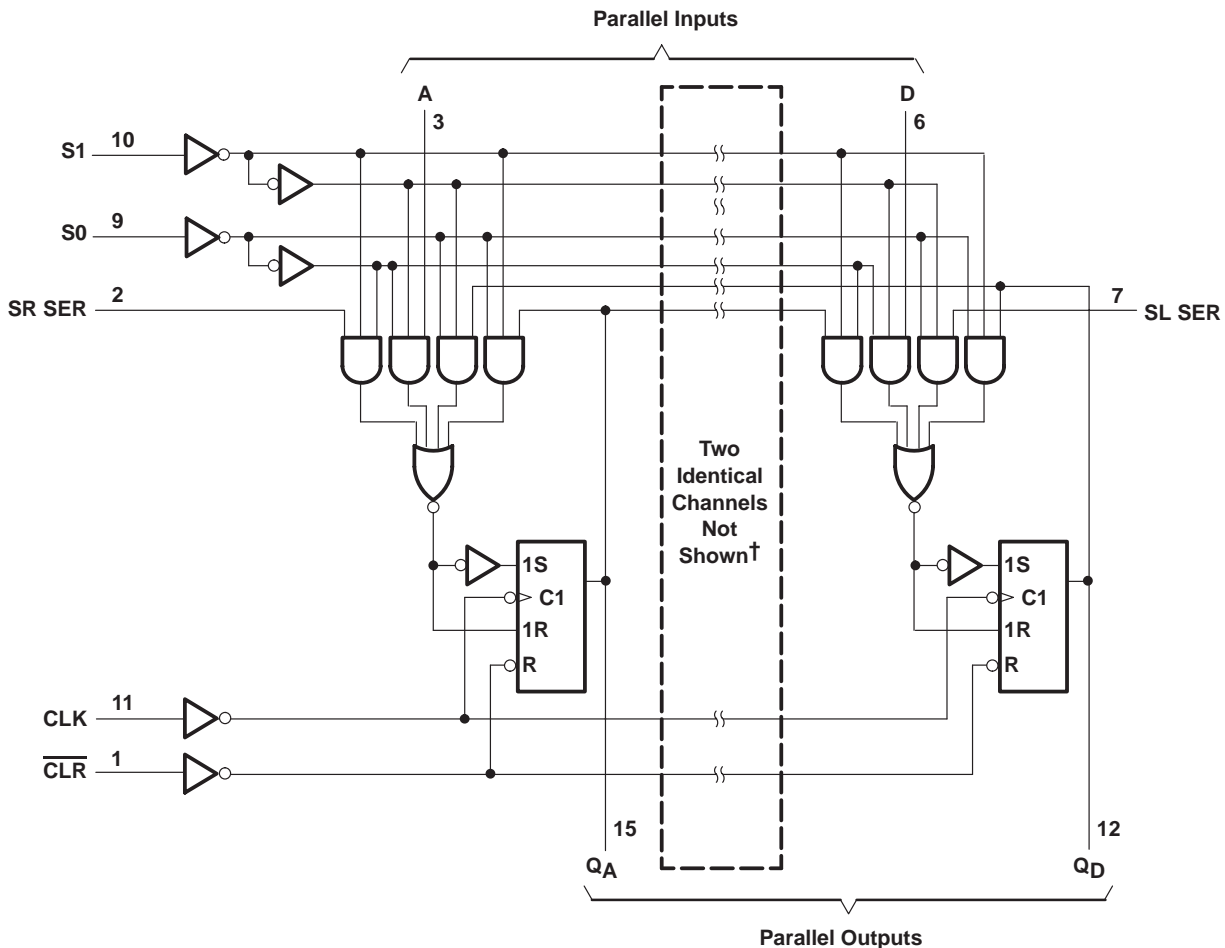


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)



† I/O ports not shown:  $Q_B$  (14) and  $Q_C$  (13)  
Pin numbers shown are for the D, J, and N packages.



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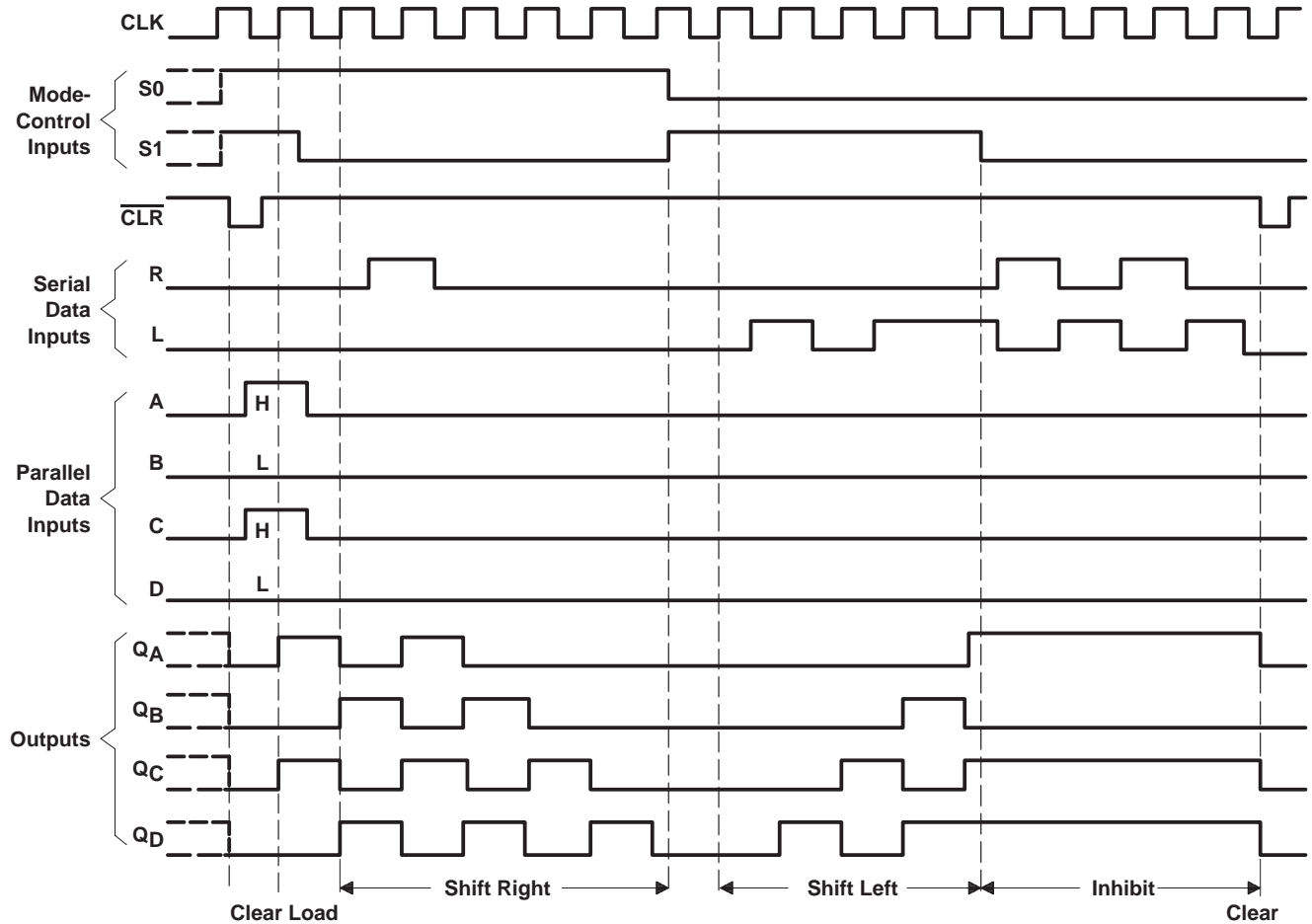


Figure 1. Typical Clear, Load, Right-Shift, and Clear Sequences

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$	7 V
Operating free-air temperature range, $T_A$ : SN54AS194	-55°C to 125°C
SN74AS194	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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## recommended operating conditions

		SN54AS194			SN74AS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$I_{OH}$	High-level output current			-2			-2	mA
$I_{OL}$	Low-level output current			20			20	mA
$f_{clock}^*$	Clock frequency	0		75	0		80	MHz
$t_w^*$	Pulse duration	$\overline{CLR}$		4		4.5		ns
		CLK high		4		4		
		CLK low		6		7		
$t_{su}^*$	Setup time before CLK $\uparrow$	Select		9		9.5		ns
		Data		3.5		4		
		Clear inactive state		6		6		
$t_h^*$	Hold time, data after CLK $\uparrow$		0.5			0.5		ns
$T_A$	Operating free-air temperature		-55	125		0	70	$^{\circ}C$

\* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS194			SN74AS194			UNIT
				MIN	TYP $\dagger$	MAX	MIN	TYP $\dagger$	MAX	
$V_{IK}$		$V_{CC} = 4.5 V,$	$I_I = -18 mA$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = 4.5 V$ to $5.5 V,$	$I_{OH} = -2 mA$	$V_{CC}-2$			$V_{CC}-2$			V
$V_{OL}$		$V_{CC} = 4.5 V,$	$I_{OL} = 20 mA$		0.35	0.5		0.35	0.5	V
$I_I$	Data, CLK, $\overline{CLR}$	$V_{CC} = 5.5 V,$	$V_I = 7 V$			0.1		0.1		mA
	Mode, SL, SR					0.2		0.2		
$I_{IH}$	Data, CLK, $\overline{CLR}$	$V_{CC} = 5.5 V,$	$V_I = 2.7 V$			20		20		$\mu A$
	Mode, SL, SR					40		40		
$I_{IL}$	Data, CLK, $\overline{CLR}$	$V_{CC} = 5.5 V,$	$V_I = 0.4 V$			-0.5		-0.5		mA
	Mode, SL, SR					-1		-1		
$I_{O\ddagger}$		$V_{CC} = 5.5 V,$	$V_O = 2.25 V$	-30		-112	-30		-112	mA
$I_{CC}$		$V_{CC} = 5.5 V$	Outputs high		30	49		30	43	mA
			Outputs low		38	60		38	53	

$\dagger$  All typical values are at  $V_{CC} = 5 V,$   $T_A = 25^{\circ}C.$

$\ddagger$  The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current,  $I_{OS}.$



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### switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX†				UNIT
			SN54AS194		SN74AS194		
			MIN	MAX	MIN	MAX	
f <sub>max</sub> *			75		80		MHz
t <sub>PLH</sub>	CLK	Any Q	2.5	8	3	7	ns
t <sub>PHL</sub>			2.5	8	3	7	
t <sub>PHL</sub>	CLR	Any Q	3.5	13	4	12	ns

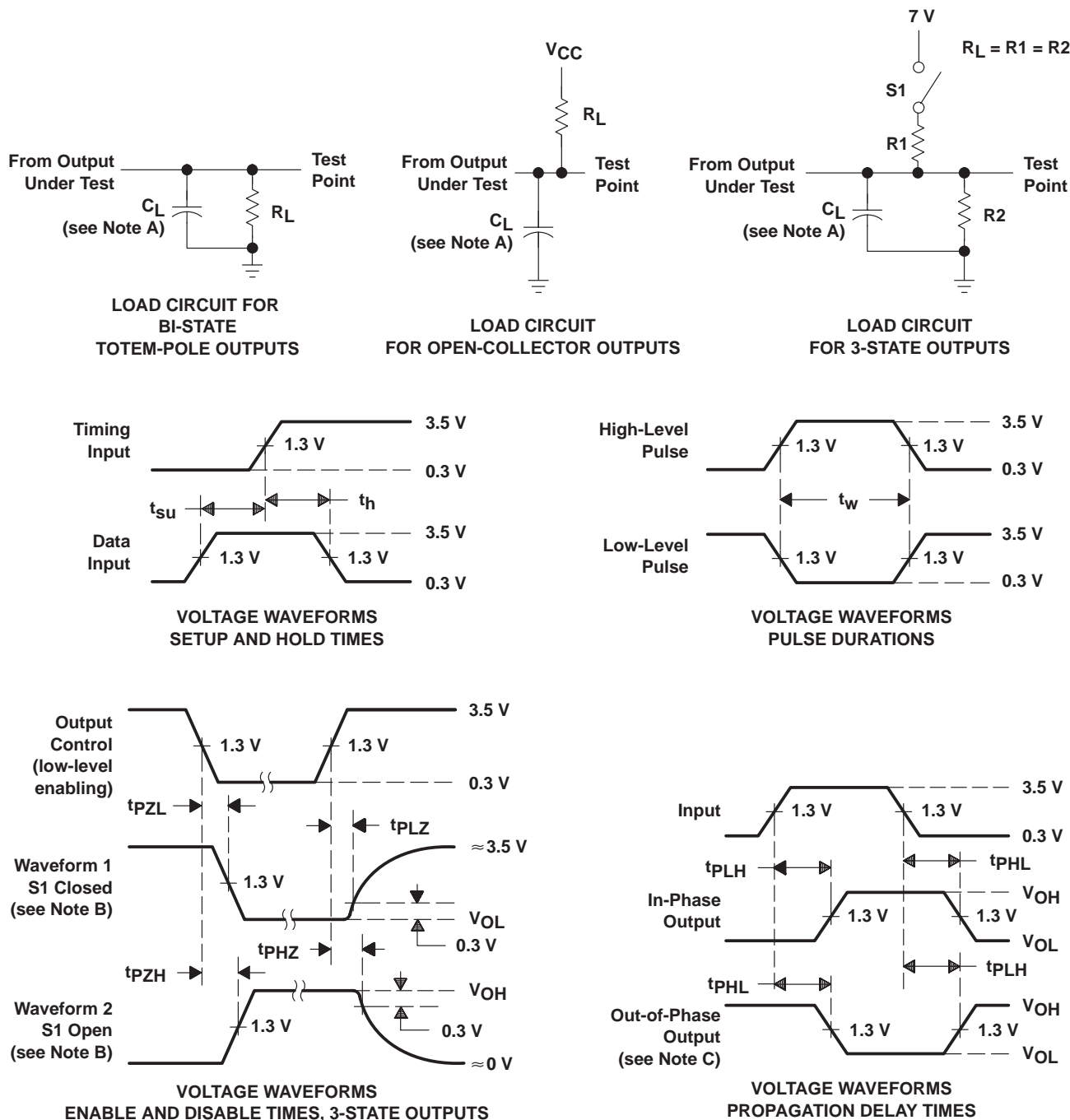
\* On products compliant to MIL-STD-883, Class B, these parameters are based on characterization data, but are not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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## PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.  
 D. All input pulses have the following characteristics:  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%.  
 E. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuits and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AS194D</a>	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	AS194
<a href="#">SN74AS194DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS194
SN74AS194DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	AS194

**(1) Status:** For more details on status, see our [product life cycle](#).

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AS194DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AS194DR	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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