

SN74AUP1G07 Low-Power Single Buffer/Driver With Open-Drain Outputs

1 Features

- Available in the Ultra Small 0.64 mm² Package (DPW) with 0.5-mm Pitch
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A}$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 1 \text{ pF}$ Typical at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot <math><10\% \text{ of } V_{CC}</math>
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys} = 250 \text{ mV}$ Typ at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 3.3 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

2 Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card
- X-ray: Baggage Scanner, Medical, and Dental

3 Description

The SN74AUP1G07 device is a single buffer gate with open drain output that operates from 0.8 V to 3.6 V.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| SN74AUP1G07 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| | SOT (5) | 2.00 mm × 1.25 mm |
| | SOT (5) | 1.60 mm × 1.20 mm |
| | USON (6) | 1.45 mm × 1.00 mm |
| | X2SON (4) | 0.80 mm × 0.80 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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5 Revision History

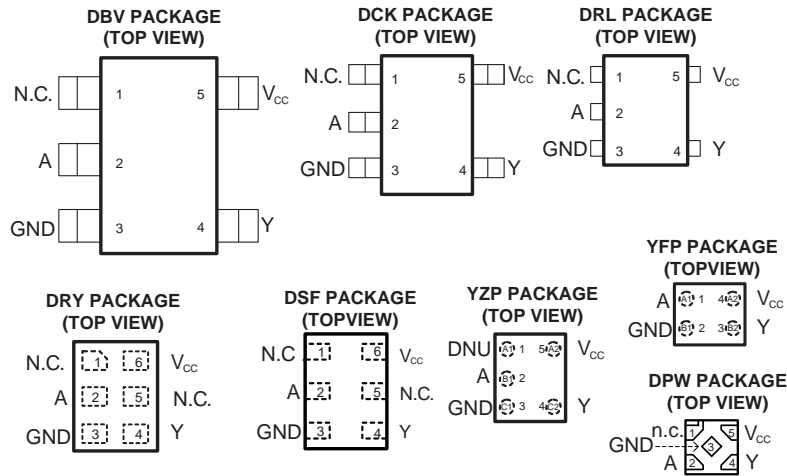
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision I (October 2012) to Revision J | Page |
|---|-------------|
| • Updated document to new TI data sheet format | 1 |
| • Removed Ordering Information table | 1 |
| • Updated I_{off} in Features. | 1 |
| • Added Applications | 1 |
| • Added Handling Ratings table | 4 |
| • Added Thermal Information table | 5 |
| • Added Typical Characteristics | 7 |

| Changes from Revision H (September 2012) to Revision I | Page |
|---|-------------|
| • Updated DPW package pinout | 3 |

| Changes from Revision F (May 2010) to Revision G | Page |
|---|-------------|
| • Changed V_{CC} to reflect updated condition | 4 |

6 Pin Configuration and Functions



N.C. – No internal connection.

DNU – Do not use

See mechanical drawings for dimensions.

Pin Functions

| NAME | PIN | | | | | I/O | DESCRIPTION |
|------|---------------|----------|-----|-----|-----|-----|---------------|
| | DBV, DCK, DRL | DSF, DRY | YFP | DPW | YZP | | |
| NC | 1 | 1, 5 | — | 1 | A1 | — | No Connection |
| A | 2 | 2 | A1 | 2 | B1 | I | Input A |
| GND | 3 | 3 | B1 | 3 | C1 | — | Ground Pin |
| Y | 4 | 4 | B2 | 4 | C2 | O | Output Y |
| VCC | 5 | 6 | A2 | 5 | A2 | — | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 4.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 4.6 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±20 | mA |
| | Continuous current through V _{CC} or GND | | ±50 | mA |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|--------------------|---------------------------|--|-----|------|---|
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|------------------------------------|-----------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 0.8 | 3.6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 0.8 V | V _{CC} | V |
| | | V _{CC} = 1.0 V to 1.95 V | 0.65 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.6 | |
| | | V _{CC} = 3 V to 3.6 V | 2 | |
| V _{IL} | Low-level input voltage | V _{CC} = 0.8 V | 0 | V |
| | | V _{CC} = 1.0 V to 1.95 V | 0.35 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| | | V _{CC} = 3 V to 3.6 V | 0.9 | |
| V _I | Input voltage | 0 | 3.6 | V |
| V _O | Output voltage | 0 | 3.6 | V |
| I _{OL} | Low-level output current | V _{CC} = 0.8 V | 20 | mA |
| | | V _{CC} = 1.1 V | 1.1 | |
| | | V _{CC} = 1.4 V | 1.7 | |
| | | V _{CC} = 1.65 V | 1.9 | |
| | | V _{CC} = 2.3 V | 3.1 | |
| | | V _{CC} = 3 V | 4 | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 0.8 V to 3.6 V | 200 | ns/V |
| T _A | Operating free-air temperature | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DBV | DCK | DPW | DRL | DRY | DSF | UNIT |
|-------------------------------|--|--------|--------|--------|--------|--------|--------|------|
| | | 5 PINS | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 6 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 298.6 | 314.4 | 291.8 | 349.7 | 554.9 | 407.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 240.2 | 128.7 | 224.2 | 120.5 | 385.4 | 232.0 | |
| R _{θJB} | Junction-to-board thermal resistance | 134.6 | 100.6 | 245.8 | 171.4 | 388.2 | 306.9 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 114.5 | 7.1 | 31.4 | 10.8 | 159.0 | 40.3 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 133.9 | 99.8 | 245.6 | 169.4 | 384.1 | 306.0 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | n/a | 195.4 | n/a | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | T _A = -40°C to 85°C | | UNIT |
|-------------------|---|--|-----------------------|-----|-----------------------|--------------------------------|-----------------------|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| V _{OL} | I _{OL} = 20 μA | 0.8 V to 3.6 V | | | 0.1 | | 0.1 | V |
| | I _{OL} = 1.1 mA | 1.1 V | | | 0.3 × V _{CC} | | 0.3 × V _{CC} | |
| | I _{OL} = 1.7 mA | 1.4 V | | | 0.31 | | 0.37 | |
| | I _{OL} = 1.9 mA | 1.65 V | | | 0.31 | | 0.35 | |
| | I _{OL} = 2.3 mA | 2.3 V | | | 0.31 | | 0.33 | |
| | I _{OL} = 3.1 mA | | | | 0.44 | | 0.45 | |
| | I _{OL} = 2.7 mA | 3 V | | | 0.31 | | 0.33 | |
| | I _{OL} = 4 mA | | | | 0.44 | | 0.45 | |
| I _I | A input | V _I = GND to 3.6 V | | | 0.1 | | 0.5 | μA |
| I _{off} | | V _I or V _O = 0 V to 3.6 V | | | 0.2 | | 0.6 | μA |
| ΔI _{off} | | V _I or V _O = 0 V to 3.6 V | | | 0.2 | | 0.6 | μA |
| I _{CC} | | V _I = GND or V _{CC} to 3.6 V, I _O = 0 | | | 0.5 | | 0.9 | μA |
| ΔI _{CC} | | V _I = V _{CC} - 0.6 V, I _O = 0 | | | 40 | | 50 | μA |
| C _i | V _I = V _{CC} or GND | 0 V | | 1.5 | | | | pF |
| | | 3.6 V | | 1.7 | | | | |
| C _o | V _O = GND | 0 V | | 1.7 | | | | pF |

7.6 Switching Characteristics, C_L = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | T _A = -40°C to 85°C | | UNIT |
|-----------------|--------------|-------------|-----------------|-----------------------|------|-----|--------------------------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t _{pd} | A | Y | 0.8 V | | 12.2 | | | | ns |
| | | | 1.2 V ± 0.1 V | 3.4 | 5.1 | 7.5 | 1.5 | 14.7 | |
| | | | 1.5 V ± 0.1 V | 2.3 | 3.6 | 5.1 | 1.3 | 8.3 | |
| | | | 1.8 V ± 0.15 V | 2.4 | 3.1 | 4 | 1 | 6.3 | |
| | | | 2.5 V ± 0.2 V | 1.5 | 2.1 | 2.9 | 0.9 | 4.1 | |
| | | | 3.3 V ± 0.3 V | 1.8 | 2.2 | 2.8 | 1.1 | 3.3 | |

7.7 Switching Characteristics, $C_L = 10\text{ pF}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C}$ to 85°C | | UNIT |
|-----------|--------------|-------------|----------------------------------|--------------------------|-----|-----|--|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 0.8 V | | 15 | | | | ns |
| | | | $1.2\text{ V} \pm 0.1\text{ V}$ | 4 | 6.2 | 9 | 2.4 | 16.2 | |
| | | | $1.5\text{ V} \pm 0.1\text{ V}$ | 3.1 | 4.4 | 6.1 | 2 | 9.4 | |
| | | | $1.8\text{ V} \pm 0.15\text{ V}$ | 3.3 | 3.9 | 4.8 | 1.6 | 7.1 | |
| | | | $2.5\text{ V} \pm 0.2\text{ V}$ | 2.1 | 2.8 | 3.5 | 1.3 | 4.8 | |
| | | | $3.3\text{ V} \pm 0.3\text{ V}$ | 2.3 | 3 | 4 | 1.4 | 4.5 | |

7.8 Switching Characteristics, $C_L = 15\text{ pF}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C}$ to 85°C | | UNIT |
|-----------|--------------|-------------|----------------------------------|--------------------------|------|------|--|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 0.8 V | | 18.2 | | | | ns |
| | | | $1.2\text{ V} \pm 0.1\text{ V}$ | 4.9 | 7.3 | 10.4 | 3.2 | 17.6 | |
| | | | $1.5\text{ V} \pm 0.1\text{ V}$ | 3.8 | 5.2 | 6.8 | 2.6 | 10.2 | |
| | | | $1.8\text{ V} \pm 0.15\text{ V}$ | 3.4 | 4.8 | 6.7 | 2.2 | 7.9 | |
| | | | $2.5\text{ V} \pm 0.2\text{ V}$ | 2.4 | 3.4 | 4.5 | 1.9 | 5.3 | |
| | | | $3.3\text{ V} \pm 0.3\text{ V}$ | 2.2 | 3.7 | 5.4 | 1.8 | 6.1 | |

7.9 Switching Characteristics, $C_L = 30\text{ pF}$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

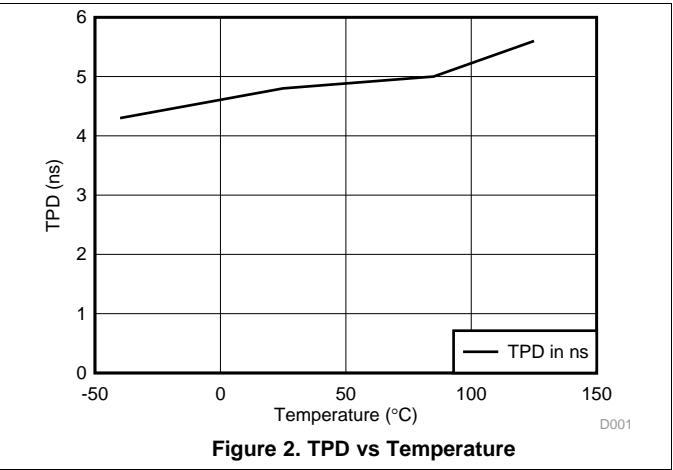
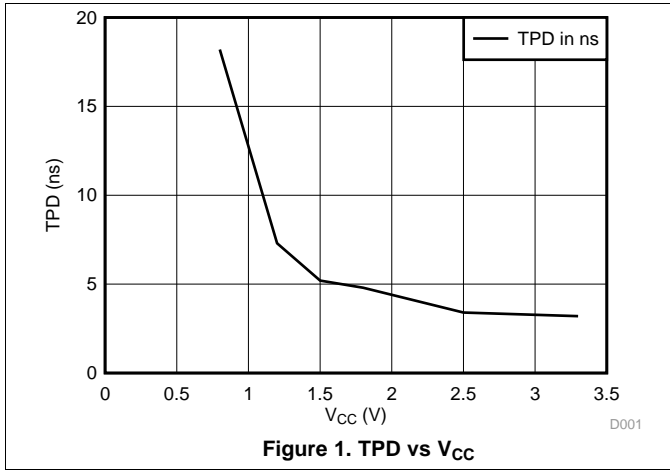
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | $T_A = -40^\circ\text{C}$ to 85°C | | UNIT |
|-----------|--------------|-------------|----------------------------------|--------------------------|------|------|--|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 0.8 V | | 26.5 | | | | ns |
| | | | $1.2\text{ V} \pm 0.1\text{ V}$ | 8.1 | 10.7 | 14.4 | 4.5 | 21.9 | |
| | | | $1.5\text{ V} \pm 0.1\text{ V}$ | 6.5 | 7.7 | 9.4 | 3.8 | 13 | |
| | | | $1.8\text{ V} \pm 0.15\text{ V}$ | 5.8 | 7.5 | 9.7 | 3.2 | 11 | |
| | | | $2.5\text{ V} \pm 0.2\text{ V}$ | 4.5 | 5.4 | 6.7 | 3 | 7.1 | |
| | | | $3.3\text{ V} \pm 0.3\text{ V}$ | 3.9 | 6.3 | 9.7 | 2.8 | 10.4 | |

7.10 Operating Characteristics

 $T_A = 25^\circ\text{C}$

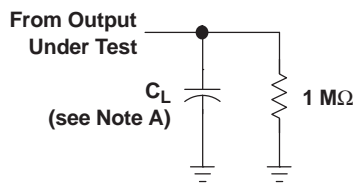
| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|---------------------|----------------------------------|-----|------|
| C_{pd} | Power dissipation capacitance | $f = 10\text{ MHz}$ | 0.8 V | 1 | pF |
| | | | $1.2\text{ V} \pm 0.1\text{ V}$ | 1 | |
| | | | $1.5\text{ V} \pm 0.1\text{ V}$ | 1 | |
| | | | $1.8\text{ V} \pm 0.15\text{ V}$ | 1 | |
| | | | $2.5\text{ V} \pm 0.2\text{ V}$ | 1 | |
| | | | $3.3\text{ V} \pm 0.3\text{ V}$ | 1 | |

7.11 Typical Characteristics



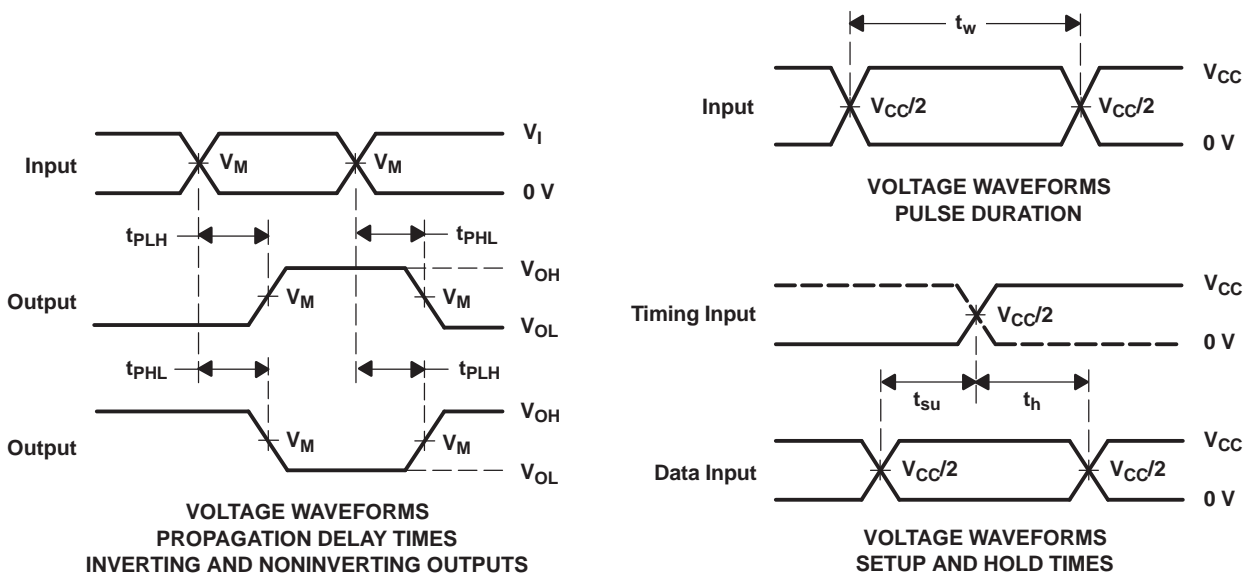
8 Parameter Measurement Information

8.1 Propagation Delays, Setup and Hold Times, and Pulse Duration



LOAD CIRCUIT

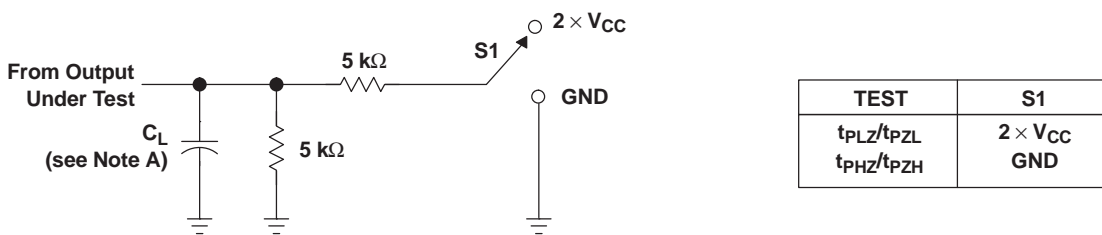
| | $V_{CC} = 0.8\text{ V}$ | $V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$ | $V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$ | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |
|-------|-------------------------|--|--|---|--|--|
| C_L | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| V_M | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| V_I | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r/t_f = 3\text{ ns}$.
 - C. The outputs are measured one at a time, with one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - E. All parameters and waveforms are not applicable to all devices.

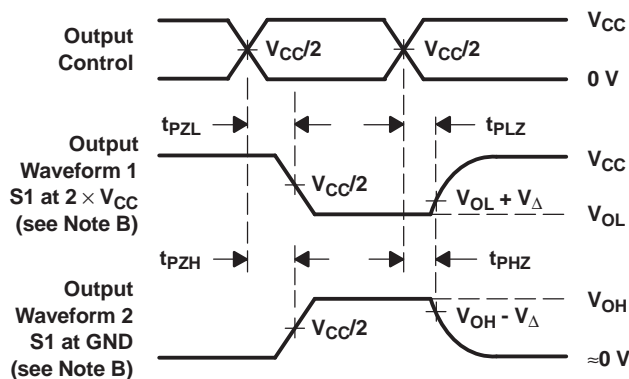
Figure 3. Load Circuit and Voltage Waveforms

8.2 Enable and Disable Times



LOAD CIRCUIT

| | $V_{CC} = 0.8 \text{ V}$ | $V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$ | $V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$ | $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |
|--------------|--------------------------|--|--|---|--|--|
| C_L | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| V_M | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ | $V_{CC}/2$ |
| V_I | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} | V_{CC} |
| V_{Δ} | 0.1 V | 0.1 V | 0.1 V | 0.15 V | 0.15 V | 0.3 V |



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

9 Detailed Description

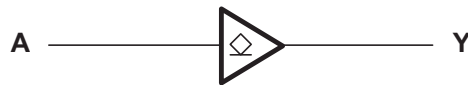
9.1 Overview

The SN74AUP1G07 device is a single buffer gate with open drain output that operates from 0.8 V to 3.6 V. The output of this single buffer/driver is open drain, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

The AUP family of devices has quiescent power consumption less than 1 μ A and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The I_{off} feature also allows for live insertion.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating V_{CC} range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- I_{off} feature allows voltages on the inputs and outputs when V_{CC} is 0 V
- Low noise due to slower edge rates

9.4 Device Functional Modes

Table 1. Function Table

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H/Z |
| L | L |

10 Application and Implementation

10.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

10.2 Typical Application

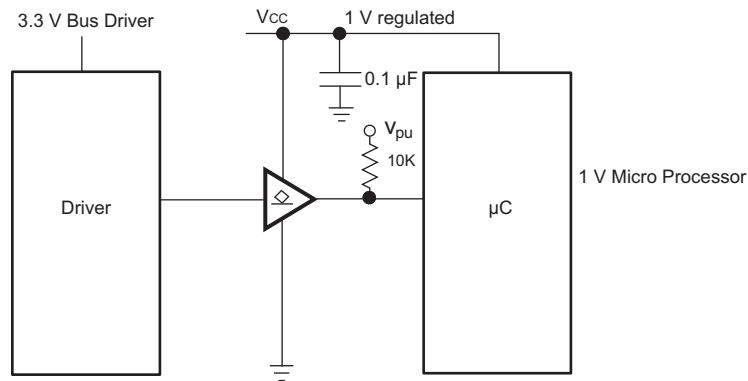


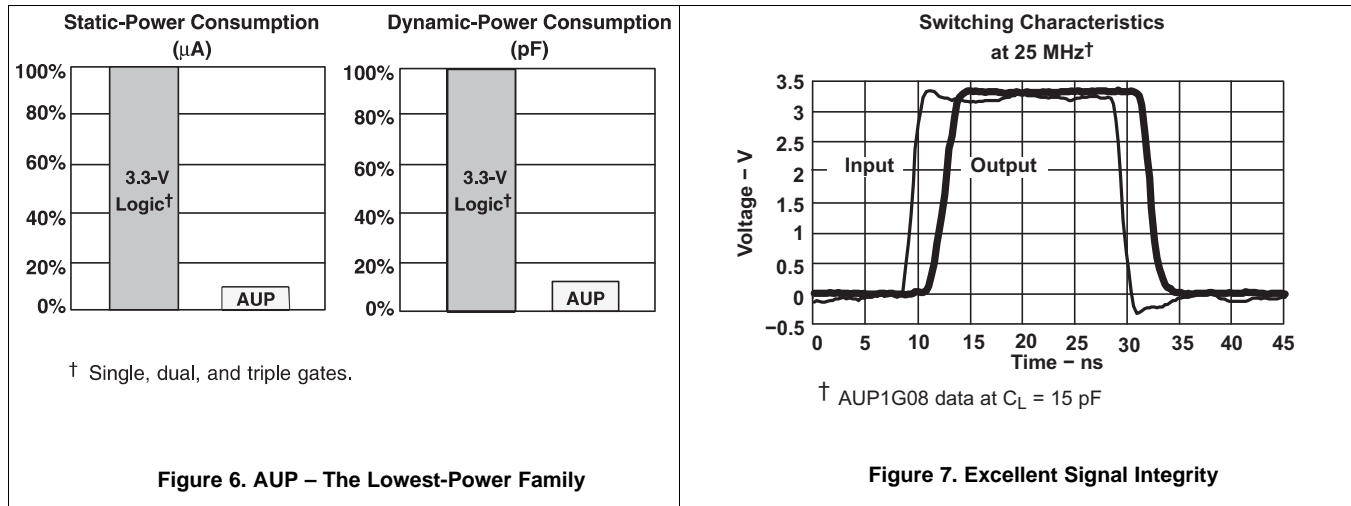
Figure 5. Typical Application Schematic

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

10.2.2 Detailed Design Procedure

1. Recommended Input conditions
 - Rise time and fall time specs. See $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#)
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#)
 - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
 - Load currents should not exceed 20 mA on the output and 50 mA total for the part

Typical Application (continued)
10.2.3 Application Curves


The AUP family of single gate logic makes excellent translators for the new lower voltage microprocessors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

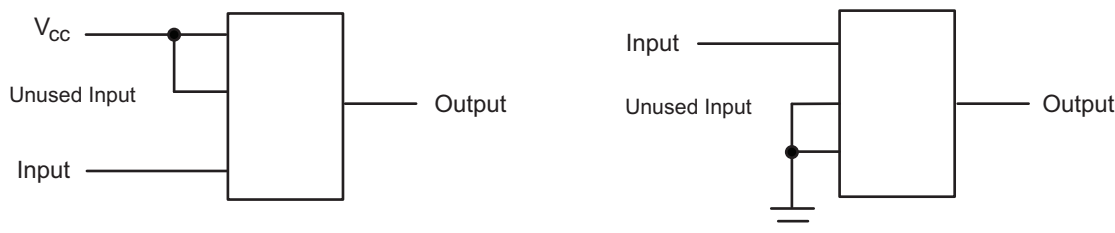


Figure 8. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

The I_{off} feature also allows for live insertion. is a trademark of others. All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-----------------------|
| SN74AUP1G07DBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (H07F, H07R) |
| SN74AUP1G07DBVR.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (H07F, H07R) |
| SN74AUP1G07DBVRE4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H07F |
| SN74AUP1G07DBVRG4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H07F |
| SN74AUP1G07DBVRG4.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | H07F |
| SN74AUP1G07DBVT | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (H07F, H07R) |
| SN74AUP1G07DBVT.B | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (H07F, H07R) |
| SN74AUP1G07DCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVF, HVK, HV R) |
| SN74AUP1G07DCKR.B | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVF, HVK, HV R) |
| SN74AUP1G07DCKRE4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVF, HVK, HV R) |
| SN74AUP1G07DCKRE4.B | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVF, HVK, HV R) |
| SN74AUP1G07DCKT | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVR) |
| SN74AUP1G07DCKT.B | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (HV5, HVR) |
| SN74AUP1G07DCKTG4 | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV5 |
| SN74AUP1G07DCKTG4.B | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV5 |
| SN74AUP1G07DPWR | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | D4 |
| SN74AUP1G07DPWR.B | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | D4 |
| SN74AUP1G07DRLR | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HV7, HVR) |
| SN74AUP1G07DRLR.B | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | (HV7, HVR) |
| SN74AUP1G07DRYR | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DRYR.B | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DRYRG4 | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DRYRG4.B | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DSF2 | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DSF2.B | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DSFR | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | HV |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74AUP1G07DSFR.B | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DSFRG4 | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07DSFRG4.B | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HV |
| SN74AUP1G07YFPR | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | - | HV N |
| SN74AUP1G07YFPR.B | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HV N |
| SN74AUP1G07YZPR | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HVN |
| SN74AUP1G07YZPR.B | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | HVN |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUP1G07DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKRE4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKRE4 | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74AUP1G07DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G07DRYRG4 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74AUP1G07DSF2 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| SN74AUP1G07DSFR | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUP1G07DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74AUP1G07YFPR | DSBGA | YFP | 4 | 3000 | 178.0 | 9.2 | 0.89 | 0.89 | 0.58 | 4.0 | 8.0 | Q1 |
| SN74AUP1G07YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUP1G07DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74AUP1G07DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G07DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G07DCKR | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74AUP1G07DCKRE4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G07DCKRE4 | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G07DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G07DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G07DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74AUP1G07DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74AUP1G07DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74AUP1G07DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G07DRYRG4 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74AUP1G07DSF2 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G07DSFR | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G07DSFRG4 | SON | DSF | 6 | 5000 | 210.0 | 185.0 | 35.0 |
| SN74AUP1G07YFPR | DSBGA | YFP | 4 | 3000 | 220.0 | 220.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUP1G07YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

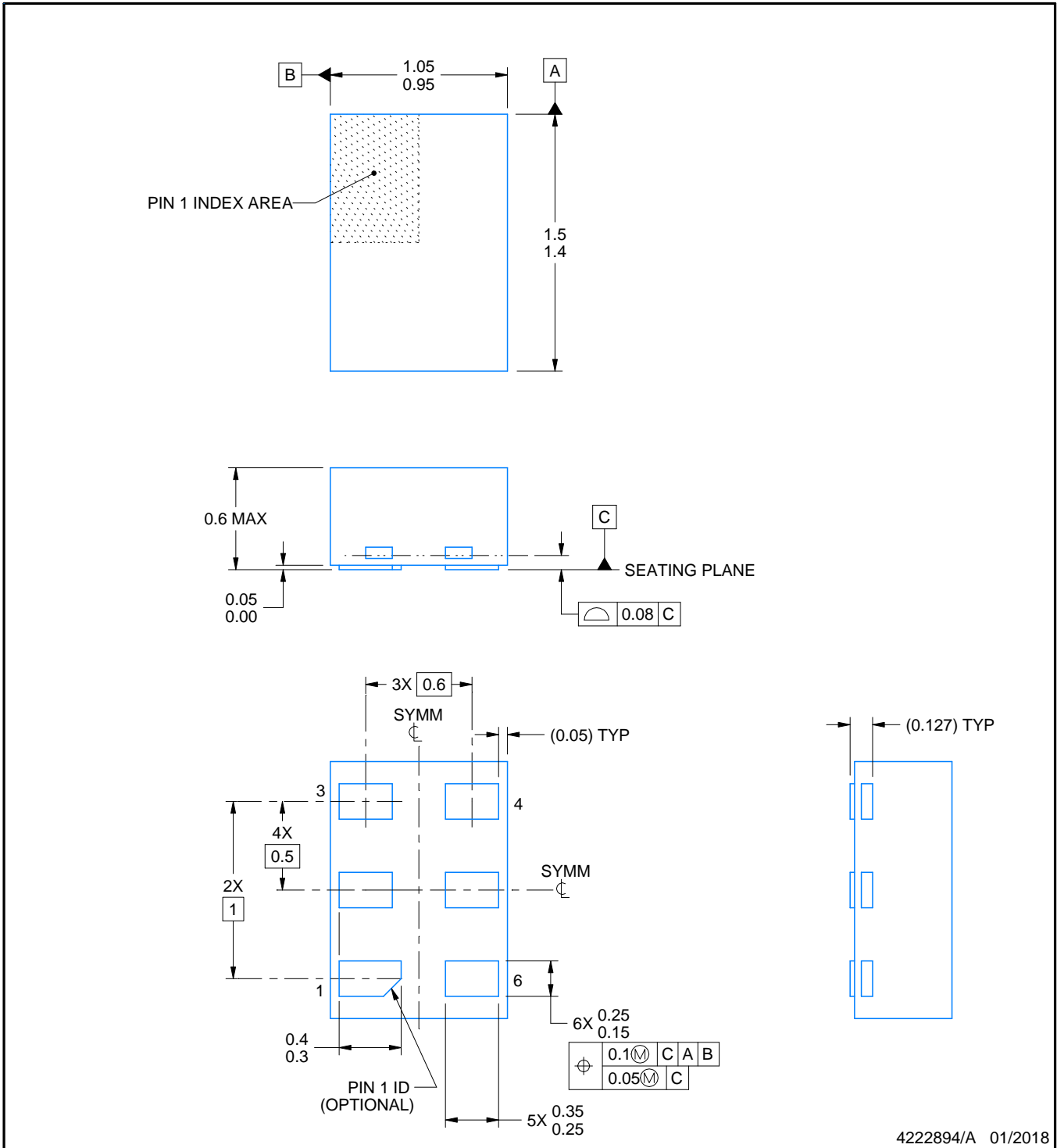
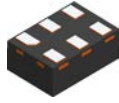
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

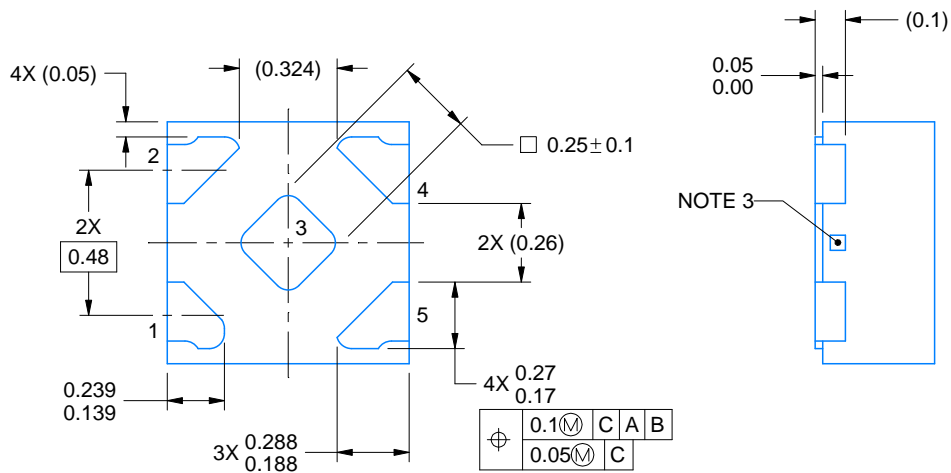
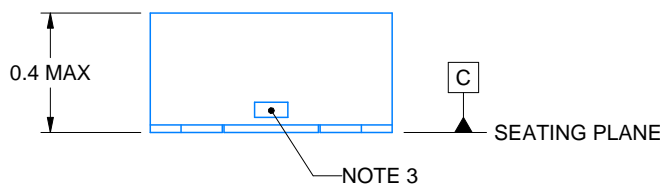
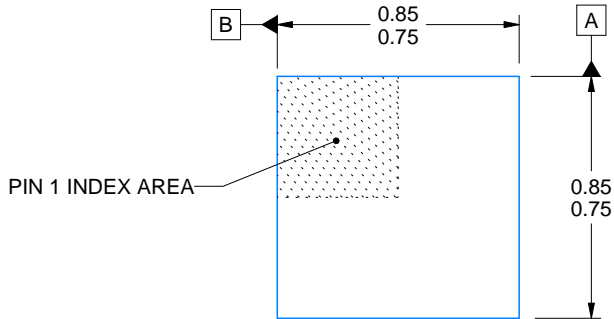
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

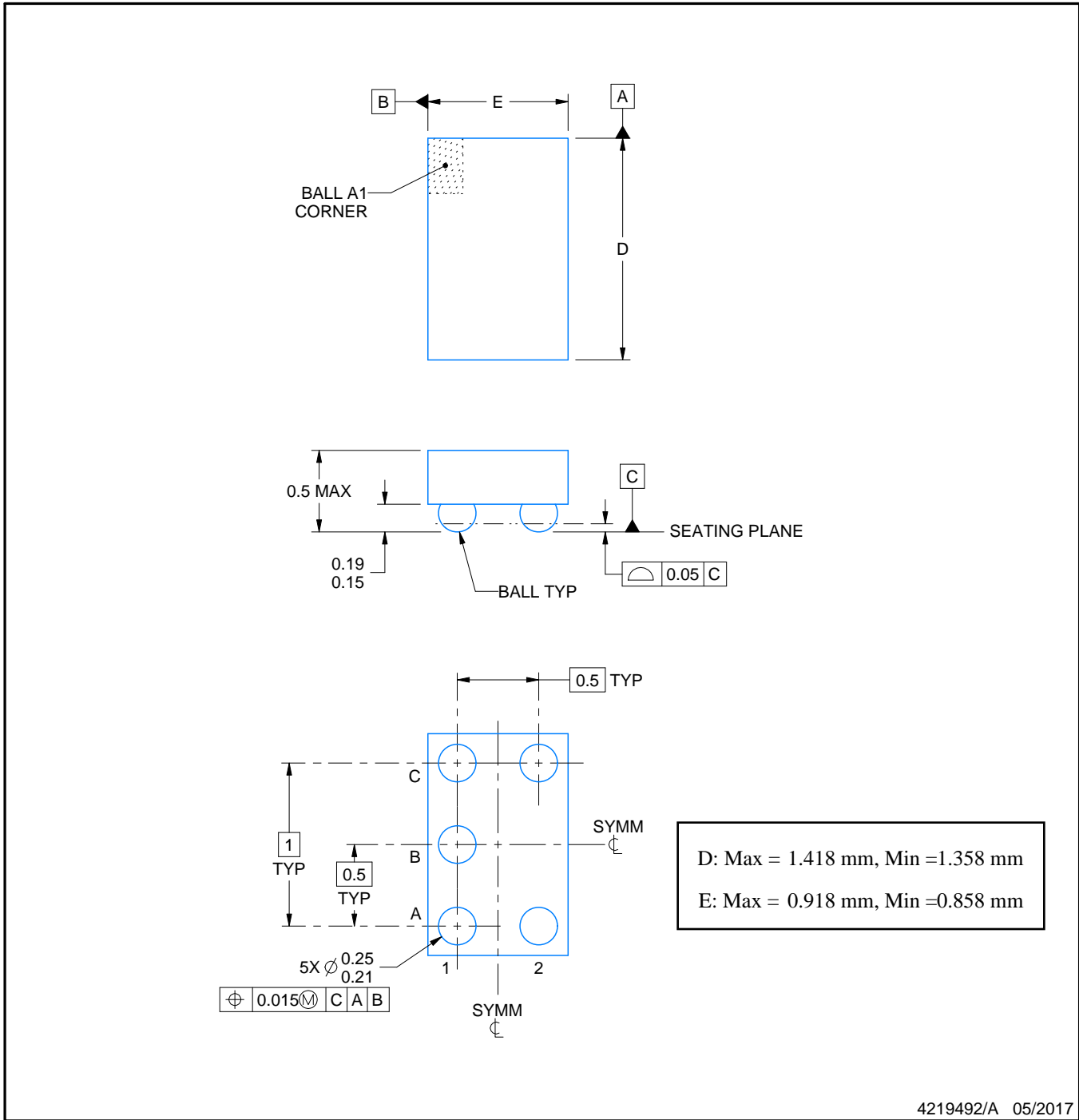
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

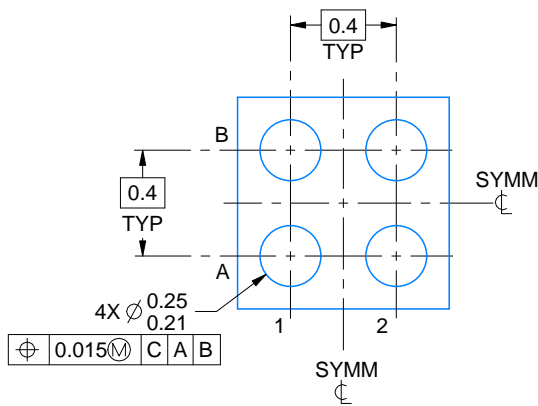
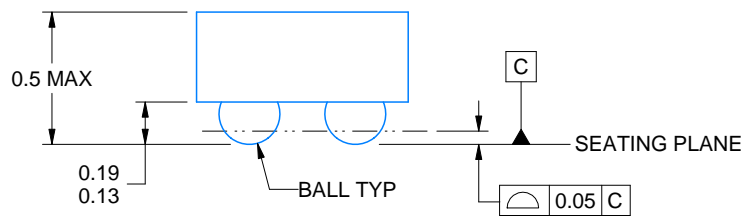
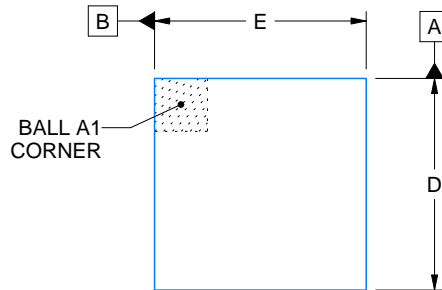


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



D: Max = 0.79 mm, Min = 0.73 mm
 E: Max = 0.79 mm, Min = 0.73 mm

4223507/A 01/2017

NOTES:

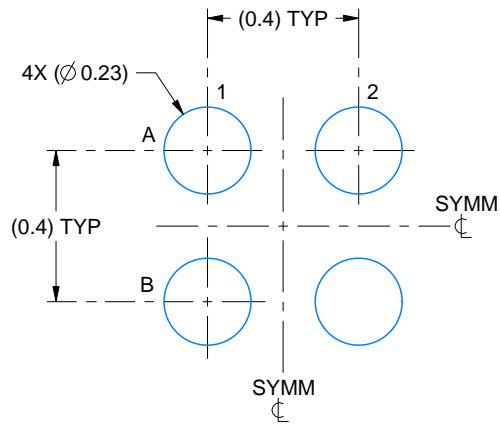
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

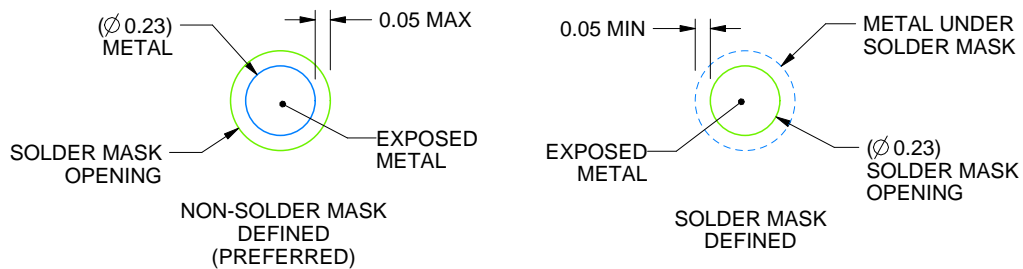
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

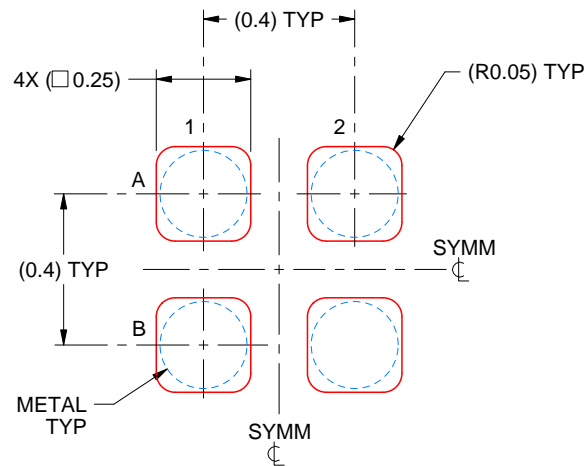
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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