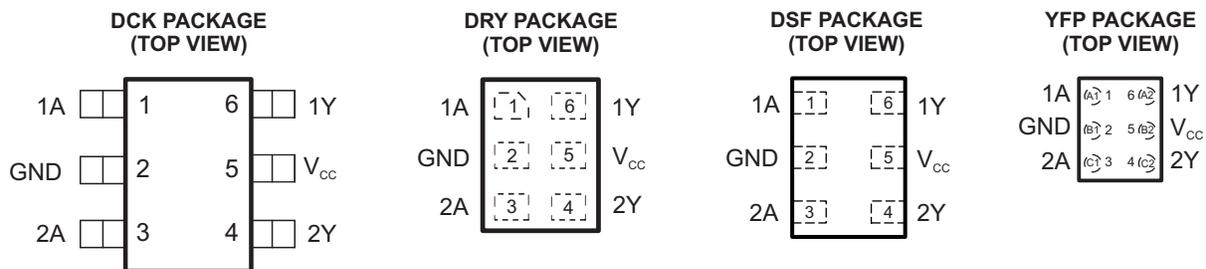


LOW-POWER DUAL SCHMITT-TRIGGER BUFFER

 Check for Samples: [SN74AUP2G17](#)

FEATURES

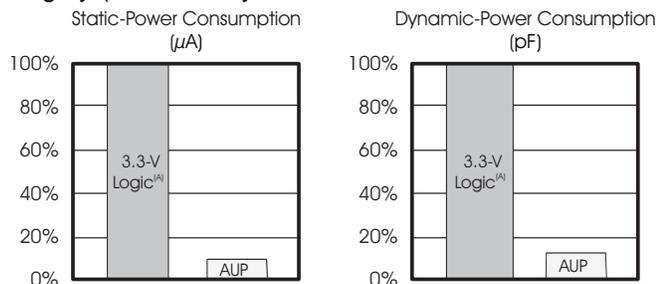
- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ($I_{CC} = 0.9 \mu\text{A}$ Maximum)
- Low Dynamic-Power Consumption ($C_{pd} = 4.3 \text{ pF}$ Typical at 3.3 V)
- Low Input Capacitance ($C_i = 1.5 \text{ pF}$ Typical)
- Low Noise – Overshoot and Undershoot <10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.1 \text{ ns}$ Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see [Figure 1](#)). This product also maintains excellent signal integrity (see the very low overshoot and undershoot characteristics shown in [Figure 2](#)).



(A) Single, dual, and triple gates

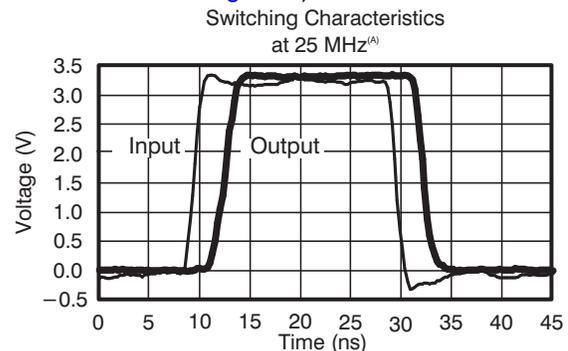
Figure 1. AUP – The Lowest-Power Family

 (A) SN74AUP2Gxx data at $C_L = 15 \text{ pF}$.

Figure 2. Excellent Signal Integrity


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The SN74AUP2G17 contains two buffers and performs the Boolean function $Y = A$. The device functions as two independent buffers, but because of Schmitt action, it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION^{(1) (2)}

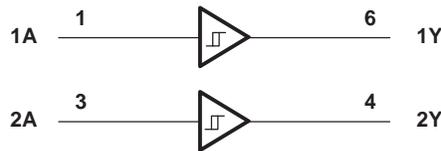
T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
-40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP2G17YFPR	___ H 7 _
	QFN – DSF	Reel of 5000	SN74AUP2G17DSFR	HL
	uQFN – DRY	Reel of 5000	SN74AUP2G17DRYR	HL
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP2G17DCKR	HL_

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (3) DCK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

**FUNCTION TABLE
(Each Inverter)**

INPUT A	OUTPUT Y
H	H
L	L

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	-0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	4.6	V
V_O	Output voltage range in the high or low state ⁽²⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50 mA
I_{OK}	Output clamp current	$V_O < 0$		-50 mA
I_O	Continuous output current			±20 mA
	Continuous current through V_{CC} or GND			±50 mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCK package		252
		DSF package		300
		DRY package		234
		YFP package		132
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	3.6	V
V_I	Input voltage	0	3.6	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$	-20	μA
		$V_{CC} = 1.1\text{ V}$	-1.1	mA
		$V_{CC} = 1.4\text{ V}$	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3\text{ V}$	-3.1	
		$V_{CC} = 3\text{ V}$	-4	
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	20	μA
		$V_{CC} = 1.1\text{ V}$	1.1	mA
		$V_{CC} = 1.4\text{ V}$	1.7	
		$V_{CC} = 1.65\text{ V}$	1.9	
		$V_{CC} = 2.3\text{ V}$	3.1	
		$V_{CC} = 3\text{ V}$	4	
T_A	Operating free-air temperature	-40	85	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V _{T+} Positive-going input threshold voltage		0.8 V	0.3		0.6	0.3	0.6	V
		1.1 V	0.53		0.9	0.53	0.9	
		1.4 V	0.74		1.11	0.74	1.11	
		1.65 V	0.91		1.29	0.91	1.29	
		2.3 V	1.37		1.77	1.37	1.77	
		3 V	1.88		2.29	1.88	2.29	
V _{T–} Negative-going input threshold voltage		0.8 V	0.1		0.6	0.1	0.6	V
		1.1 V	0.26		0.65	0.26	0.65	
		1.4 V	0.39		0.75	0.39	0.75	
		1.65 V	0.47		0.84	0.47	0.84	
		2.3 V	0.69		1.04	0.69	1.04	
		3 V	0.88		1.24	0.88	1.24	
ΔV _T Hysteresis (V _{T+} – V _{T–})		0.8 V	0.07		0.5	0.07	0.5	V
		1.1 V	0.08		0.46	0.08	0.46	
		1.4 V	0.18		0.56	0.18	0.56	
		1.65 V	0.27		0.66	0.27	0.66	
		2.3 V	0.53		0.92	0.53	0.92	
		3 V	0.79		1.31	0.79	1.31	
V _{OH}	I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1		V _{CC} – 0.1		V	
	I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}		0.7 × V _{CC}			
	I _{OH} = –1.7 mA	1.4 V	1.11		1.03			
	I _{OH} = –1.9 mA	1.65 V	1.32		1.3			
	I _{OH} = –2.3 mA	2.3 V	2.05		1.97			
	I _{OH} = –3.1 mA		1.9		1.85			
	I _{OH} = –2.7 mA	3 V	2.72		2.67			
	I _{OH} = –4 mA		2.6		2.55			
V _{OL}	I _{OL} = 20 μA	0.8 V to 3.6 V	0.1		0.1		V	
	I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}		0.3 × V _{CC}			
	I _{OL} = 1.7 mA	1.4 V	0.31		0.37			
	I _{OL} = 1.9 mA	1.65 V	0.31		0.35			
	I _{OL} = 2.3 mA	2.3 V	0.31		0.33			
	I _{OL} = 3.1 mA		0.44		0.45			
	I _{OL} = 2.7 mA	3 V	0.31		0.33			
	I _{OL} = 4 mA		0.44		0.45			
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V	0.1	0.5	μA		
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V	0.2	0.6	μA		
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V	0.2	0.6	μA		
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V	0.5	0.9	μA		
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V	40	50	μA		
C _i	V _I = V _{CC} or GND	0 V	1.5			pF		
		3.6 V	1.5					
C _o	V _O = GND	0 V	3			pF		

 (1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND.

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	22.7					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	6.3	8	12.8	3.9	14.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	4.6	5.8	8.4	2.8	10	
			$1.8\text{ V} \pm 0.15\text{ V}$	3.9	4.8	7.2	2.4	8.1	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.1	3.6	5.1	2	6.1	
			$3.3\text{ V} \pm 0.3\text{ V}$	2.7	3	4.4	1.9	5.1	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	25.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	7.1	9.1	13.8	4.7	15.6	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.2	6.5	9.4	3.4	11	
			$1.8\text{ V} \pm 0.15\text{ V}$	4.5	5.4	8	2.9	9	
			$2.5\text{ V} \pm 0.2\text{ V}$	3.5	4.2	5.7	2.4	6.8	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.1	3.5	4.9	2.2	5.7	

SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	27.6					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	7.8	10.1	14.8	5.3	16.7	
			$1.5\text{ V} \pm 0.1\text{ V}$	5.8	7.4	10.3	3.9	12	
			$1.8\text{ V} \pm 0.15\text{ V}$	5	6.1	8.8	3.4	10	
			$2.5\text{ V} \pm 0.2\text{ V}$	4	4.7	6.4	2.8	7.5	
			$3.3\text{ V} \pm 0.3\text{ V}$	3.5	4.1	5.4	2.6	6.2	

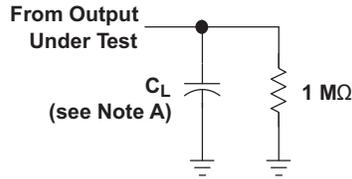
SWITCHING CHARACTERISTICSover recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.8 V	35.1					ns
			$1.2\text{ V} \pm 0.1\text{ V}$	10	13.1	18.1	7.5	19.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	7.4	9.6	12.9	5.6	14.9	
			$1.8\text{ V} \pm 0.15\text{ V}$	6.4	7.9	11	4.8	12.4	
			$2.5\text{ V} \pm 0.2\text{ V}$	5.2	6.1	7.9	4	9.3	
			$3.3\text{ V} \pm 0.3\text{ V}$	4.6	5.3	6.7	3.6	7.7	

OPERATING CHARACTERISTICS
 $T_A = 25^\circ\text{C}$

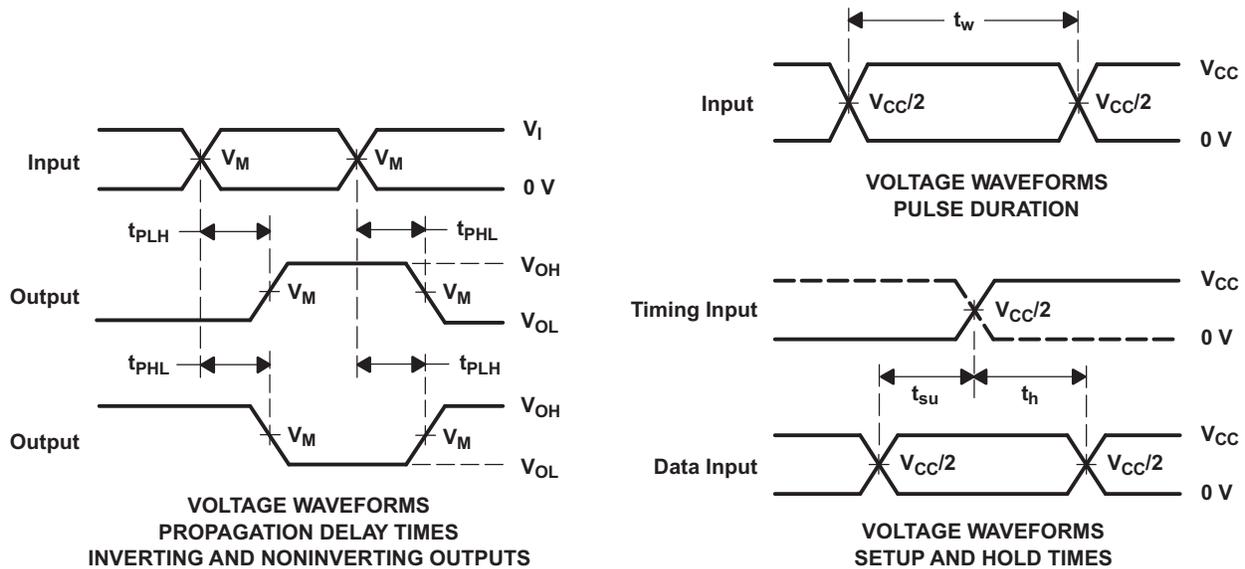
PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
			1.2 V ± 0.1 V	4	
			1.5 V ± 0.1 V	4	
			1.8 V ± 0.15 V	4	
			2.5 V ± 0.2 V	4.1	
			3.3 V ± 0.3 V	4.3	

**PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)**



LOAD CIRCUIT

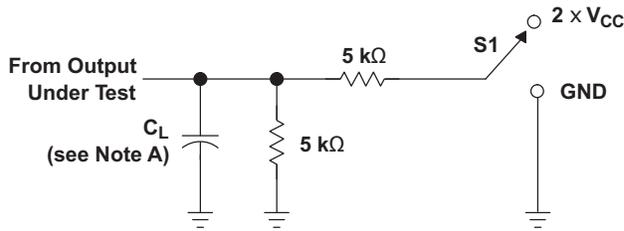
	$V_{CC} = 0.8\text{ V}$	$V_{CC} = 1.2\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, for propagation delays $t_r/t_f = 3\text{ ns}$, for setup and hold times and pulse width $t_r/t_f = 1.2\text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLH} and t_{PHL} are the same as t_{pd} .
- F. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

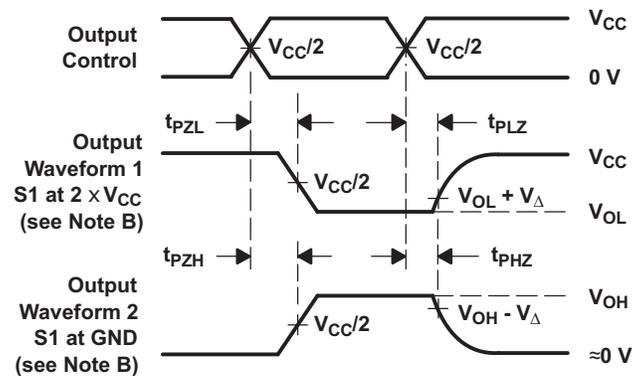
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PLH} and t_{PHL} are the same as t_{pd} .
- G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AUP2G17DCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(HL5, HLF)
SN74AUP2G17DCKR.B	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HL5, HLF)
SN74AUP2G17DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17DRYRG4	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HL
SN74AUP2G17YFPR	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H7N
SN74AUP2G17YFPR.B	Active	Production	DSBGA (YFP) 6	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	H7N

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP2G17DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP2G17DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G17DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP2G17DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP2G17YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP2G17DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP2G17DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G17DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP2G17DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP2G17YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0

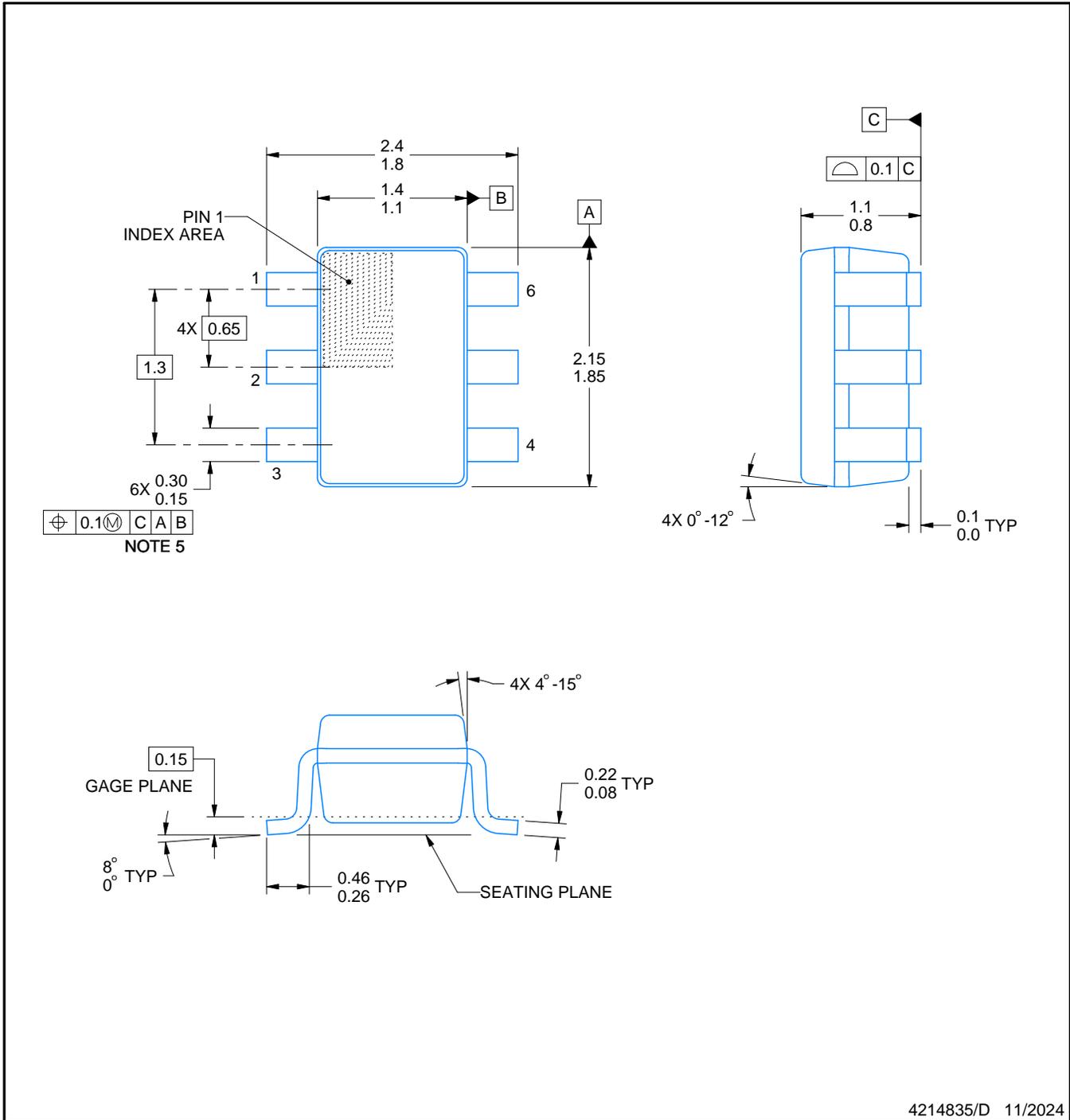
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

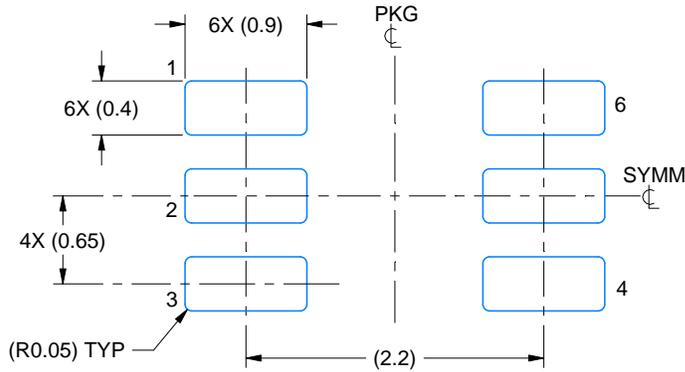
SMALL OUTLINE TRANSISTOR



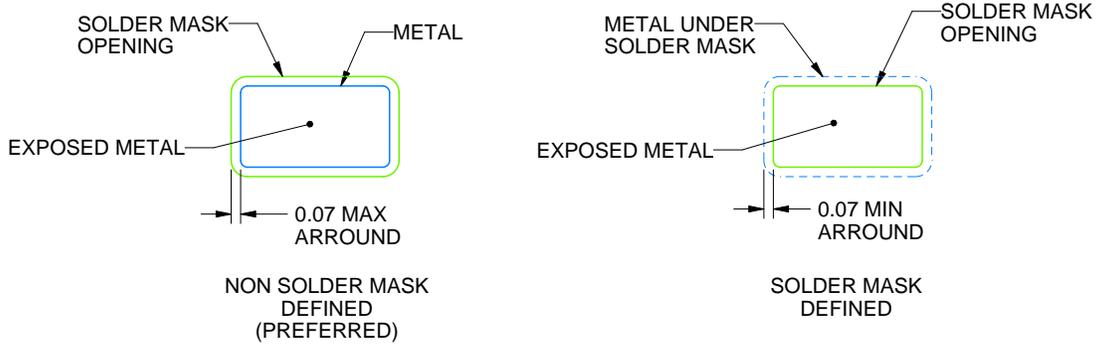
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

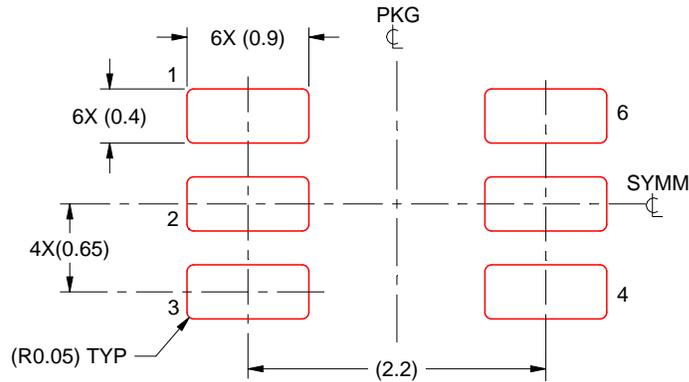


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

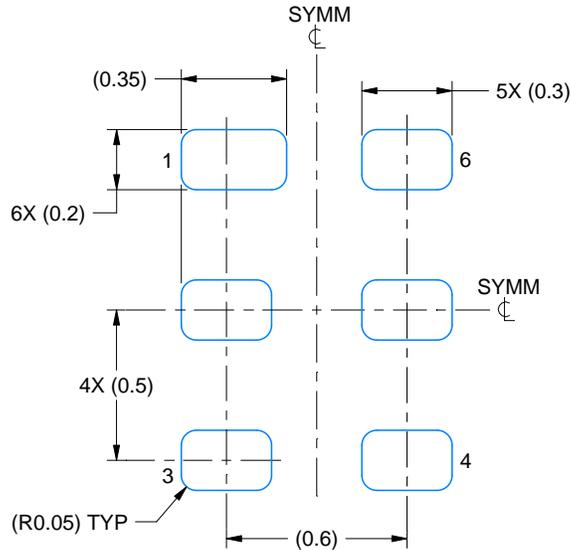
4207181/G

EXAMPLE BOARD LAYOUT

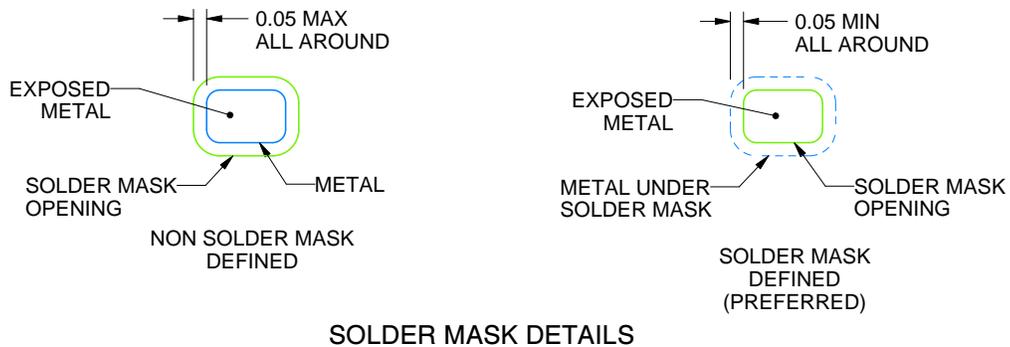
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

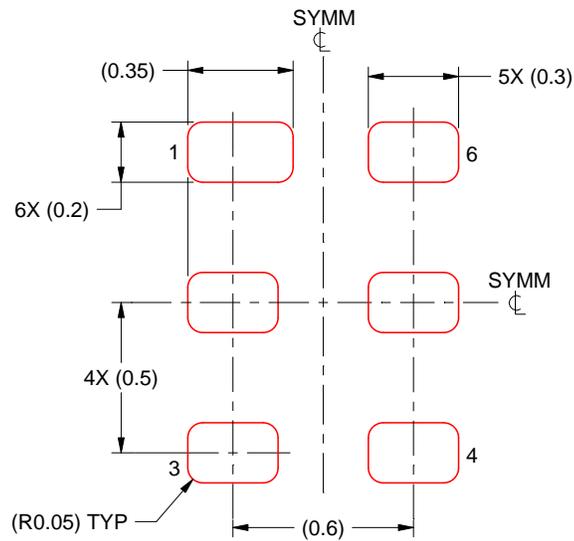
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

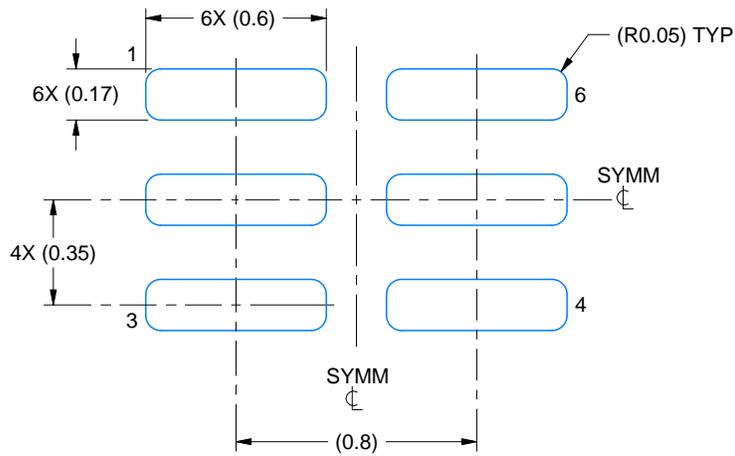
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

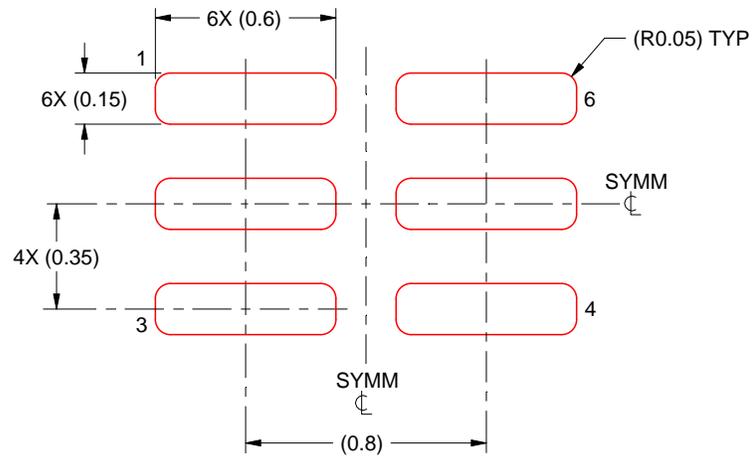
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



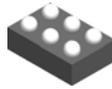
SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

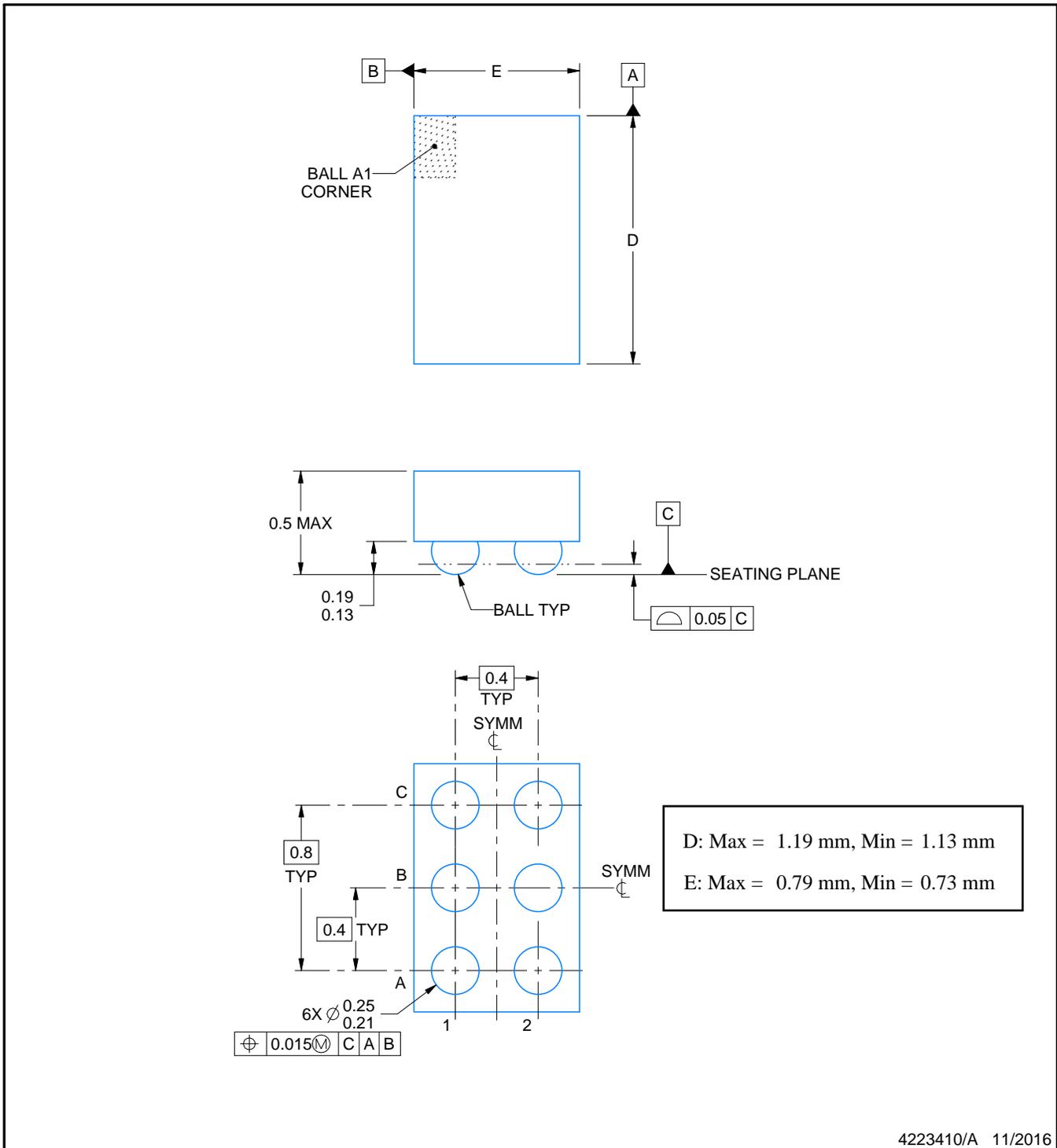
YFP0006



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

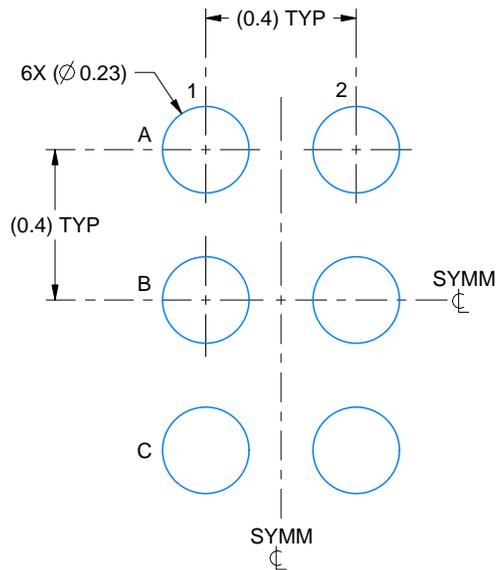
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

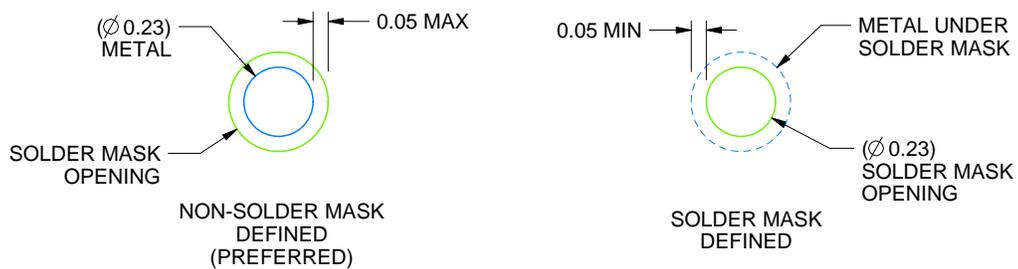
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

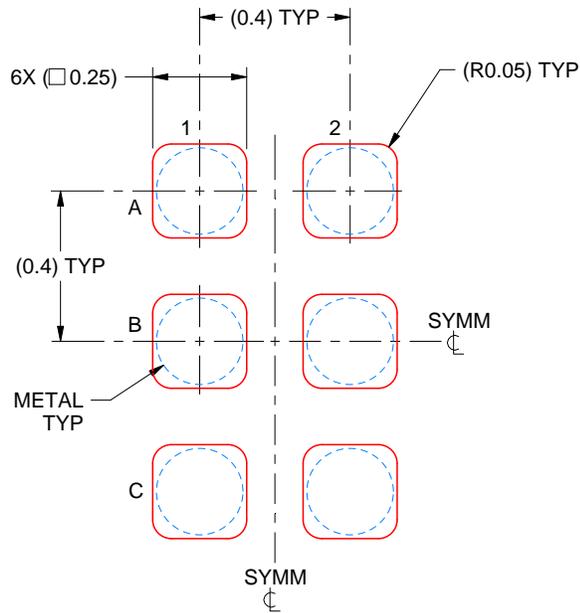
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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