

# SN74CB3Q3125 Quadruple FET Bus Switch

## 2.5V/3.3V Low-Voltage, High-Bandwidth Bus Switch

### 1 Features

- High-bandwidth data path (up to 500MHz)
- 5V tolerant I/Os with device powered up or powered down
- Low and flat ON-state resistance ( $r_{on}$ ) characteristics over operating range ( $r_{on} = 3\Omega$  typical)
- Rail-to-rail switching on data I/O ports
  - 0V to 5V switching with 3.3V  $V_{CC}$
  - 0V to 3.3V switching with 2.5V  $V_{CC}$
- Bidirectional data flow with near-zero propagation delay
- Low input and output capacitance minimizes loading and signal distortion ( $C_{io(OFF)} = 4pF$  typical)
- Fast switching frequency ( $f_{OE} = 20MHz$  maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption ( $I_{CC} = 0.3mA$  typical)
- $V_{CC}$  operating range from 2.3V to 3.6V
- Data I/Os support 0V to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, and 5V)
- Control inputs can be driven by TTL, 5V, or 3.3V CMOS outputs
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000V Human-Body Model (A114-B, Class II)
  - 1000V Charged-Device Model (C101)
- Supports both digital and analog applications: USB interface, differential signal interface, bus isolation, low-distortion signal gating.
- For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application note [CBT-C](#), [CB3T](#), and [CB3Q Signal-Switch Families](#).

### 2 Applications

- IP phones: wired and wireless
- Optical modules
- Optical networking: video over fiber and EPON
- Private branch exchange (PBX)
- WiMAX and wireless infrastructure equipment

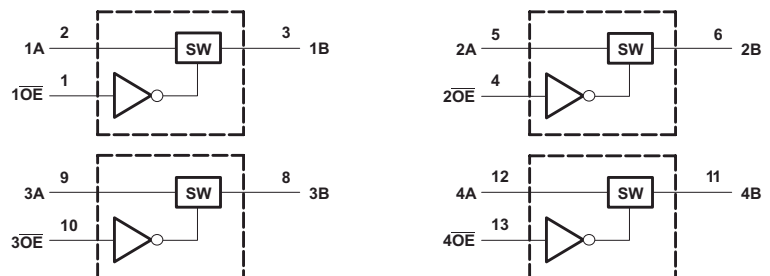
### 3 Description

The SN74CB3Q3125 device is a high-bandwidth FET bus switch that uses a charge pump to elevate the gate voltage of the pass transistor, thus providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The SN74CB3Q3125 device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus.

#### Package Information

| PART NUMBER  | PACKAGE <sup>(1)</sup> | BODY SIZE (NOM) |
|--------------|------------------------|-----------------|
| SN74CB3Q3125 | RGY (VQFN, 14)         | 3.50mm × 3.50mm |
|              | DBQ (SSOP, 16)         | 4.90mm × 3.90mm |
|              | PW (TSSOP, 14)         | 5.00mm × 4.40mm |
|              | DGV (TVSOP, 14)        | 4.40mm × 3.60mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Pin numbers shown are for the DGV, PW, and RGY packages.

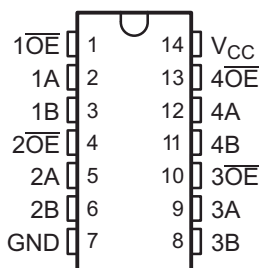
#### Logic Diagram (Positive Logic)



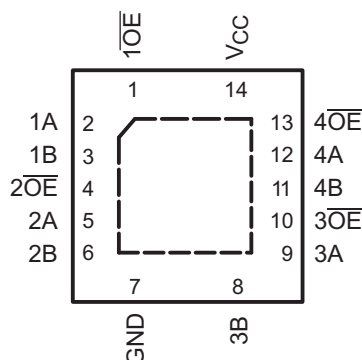
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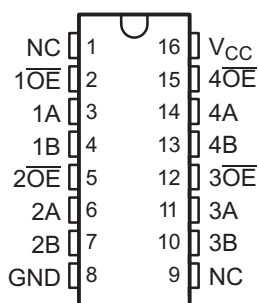
## 4 Pin Configuration and Functions



**Figure 4-1. DGV or PW Package, 14-Pin TVSOP or TSSOP (Top View)**



**Figure 4-2. RGY Package, 14-Pin VQFN (Top View)**



NC - No internal connection

**Figure 4-3. DBQ Package, 16-Pin SSOP (Top View)**

**Table 4-1. Pin Functions**

| PIN             |              |      | TYPE <sup>(1)</sup> | DESCRIPTION                |
|-----------------|--------------|------|---------------------|----------------------------|
| NAME            | DGV, PW, RGY | DBQ  |                     |                            |
| 1 OE            | 1            | 2    | I                   | Output Enable (Active Low) |
| 1A              | 2            | 3    | I/O                 | Channel 1A I/O 1A          |
| 1B              | 3            | 4    | I/O                 | Channel 1B I/O 1B          |
| 2 OE            | 4            | 5    | I                   | Output Enable (Active Low) |
| 2A              | 5            | 6    | I/O                 | Channel 2A I/O 2A          |
| 2B              | 6            | 7    | I/O                 | Channel 2B I/O 2B          |
| GND             | 7            | 8    | —                   | Ground                     |
| 3B              | 8            | 10   | I/O                 | Channel 3B I/O 3B          |
| 3A              | 9            | 11   | I/O                 | Channel 3A I/O 3B          |
| 3 OE            | 10           | 12   | I                   | Output Enable (Active Low) |
| 4B              | 11           | 13   | I/O                 | Channel 4B I/O 4B          |
| 4A              | 12           | 14   | I/O                 | Channel 4A I/O 4B          |
| 4 OE            | 13           | 15   | I                   | Output Enable (Active Low) |
| NC              | —            | 1, 9 | —                   | No Connect                 |
| V <sub>CC</sub> | 14           | 16   | —                   | Power                      |

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                   |                                                                 |                      | MIN  | MAX | UNIT |
|-------------------|-----------------------------------------------------------------|----------------------|------|-----|------|
| V <sub>CC</sub>   | Supply voltage                                                  |                      | −0.5 | 4.6 | V    |
| V <sub>IN</sub>   | Control input voltage <sup>(2)</sup> <sup>(3)</sup>             |                      | −0.5 | 7   | V    |
| V <sub>I/O</sub>  | Switch I/O voltage <sup>(2)</sup> <sup>(3)</sup> <sup>(4)</sup> |                      | −0.5 | 7   | V    |
| I <sub>I/K</sub>  | Control input clamp current                                     | V <sub>IN</sub> < 0  | −50  |     | mA   |
| I <sub>I/OK</sub> | I/O port clamp current                                          | V <sub>I/O</sub> < 0 | −50  |     | mA   |
| I <sub>IO</sub>   | ON-state switch current <sup>(5)</sup>                          |                      | ±64  |     | mA   |
|                   | Continuous current through V <sub>CC</sub> or GND               |                      | ±100 |     | mA   |
| T <sub>J</sub>    | Junction temperature                                            |                      | 150  |     | °C   |
| T <sub>stg</sub>  | Storage temperature                                             |                      | −65  | 150 |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.

### 5.2 ESD Ratings

|                    |                         |                                                                                | VALUE | UNIT |
|--------------------|-------------------------|--------------------------------------------------------------------------------|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | +2000 | V    |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | +1000 |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |                                  |                                | MIN | MAX | UNIT |
|------------------|----------------------------------|--------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                   |                                | 2.3 | 3.6 | V    |
| V <sub>IH</sub>  | High-level control input voltage | V <sub>CC</sub> = 2.3V to 2.7V | 1.7 | 5.5 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7V to 3.6V | 2   | 5.5 |      |
| V <sub>IL</sub>  | Low-level control input voltage  | V <sub>CC</sub> = 2.3V to 2.7V | 0   | 0.7 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7V to 3.6V | 0   | 0.8 |      |
| V <sub>I/O</sub> | Data input and output voltage    |                                | 0   | 5.5 | V    |
| T <sub>A</sub>   | Operating free-air temperature   |                                | −40 | 85  | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup>                           | SN74CB3Q3257 |             |            |            | UNIT |
|---------------------------------------------------------|--------------|-------------|------------|------------|------|
|                                                         | DBQ (SSOP)   | DGV (TVSOP) | PW (TSSOP) | RGY (VQFN) |      |
|                                                         | 16 PINS      | 14 PINS     | 14 PINS    | 14 PINS    |      |
| R <sub>θJA</sub> Junction-to-ambient thermal resistance | 90           | 127         | 113        | 47         | °C/W |

(1) For more information about traditional and new thermal metrics, see the application note, [Semiconductor and IC Package Thermal Metrics](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                         | TEST CONDITIONS                                                      |                                                                                                            | MIN | TYP <sup>(2)</sup> | MAX  | UNIT       |
|---------------------------------------------------|----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----|--------------------|------|------------|
| V <sub>IK</sub>                                   | V <sub>CC</sub> = 3.6V,                                              | I <sub>I</sub> = –18mA                                                                                     |     |                    | –1.8 | V          |
| I <sub>IN</sub> Control inputs                    | V <sub>CC</sub> = 3.6V,                                              | V <sub>IN</sub> = 0 to 5.5V                                                                                |     |                    | ±1   | μA         |
| I <sub>OZ</sub> <sup>(3)</sup>                    | V <sub>CC</sub> = 3.6V,                                              | V <sub>O</sub> = 0 to 5.5V,<br>V <sub>I</sub> = 0, Switch OFF,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND |     |                    | ±1   | μA         |
| I <sub>off</sub>                                  | V <sub>CC</sub> = 0,                                                 | V <sub>O</sub> = 0 to 5.5V,<br>V <sub>I</sub> = 0                                                          |     |                    | 1    | μA         |
| I <sub>CC</sub>                                   | V <sub>CC</sub> = 3.6V,                                              | I <sub>I/O</sub> = 0,<br>Switch ON or OFF, V <sub>IN</sub> = V <sub>CC</sub> or GND                        |     | 0.3                | 1    | mA         |
| ΔI <sub>CC</sub> <sup>(4)</sup> Control inputs    | V <sub>CC</sub> = 3.6V,                                              | One input at 3V,<br>Other inputs at V <sub>CC</sub> or GND                                                 |     |                    | 30   | μA         |
| I <sub>CCD</sub> <sup>(5)</sup> Per control input | V <sub>CC</sub> = 3.6V,<br>Control input switching at 50% duty cycle | A and B ports open,                                                                                        |     | 0.04               | 0.2  | mA/<br>MHz |
| C <sub>in</sub> Control inputs                    | V <sub>CC</sub> = 3.3V,                                              | V <sub>IN</sub> = 5.5V, 3.3V, or 0                                                                         |     | 2.5                | 3.5  | pF         |
| C <sub>io(OFF)</sub>                              | V <sub>CC</sub> = 3.3V,                                              | Switch OFF,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5V, 3.3V, or 0               |     | 4                  | 5    | pF         |
| C <sub>io(ON)</sub>                               | V <sub>CC</sub> = 3.3V,                                              | Switch ON,<br>V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>I/O</sub> = 5.5V, 3.3V, or 0                |     | 8                  | 10   | pF         |
| r <sub>on</sub> <sup>(6)</sup>                    | V <sub>CC</sub> = 2.3V,<br>TYP at V <sub>CC</sub> = 2.5V             | V <sub>I</sub> = 0, I <sub>O</sub> = 30mA                                                                  |     | 4                  | 8    | Ω          |
|                                                   |                                                                      | V <sub>I</sub> = 1.7V, I <sub>O</sub> = –15mA                                                              |     | 4                  | 9    |            |
|                                                   | V <sub>CC</sub> = 3V                                                 | V <sub>I</sub> = 0, I <sub>O</sub> = 30mA                                                                  |     | 4                  | 6    |            |
|                                                   |                                                                      | V <sub>I</sub> = 2.4V, I <sub>O</sub> = –15mA                                                              |     | 4                  | 8    |            |

(1) V<sub>IN</sub> and I<sub>IN</sub> refer to control inputs. V<sub>I</sub>, V<sub>O</sub>, I<sub>I</sub>, and I<sub>O</sub> refer to data pins.

(2) All typical values are at V<sub>CC</sub> = 3.3V (unless otherwise noted), T<sub>A</sub> = 25°C.

(3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.

(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 5-2](#)).

(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

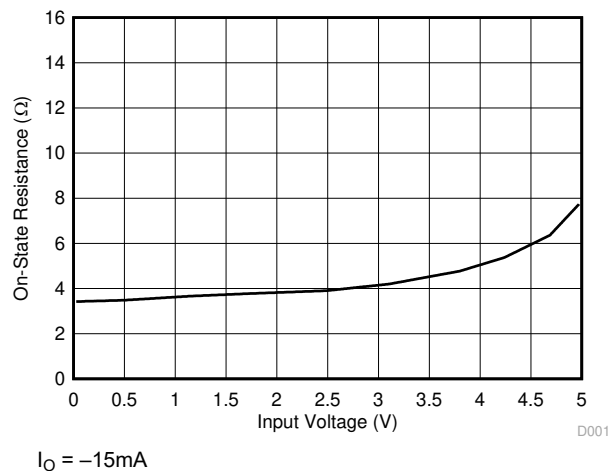
| PARAMETER      | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.5V \pm 0.2V$ |      | $V_{CC} = 3.3V \pm 0.3V$ |     | UNIT |
|----------------|-----------------|----------------|--------------------------|------|--------------------------|-----|------|
|                |                 |                | MIN                      | MAX  | MIN                      | MAX |      |
| $f_{OE}^{(1)}$ | $\overline{OE}$ | A or B         |                          | 10   |                          | 20  | MHz  |
| $t_{pd}^{(2)}$ | A or B          | B or A         |                          | 0.12 |                          | 0.2 | ns   |
| $t_{en}$       | $\overline{OE}$ | A or B         | 1.5                      | 6.7  | 1.5                      | 6.6 | ns   |
| $t_{dis}$      | $\overline{OE}$ | A or B         | 1                        | 4.6  | 1                        | 5.3 | ns   |

(1) Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5V$ ,  $R_L \geq 1M\Omega$ ,  $C_L = 0$ ).

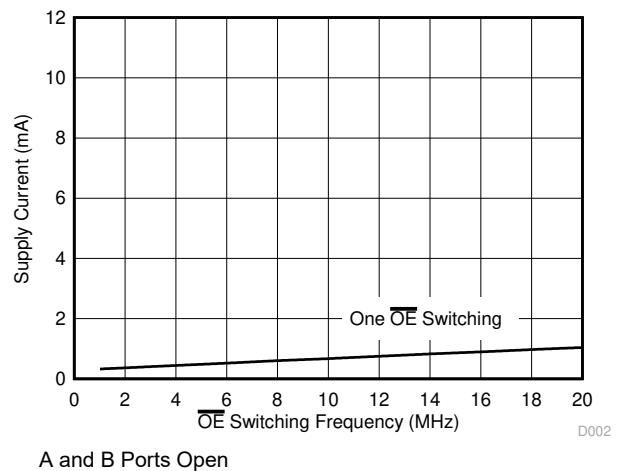
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## 5.7 Typical Characteristics

At  $T_A = 25^\circ C$  and  $V_{CC} = 3.3V$ , unless otherwise noted.

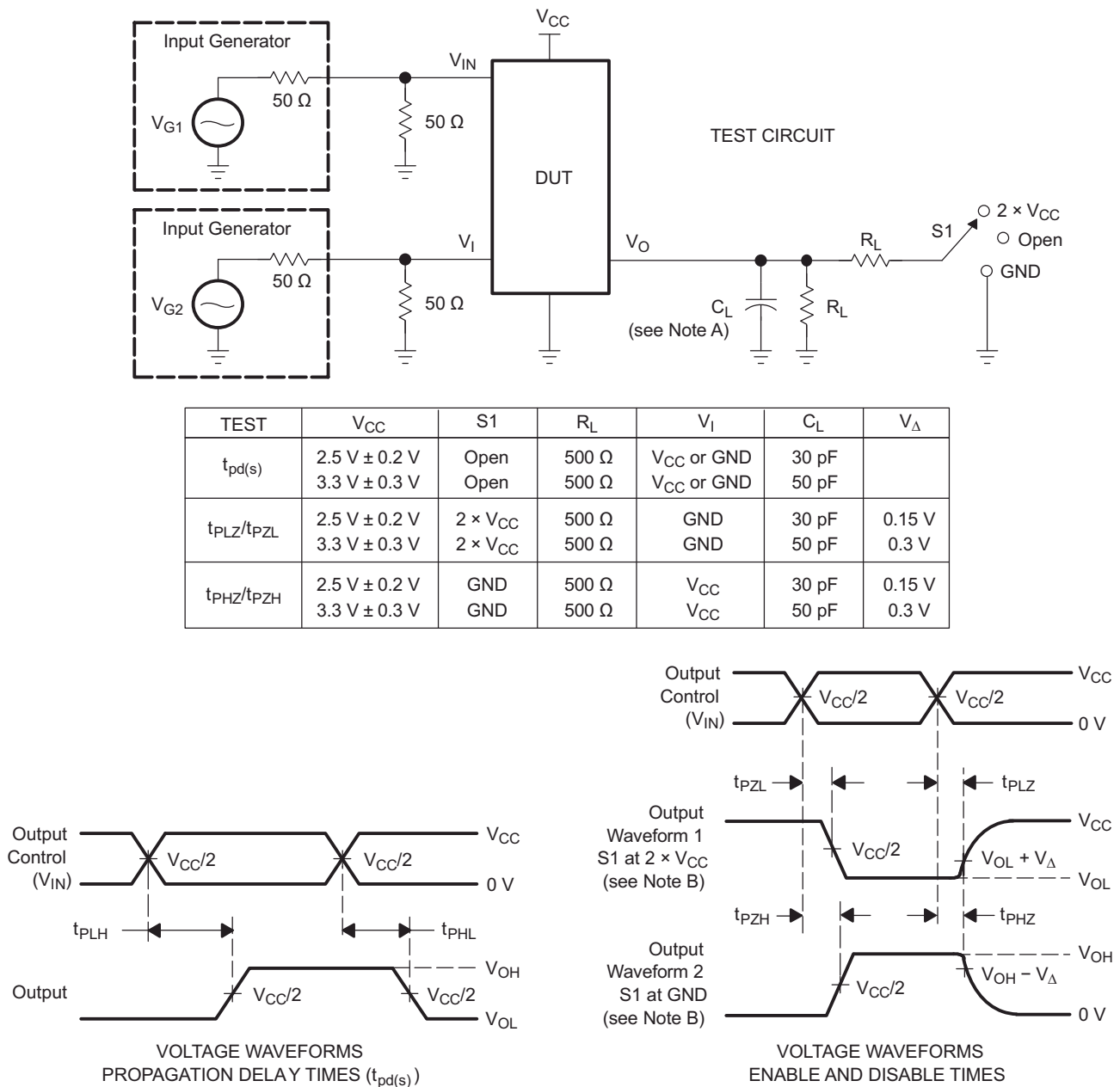


**Figure 5-1. Typical On-State Resistance vs Input Voltage**



**Figure 5-2. Typical Supply Current vs  $\overline{OE}$  Switching Frequency**

## 6 Parameter Measurement Information



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z<sub>O</sub> = 50Ω, t<sub>r</sub> ≤ 2.5ns, t<sub>f</sub> ≤ 2.5ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd(s)</sub>. The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. Test Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SN74CB3Q3125 device is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The SN74CB3Q3125 device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3125 device provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3125 device is organized as four 1-bit bus switches with separate output-enable ( $1 \overline{OE}$ ,  $2 \overline{OE}$ ,  $3 \overline{OE}$ ,  $4 \overline{OE}$ ) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

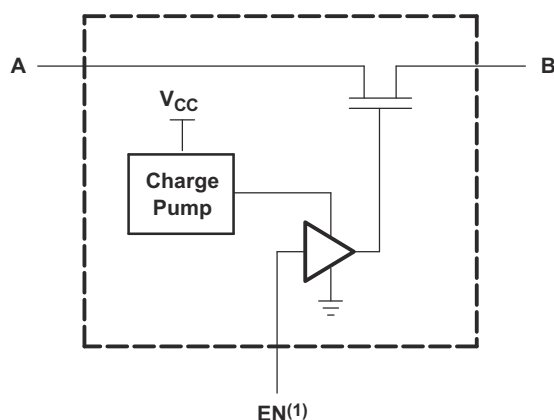
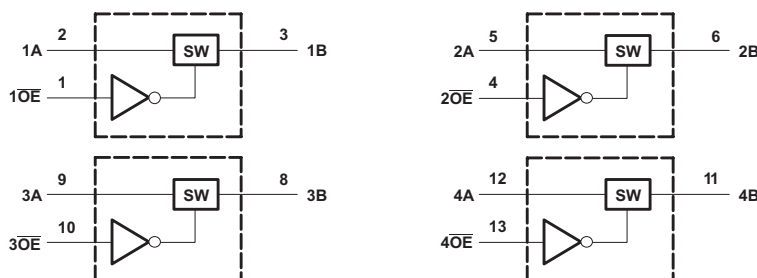


Figure 7-1. Simplified Schematic, Each FET Switch (SW)

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The SN74CB3Q3125 device has a high-bandwidth data path (up to 500MHz) and has 5V tolerant I/Os with the device powered up or powered down. It also has low and flat ON-state resistance ( $r_{on}$ ) characteristics over operating range ( $r_{on} = 4\Omega$  Typ).

The SN74CB3Q3125 device has rail-to-rail switching on data I/O ports for 0V to 5V switching with 3.3V  $V_{CC}$  and 0V to 3.3V switching with 2.5V  $V_{CC}$  as well as bidirectional data flow with near-zero propagation delay and low input/output capacitance that minimizes loading and signal distortion ( $C_{io(OFF)} = 3.5pF$  Typ).

The SN74CB3Q3125 device also provides a fast switching frequency ( $f_{OE} = 20MHz$  Max) with data and control inputs that provide undershoot clamp diodes as well as low power consumption ( $I_{CC} = 0.6mA$  Typ).

The  $V_{CC}$  operating range is from 2.3 V to 3.6 V and the data I/Os support 0V to 5V signal levels of (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V).

The control inputs can be driven by TTL or 5V or 3.3V CMOS outputs, and  $I_{off}$  supports partial-power-down mode operation.

### 7.4 Device Functional Modes

[Table 7-1](#) lists the functional modes for the SN74CB3Q3125 device.

**Table 7-1. Function Table**

| INPUT<br>OE | INPUT/OUTPUT<br>A | FUNCTION        |
|-------------|-------------------|-----------------|
| L           | B                 | A port = B port |
| H           | Z                 | Disconnect      |

## 8 Application and Implementation

### Note

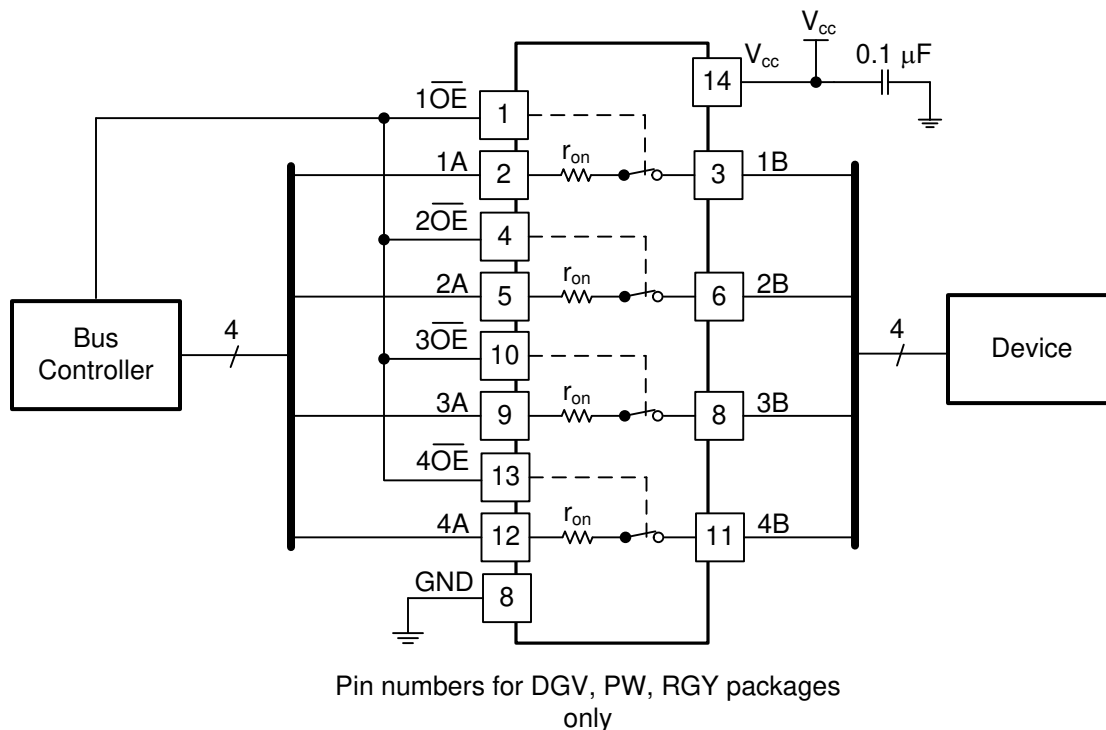
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74CB3Q3125 device can be used to control up to four channels simultaneously.

### 8.2 Typical Application

The application shown in Figure 8-1 is a 4-bit bus being controlled. The  $\overline{OE}$  pins are used to control the chip from the bus controller. This is a very generic example and can apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.



**Figure 8-1. Typical Application of the SN74CB3Q3257**

#### 8.2.1 Design Requirements

The 0.1-μF capacitor must be placed as close as possible to the SN74CB3Q3257 device.

### 8.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in [Section 5.3](#)
  - Inputs and outputs are overvoltage tolerant, which allows them to go as high as 5.5V at any valid  $V_{CC}$
2. Recommended output conditions:
  - Load currents must not exceed  $\pm 64\text{mA}$  per channel
3. Frequency selection criterion:
  - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in [Section 10](#)

### 8.2.3 Application Curve

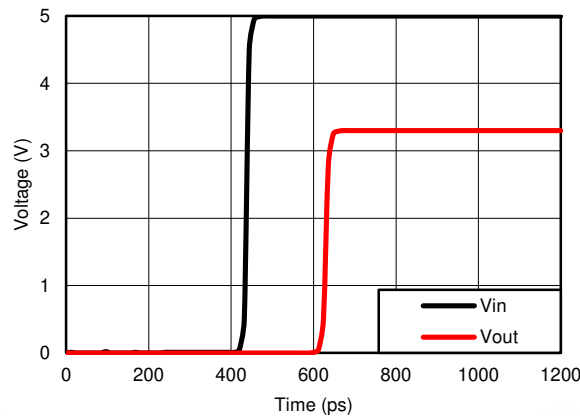


Figure 8-2. Propagation Delay ( $t_{pd}$ ) Simulation Result at  $V_{CC} = 3.3\text{V}$

## 9 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Section 5.1](#) table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  bypass capacitor is recommended. If multiple pins are labeled  $V_{CC}$ , then a 0.01- $\mu\text{F}$  or 0.022- $\mu\text{F}$  capacitor is recommended for each  $V_{CC}$  because the  $V_{CC}$  pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example  $V_{CC}$  and  $V_{DD}$ , a 0.1- $\mu\text{F}$  bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

## 10 Layout

### 10.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace, which results in the reflection. Not all PCB traces can be straight; therefore, some traces must turn corners. [Figure 10-1](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

## 10.2 Layout Example

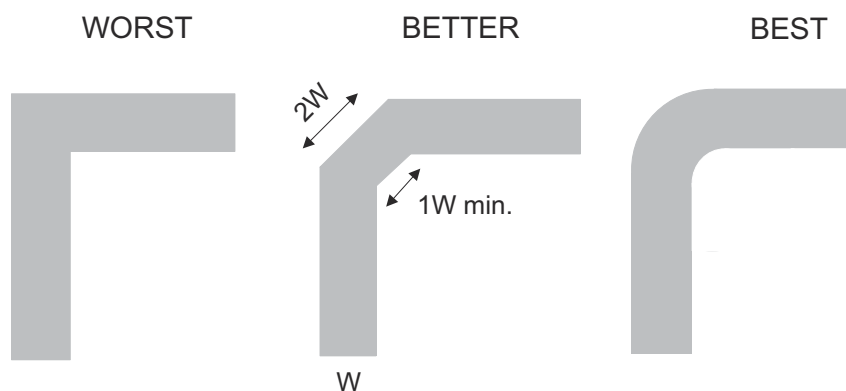


Figure 10-1. Trace Example

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)
- Texas Instruments, [Selecting the Right Texas Instruments Signal Switch](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.4 Trademarks

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### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision C (June 2015) to Revision D (January 2026)</b> | <b>Page</b> |
|-------------------------------------------------------------------------|-------------|
| • Updated Package Information table.....                                | 1           |

| <b>Changes from Revision B (March 2005) to Revision C (June 2015)</b>                                                                                                                                                                                                                                                                                                             | <b>Page</b> |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| • Added <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1           |
| • Deleted <i>Ordering Information</i> table.....                                                                                                                                                                                                                                                                                                                                  | 1           |

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74CB3Q3125DBQR</a> | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125DBQR.A               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125DBQR.B               | Active        | Production           | SSOP (DBQ)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| <a href="#">SN74CB3Q3125DGVR</a> | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| SN74CB3Q3125DGVR.B               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| SN74CB3Q3125DGVRG4               | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| SN74CB3Q3125DGVRG4.B             | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| <a href="#">SN74CB3Q3125PW</a>   | Obsolete      | Production           | TSSOP (PW)   14  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | BU125               |
| <a href="#">SN74CB3Q3125PWR</a>  | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| SN74CB3Q3125PWR.A                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| SN74CB3Q3125PWR.B                | Active        | Production           | TSSOP (PW)   14  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU125               |
| <a href="#">SN74CB3Q3125RGYR</a> | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125RGYR.A               | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125RGYR.B               | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125RGYRG4               | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125RGYRG4.A             | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |
| SN74CB3Q3125RGYRG4.B             | Active        | Production           | VQFN (RGY)   14  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU125               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CB3Q3125DBQR   | SSOP         | DBQ             | 16   | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3125DGVR   | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3125DGVRG4 | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3125PWR    | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3125RGYR   | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| SN74CB3Q3125RGYRG4 | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CB3Q3125DBQR   | SSOP         | DBQ             | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3125DGVR   | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3125DGVRG4 | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3125PWR    | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3125RGYR   | VQFN         | RGY             | 14   | 3000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3125RGYRG4 | VQFN         | RGY             | 14   | 3000 | 353.0       | 353.0      | 32.0        |

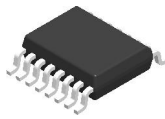
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

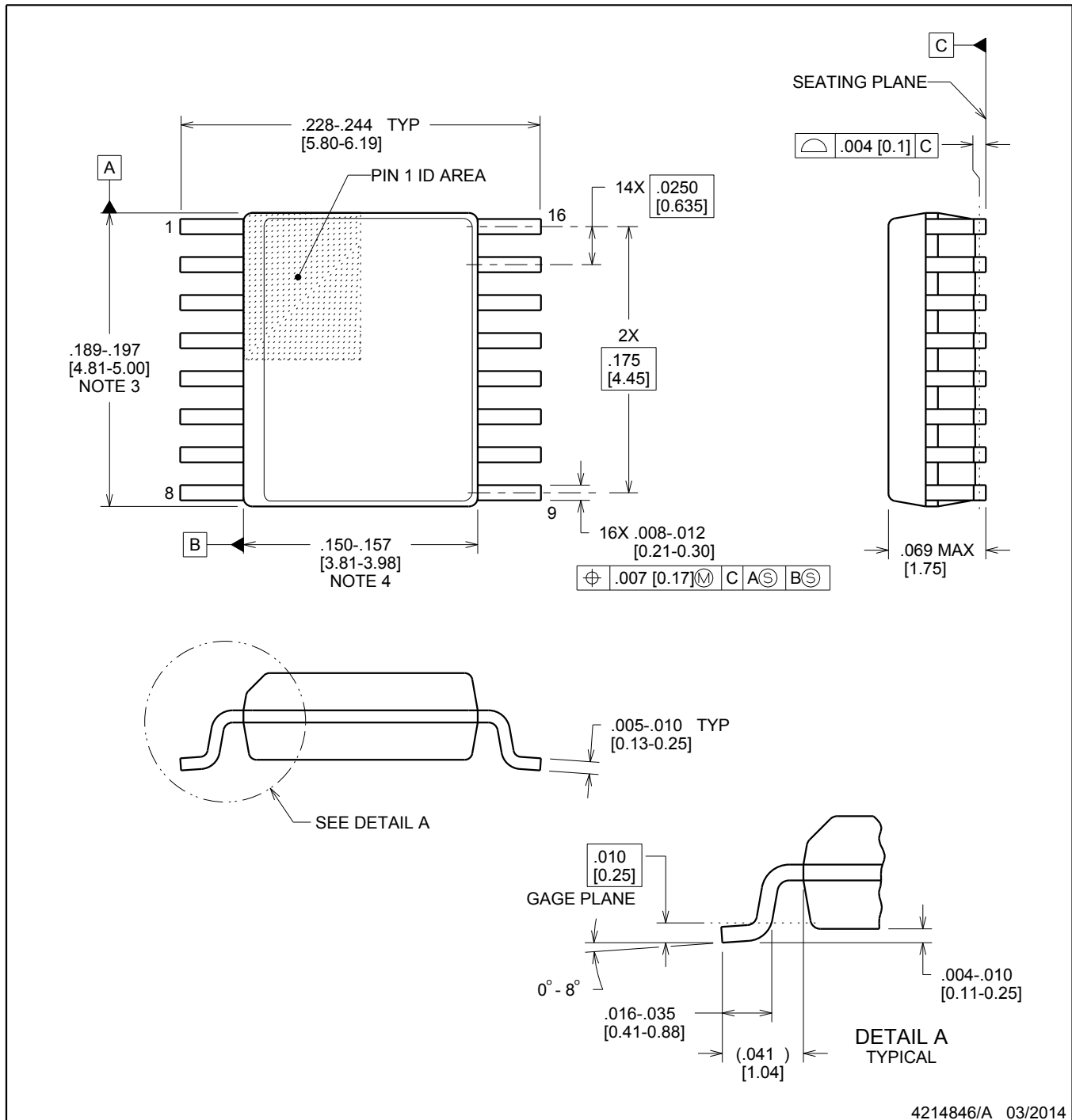


**DBQ0016A**

## PACKAGE OUTLINE

**SSOP - 1.75 mm max height**

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

### NOTES:

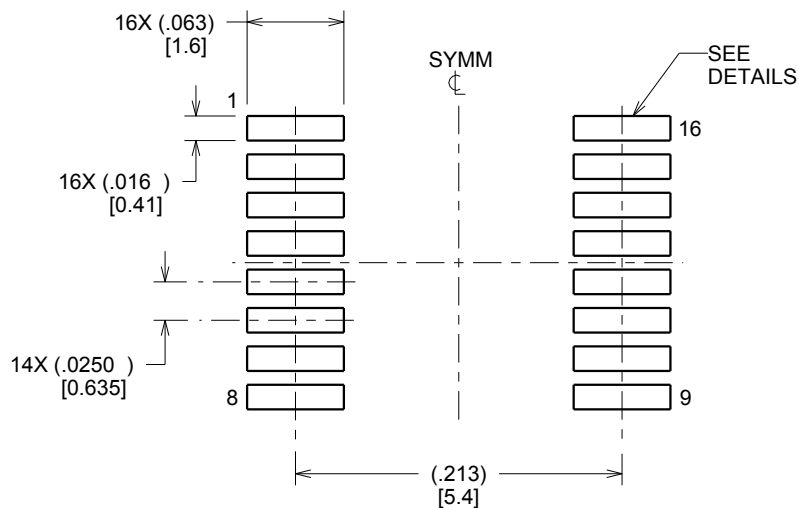
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

# EXAMPLE BOARD LAYOUT

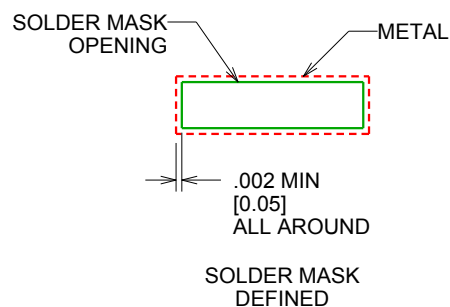
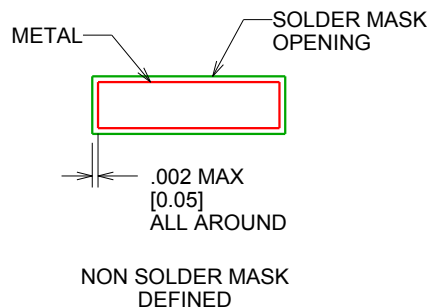
DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

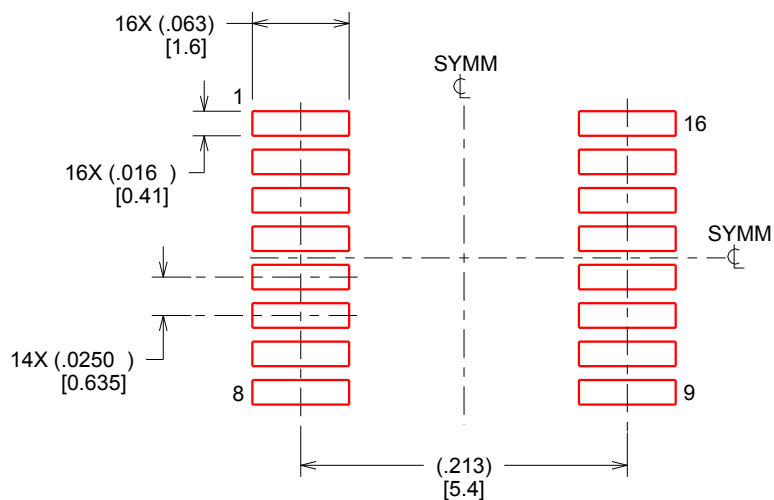
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.127 MM] THICK STENCIL  
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

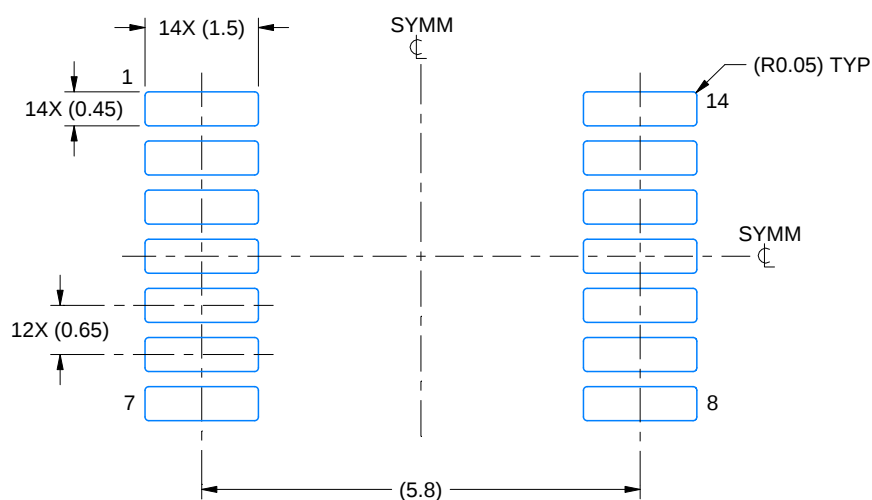
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

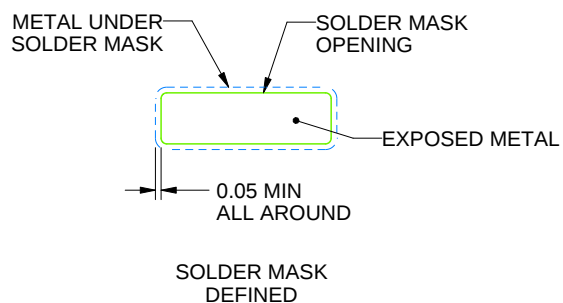
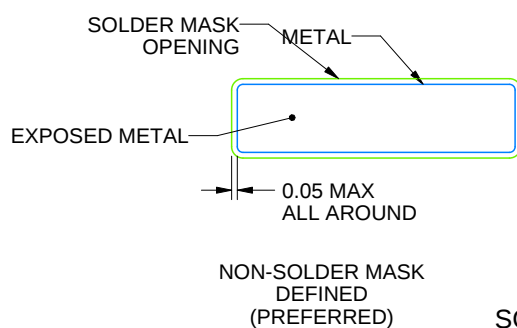
**PW0014A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

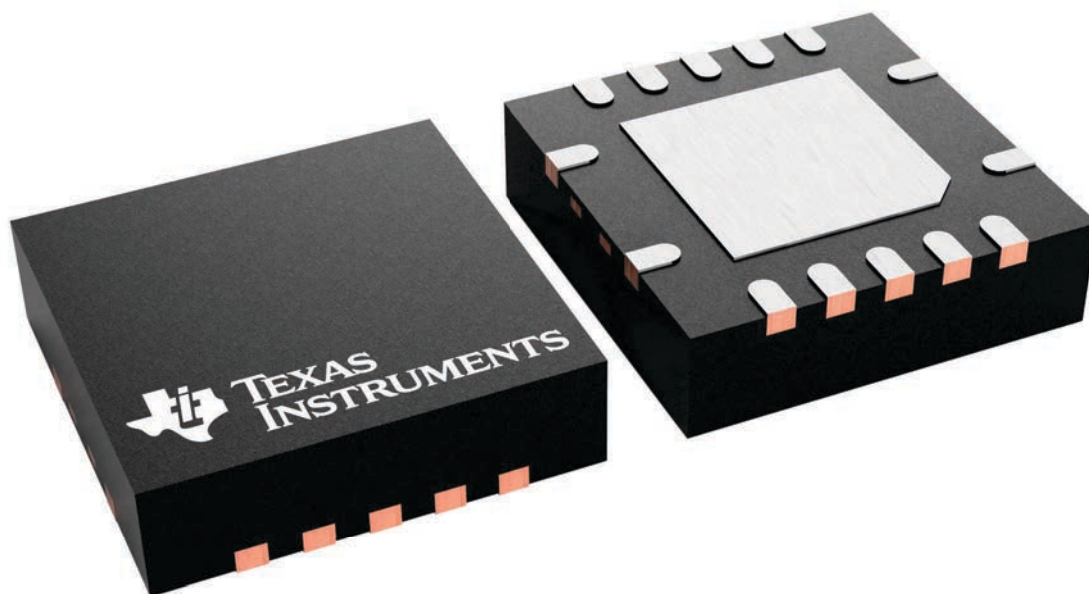
**RGY 14**

**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231541/A

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