

Dual FET Bus Switch 2.5-V/3.3-V Low-Voltage High-Bandwidth Bus Switch

Check for Samples: [SN74CB3Q3306A-EP](#)

FEATURES

- High-Bandwidth Data Path (up to 500 MHz⁽¹⁾)
- 5-V-Tolerant I/Os With Device Powered Up or Powered Down
- Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range ($r_{on} = 4\ \Omega$ Typ)
- Rail-to-Rail Switching on Data I/O Ports
 - 0- to 5-V Switching With 3.3-V V_{CC}
 - 0- to 3.3-V Switching With 2.5-V V_{CC}
- Bidirectional Data Flow With Near-Zero Propagation Delay
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 3.5\text{ pF}$ Typ)
- Fast Switching Frequency ($f_{OE} = 20\text{ MHz}$ Max)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ($I_{CC} = 0.25\text{ mA}$ Typ)
- V_{CC} Operating Range From 2.3 V to 3.6 V
- Data I/Os Support 0- to 5-V Signaling Levels (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation

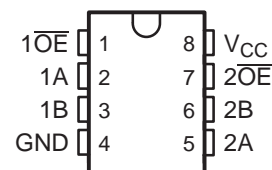
(1) For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number [SCDA008](#).

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Differential Signal Interface, Bus Isolation, Low-Distortion Signal Gating

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C) Temperature Range
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_J	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
-55°C to 125°C	TSSOP – PW	Tube	CCB3Q3306AMPWEP	U306AM	V62/14606-01XE-T
		Tape and reel	CCB3Q3306AMPWREP		V62/14606-01XE

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74CB3Q3306A-EP

SCDS352 – DECEMBER 2013

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The SN74CB3Q3306A is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3306A provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3306A is organized as two 1-bit switches with separate output-enable ($\overline{1OE}$, $\overline{2OE}$) inputs. It can be used as two 1-bit bus switches or as one 2-bit bus switch. When \overline{OE} is low, the associated 1-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 1-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**Table 1. FUNCTION TABLE
(EACH BUS SWITCH)**

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

LOGIC DIAGRAM (POSITIVE LOGIC)

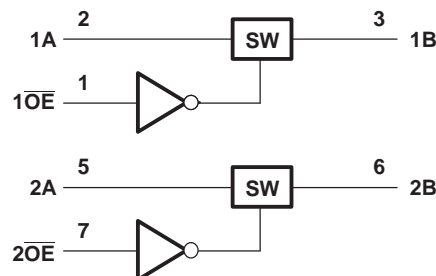
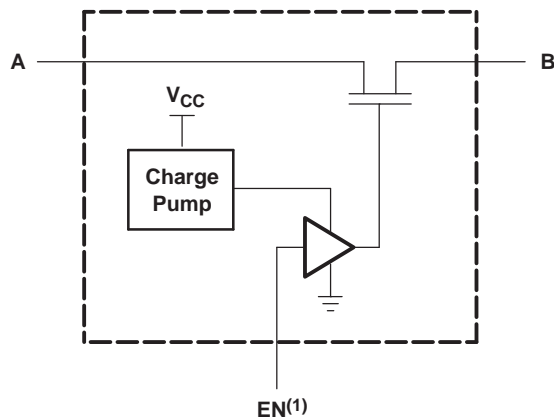


Figure 1. SIMPLIFIED SCHEMATIC, EACH FET SWITCH (SW)



(1) EN is the internal enable signal applied to the switch.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	4.6	V
V _{IN}	Control input voltage range ^{(2) (3)}		−0.5	7	V
V _{I/O}	Switch I/O voltage range ^{(2) (3) (4)}		−0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		−50	mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		−50	mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±64	mA
	Continuous current through each V _{CC} or GND			±100	mA
T _J	Maximum junction temperature			150	°C
T _{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.

(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		SN74CB3Q3306A-EP	UNITS
		PW	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	190.6	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	74	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	119.4	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	12	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	117.7	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	5.5	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	5.5	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	0.8	
V_{IO}	Data input/output voltage		0	5.5	V
T_J	Operating junction temperature		–55	125	°C

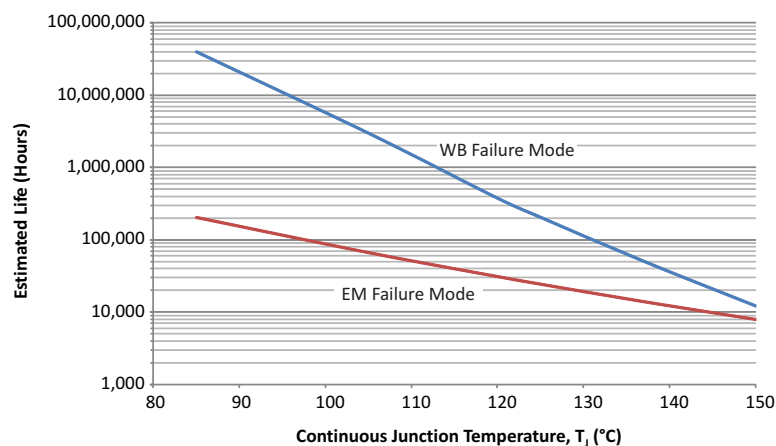
- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS⁽¹⁾

over recommended operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.6\text{ V}$,	$I_I = -18\text{ mA}$				-1.8	V
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_{IN} = 0\text{ to }5.5\text{ V}$				± 1	μA
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$				± 1	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$				1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_{IO} = 0$, Switch ON or OFF, $V_{IN} = V_{CC}$ or GND			0.25	0.7	mA
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V, Other inputs at V_{CC} or GND	$T_J = -55^\circ\text{C to }85^\circ\text{C}$			25	μA
				$T_J = 125^\circ\text{C}$			36	
I_{CCD} ⁽⁵⁾	Per control input	$V_{CC} = 3.6\text{ V}$,	A and B ports open, Control input switching at 50% duty cycle			0.03		mA/MHz
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$,	$V_{IN} = 5.5\text{ V}$, 3.3 V, or 0			2.5		pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$,	Switch OFF, $V_{IN} = V_{CC}$, $V_{IO} = 5.5\text{ V}$, 3.3 V, or 0			3.5		pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$,	Switch ON, $V_{IN} = \text{GND}$, $V_{IO} = 5.5\text{ V}$, 3.3 V, or 0			8		pF
r_{on} ⁽⁶⁾	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		4	8	Ω
				$T_J = 125^\circ\text{C}$			10	
		$V_I = 1.7\text{ V}$,	$I_O = -15\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		5	9	
				$T_J = 125^\circ\text{C}$			58	
	$V_{CC} = 3\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		4	6	
				$T_J = 125^\circ\text{C}$			8	
		$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$	$T_J = -55^\circ\text{C to }85^\circ\text{C}$		5	8	
				$T_J = 125^\circ\text{C}$			66	

- (1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.
- (2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
- (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
- (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- (5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4).
- (6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



- (1) See datasheet for absolute maximum and minimum recommended operating conditions.
- (2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
- (3) Enhanced plastic product disclaimer applies.

Figure 2. SN74CB3Q3306A-EP Operating Life Derating Chart

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range (unless otherwise noted) (see [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}^{(1)}$	\overline{OE}	A or B		10		20	MHz
$t_{pd}^{(2)}$	$T_J = -55^\circ\text{ to }85^\circ\text{C}$	A or B		0.2		0.3	ns
	$T_J = 125^\circ\text{C}$			1.2		2.3	
t_{en}	\overline{OE}	A or B	1.5	12	1.5	10	ns
t_{dis}	\overline{OE}	A or B	1	14	1	9	ns

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5\text{ V}$, $R_L \geq 1\text{ M}\Omega$, $C_L = 0$)

(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

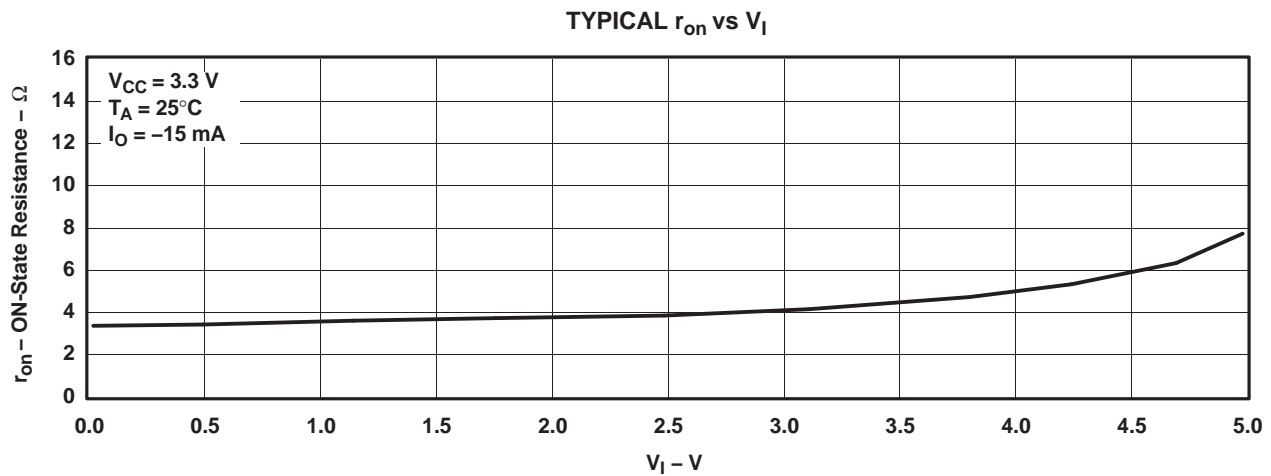


Figure 3. Typical r_{on} vs V_I

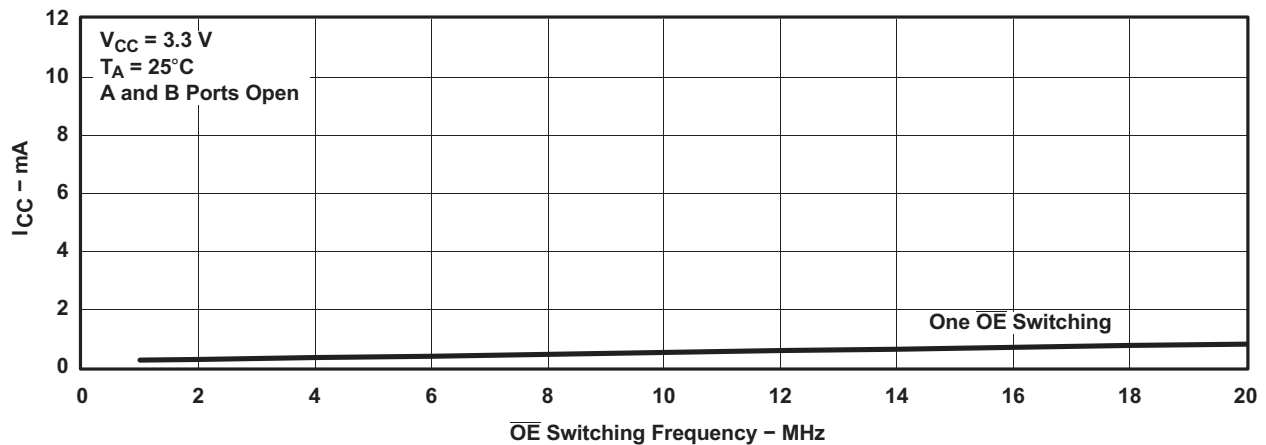
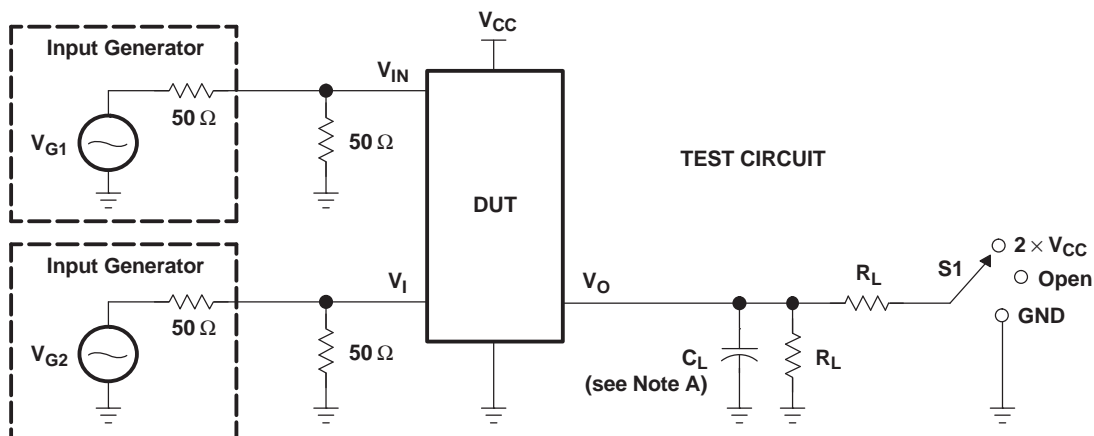
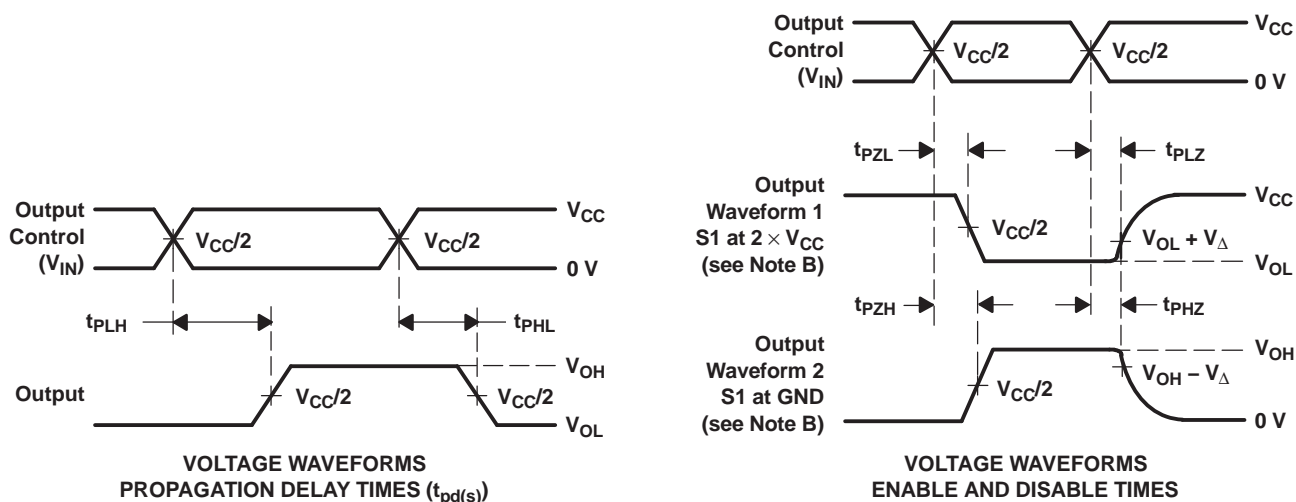


Figure 4. Typical I_{CC} vs \overline{OE} Switching Frequency

PARAMETER MEASUREMENT INFORMATION



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd(s)}	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PZH} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd(s)}. The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CCB3Q3306AMPWEP	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
CCB3Q3306AMPWREP	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
V62/14606-01XE	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM
V62/14606-01XE-T	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	U306AM

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74CB3Q3306A-EP :

- Catalog : [SN74CB3Q3306A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CCB3Q3306AMPWREP	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CCB3Q3306AMPWREP	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

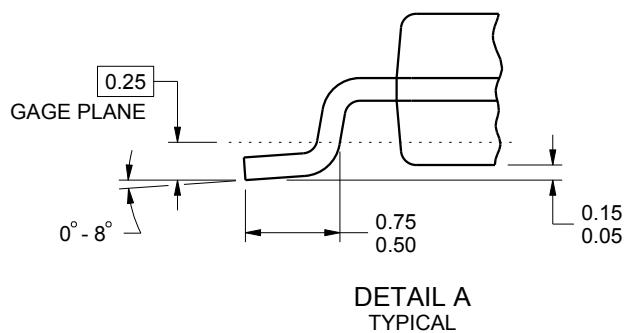
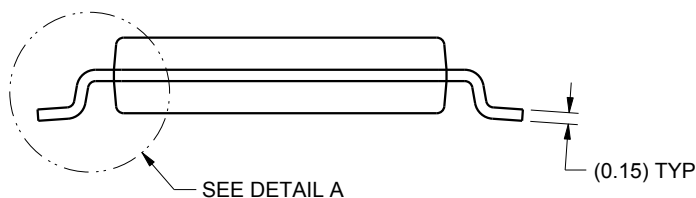
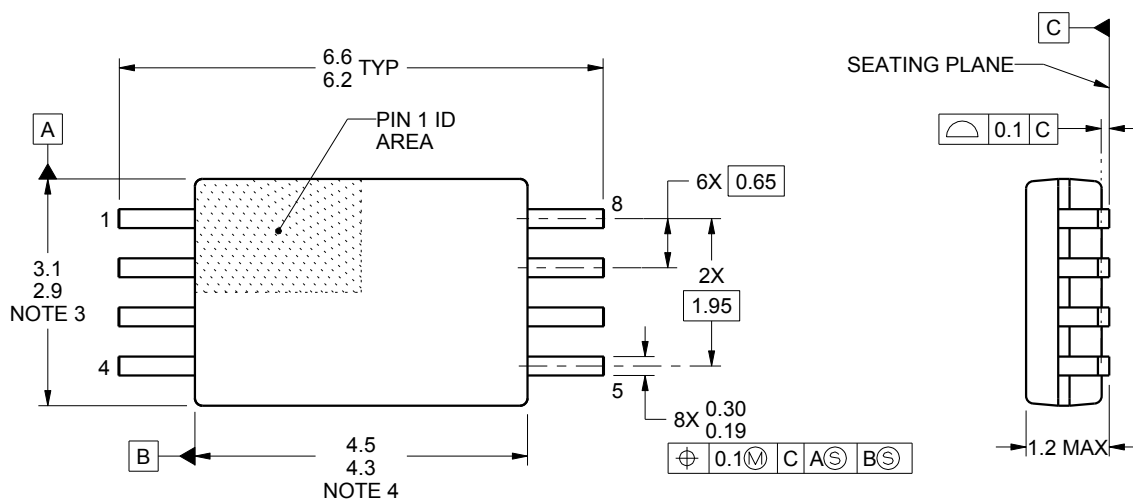
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CCB3Q3306AMPWEP	PW	TSSOP	8	150	530	10.2	3600	3.5
V62/14606-01XE-T	PW	TSSOP	8	150	530	10.2	3600	3.5



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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