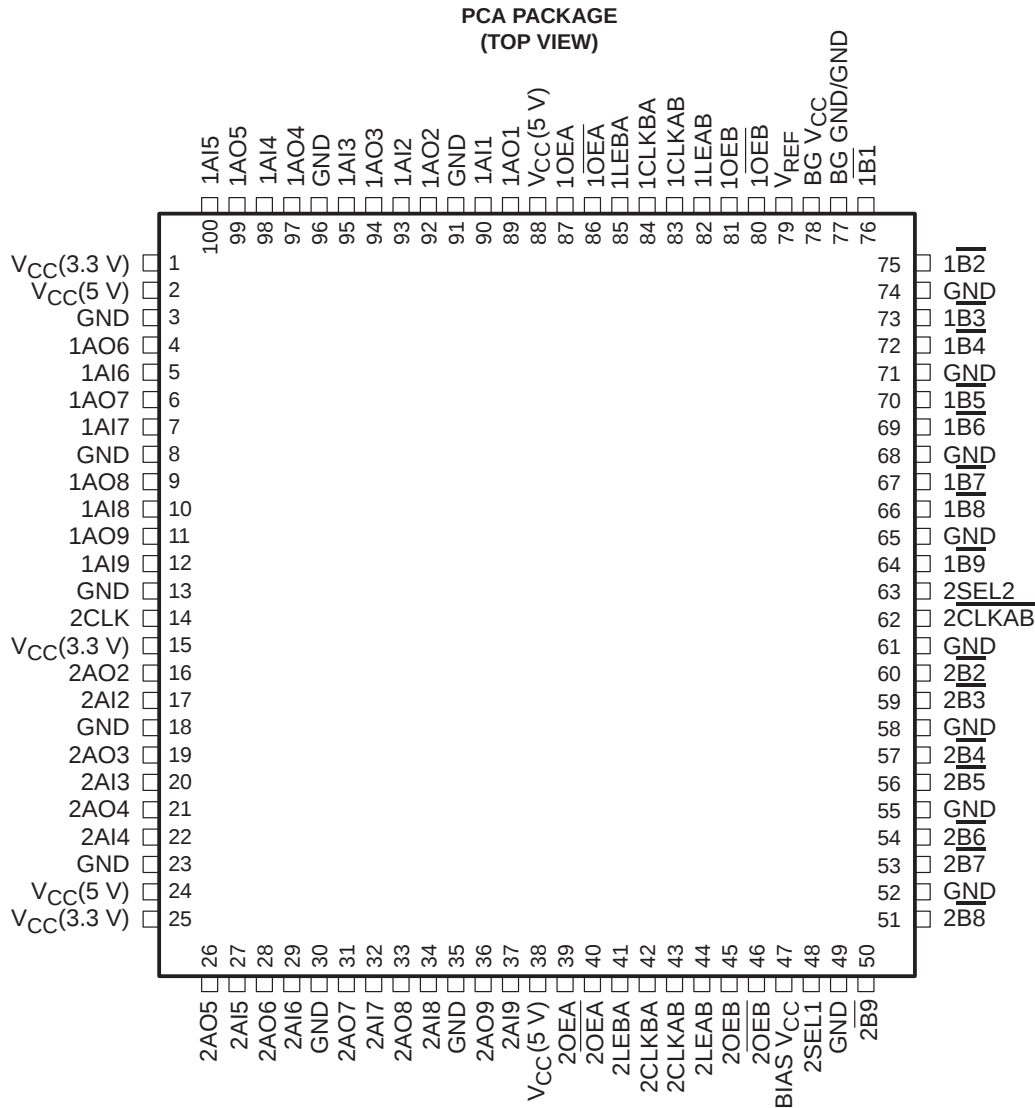


# SN74FB1653

## 17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCIEVER WITH BUFFERED CLOCK LINE

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- Compatible With IEEE Std 1194.1-1991 (BTL)
- LVTTTL A Port, Backplane Transceiver Logic (BTL)  $\bar{B}$  Port
- Open-Collector  $\bar{B}$ -Port Outputs Sink 100 mA
- $\bar{B}$ -Port Biasing Network Preconditions the Connector and PC Trace to the BTL High-Level Voltage
- High-Impedance State During Power Up and Power Down
- Selectable Clock Delay
- TTL-Input Structures Incorporate Active Clamping Networks to Aid in Line Termination
- BIAS  $V_{CC}$  Minimizes Signal Distortion During Live Insertion/Withdrawal



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# SN74FB1653

## 17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER

### WITH BUFFERED CLOCK LINE

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#### description/ordering information

The SN74FB1653 contains an 8-bit and a 9-bit transceiver with a buffered clock. The clock and transceivers are designed to translate signals between LVTTTL and BTL environments. The device is designed specifically to be compatible with IEEE Std 1194.1-1991 (BTL).

The A port operates at LVTTTL signal levels. The A outputs reflect the inverse of the data at the  $\bar{B}$  port when the A-port output enable (OEA) is high. When OEA is low or when  $V_{CC}$ (5 V) typically is less than 2.5 V, the A outputs are in the high-impedance state.

The  $\bar{B}$  port operates at BTL signal levels. The open-collector  $\bar{B}$  ports are specified to sink 100 mA. Two output enables (OEB and  $\overline{OEB}$ ) are provided for the  $\bar{B}$  outputs. When OEB is low,  $\overline{OEB}$  is high, or  $V_{CC}$ (5 V) typically is less than 2.5 V, the  $\bar{B}$  port is turned off.

The clock-select (2SEL1 and 2SEL2) inputs are used to configure the TTL-to-BTL clock paths and delays (refer to the *MUX-MODE DELAY* table).

BIAS  $V_{CC}$  establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when  $V_{CC}$ (5 V) is not connected.

BG  $V_{CC}$  and BG GND are the supply inputs for the bias generator.

$V_{REF}$  is an internally generated voltage source. It is recommended that  $V_{REF}$  be decoupled with an external 0.1- $\mu$ F capacitor.

Enhanced heat-dissipation techniques should be used when operating this device from AI to A0 at frequencies greater than 50 MHz, or from AI to  $\bar{B}$  or  $\bar{B}$  to A0 at frequencies greater than 100 MHz.

#### ORDERING INFORMATION

| $T_A$       | PACKAGE <sup>†</sup> |      | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------------|----------------------|------|-----------------------|------------------|
| 0°C to 70°C | TQFP – PCA           | Tube | SN74FB1653PCA         | FB1653           |

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### Function Tables

##### TRANSCEIVER

| INPUTS           |     |     |                  | FUNCTION                                         |
|------------------|-----|-----|------------------|--------------------------------------------------|
| $\overline{OEA}$ | OEA | OEB | $\overline{OEB}$ |                                                  |
| X                | X   | H   | L                | $\bar{A}$ data to B bus                          |
| L                | H   | X   | X                | $\bar{B}$ data to A bus                          |
| L                | H   | H   | L                | $\bar{A}$ data to B bus, $\bar{B}$ data to A bus |
| X                | X   | L   | X                | B-bus isolation                                  |
| X                | X   | X   | H                |                                                  |
| H                | X   | X   | X                | A-bus isolation                                  |
| X                | L   | X   | X                |                                                  |

##### STORAGE MODE

| INPUTS |     | FUNCTION    |
|--------|-----|-------------|
| LE     | CLK |             |
| H      | X   | Transparent |
| L      | ↑   | Store data  |
| L      | L   | Storage     |

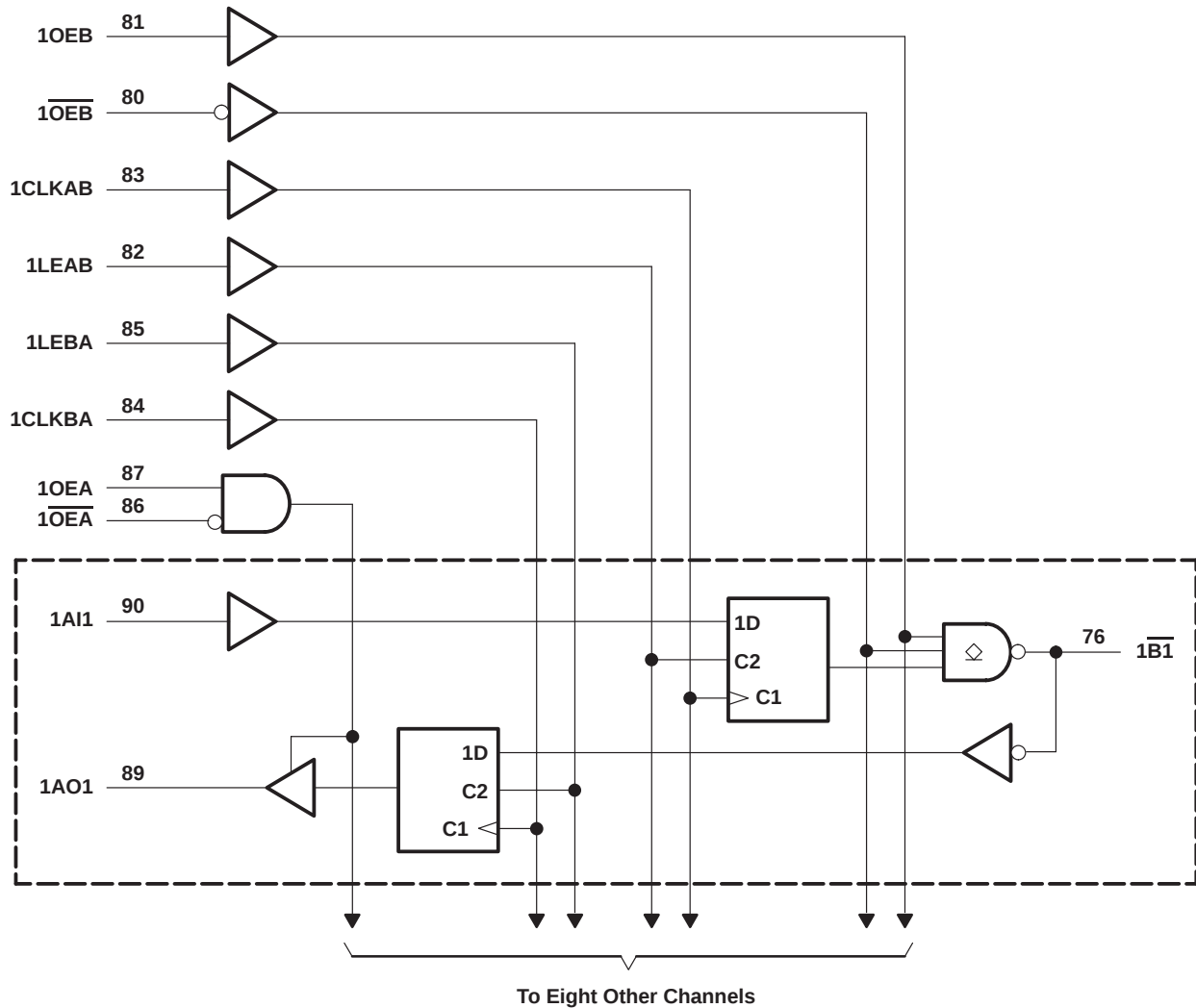


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functional block diagram



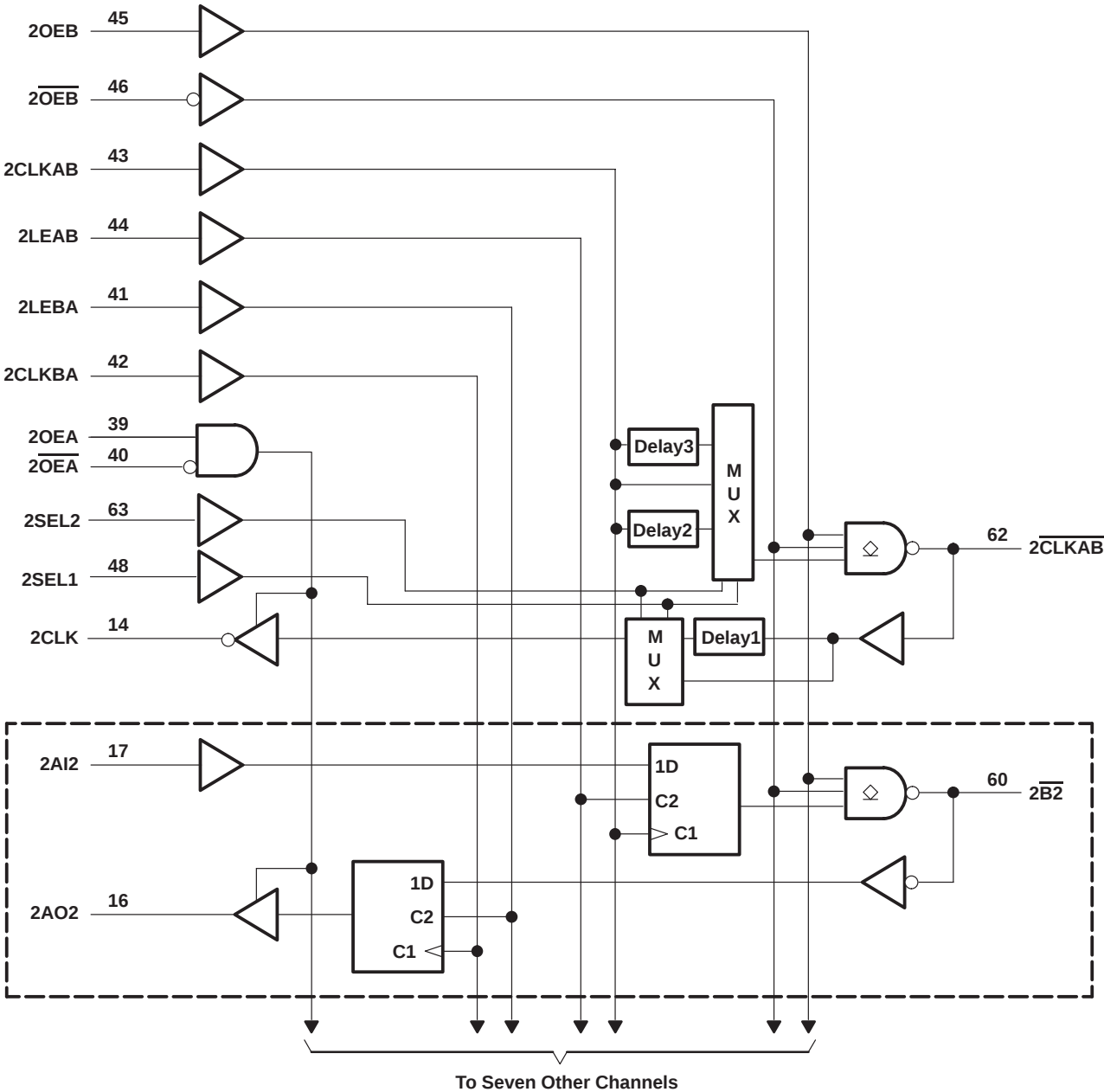
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17-BIT LVTTL/BTL UNIVERSAL STORAGE TRANSCEIVER

WITH BUFFERED CLOCK LINE

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functional block diagram (continued)



MUX-MODE DELAY

| INPUTS |       | DELAY PATH†      |                |
|--------|-------|------------------|----------------|
| 2SEL1  | 2SEL2 | 2CLKAB TO 2CLKAB | 2CLKAB TO 2CLK |
| L      | L     | No delay         | No delay       |
| L      | H     | No delay         | Delay1         |
| H      | L     | Delay2           | Delay1         |
| H      | H     | Delay3           | Delay1         |

† Refer to delay1 through delay3 in the functional block diagram.

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## 17-BIT LVTTTL/BTL UNIVERSAL STORAGE TRANSCEIVER WITH BUFFERED CLOCK LINE

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                       |                    |
|---------------------------------------------------------------------------------------|--------------------|
| Supply voltage range: $V_{CC}(5\text{ V})$ , BIAS $V_{CC}$ , BG $V_{CC}$              | –0.5 V to 7 V      |
| $V_{CC}(3.3\text{ V})$                                                                | –0.5 V to 4.6 V    |
| Input voltage range, $V_I$ : Except $\overline{B}$ port                               | –1.2 V to 7 V      |
| $\overline{B}$ port                                                                   | –1.2 V to 3.5 V    |
| Input clamp current, $I_{IK}$ : Except $\overline{B}$ port                            | –40 mA             |
| $\overline{B}$ port                                                                   | –18 mA             |
| Voltage range applied to any $\overline{B}$ output in the disabled or power-off state | –0.5 V to 3.5 V    |
| Voltage range applied to any output in the high state                                 | –0.5 V to $V_{CC}$ |
| Current applied to any single output in the low state: A port                         | 48 mA              |
| $\overline{B}$ port                                                                   | 200 mA             |
| Package thermal impedance, $\theta_{JA}$ (see Note 1)                                 | 22°C/W             |
| Storage temperature range, $T_{stg}$                                                  | –65°C to 150°C     |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 2)

|                                              |                                | MIN                        | NOM | MAX  | UNIT |
|----------------------------------------------|--------------------------------|----------------------------|-----|------|------|
| $V_{CC}$ ,<br>BG $V_{CC}$ ,<br>BIAS $V_{CC}$ | Supply voltage                 | 4.5                        | 5   | 5.5  | V    |
| $V_{CC}(3.3\text{ V})$                       | Supply voltage                 | 3                          | 3.3 | 3.6  | V    |
| $V_{IH}$                                     | High-level input voltage       | $\overline{B}$ port        |     | 1.62 | 2.3  |
|                                              |                                | Except $\overline{B}$ port |     | 2    |      |
| $V_{IL}$                                     | Low-level input voltage        | $\overline{B}$ port        |     | 0.75 | 1.47 |
|                                              |                                | Except $\overline{B}$ port |     | 0.8  |      |
| $I_{IK}$                                     | Input clamp current            |                            |     | –18  | mA   |
| $I_{OH}$                                     | High-level output current      | AO port                    |     | –3   | mA   |
| $I_{OL}$                                     | Low-level output current       | AO port                    |     | 24   | mA   |
|                                              |                                | $\overline{B}$ port        |     | 100  |      |
| $T_A$                                        | Operating free-air temperature | 0                          |     | 70   | °C   |

NOTE 2: To ensure proper device operation, all unused inputs must be terminated as follows: A and control inputs to  $V_{CC}(5\text{ V})$  or GND, and B inputs to GND only. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## electrical characteristics over recommended operating free-air temperature range

| PARAMETER              |                                                 | TEST CONDITIONS                                                                            |                                       | MIN  | TYP <sup>†</sup> | MAX  | UNIT          |
|------------------------|-------------------------------------------------|--------------------------------------------------------------------------------------------|---------------------------------------|------|------------------|------|---------------|
| $V_{IK}$               | $\overline{B}$ port                             | $V_{CC}(5\text{ V}) = 4.5\text{ V}$ ,                                                      | $I_I = -18\text{ mA}$                 |      |                  | -1.2 | V             |
|                        | Except $\overline{B}$ port                      | $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$                                                      | $I_I = -40\text{ mA}$                 |      |                  | -0.5 |               |
| $V_{OH}$               | AO port                                         | $V_{CC}(5\text{ V}) = 4.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3\text{ V}$               | $I_{OH} = -3\text{ mA}$               |      | 2.5              |      | V             |
| $V_{OL}$               | AO port                                         | $V_{CC}(5\text{ V}) = 4.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3\text{ V}$               | $I_{OL} = 24\text{ mA}$               |      | 0.35             | 0.5  | V             |
|                        | $\overline{B}$ port                             | $V_{CC}(5\text{ V}) = 4.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3\text{ V}$               | $I_{OL} = 80\text{ mA}$               | 0.75 |                  | 1.1  |               |
|                        |                                                 |                                                                                            | $I_{OL} = 100\text{ mA}$              |      |                  | 1.15 |               |
| $I_I$                  | Except $\overline{B}$ port                      | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_I = 5.5\text{ V}$                  |      |                  | 50   | $\mu\text{A}$ |
| $I_{IH}^{\ddagger}$    | Except $\overline{B}$ port                      | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_I = 2.7\text{ V}$                  |      |                  | 50   | $\mu\text{A}$ |
| $I_{IL}^{\ddagger}$    | Except $\overline{B}$ port                      | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_I = 0.5\text{ V}$                  |      |                  | -50  | $\mu\text{A}$ |
|                        | $\overline{B}$ port                             | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_I = 0.75\text{ V}$                 |      |                  | -100 |               |
| $I_{OH}$               | $\overline{B}$ port                             | $V_{CC}(5\text{ V}) = 0\text{ to }5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$ | $V_O = 2.1\text{ V}$                  |      |                  | 100  | $\mu\text{A}$ |
| $I_{OZH}$              | AO port                                         | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_O = 2.7\text{ V}$                  |      |                  | 50   | $\mu\text{A}$ |
| $I_{OZL}$              | AO port                                         | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.6\text{ V}$             | $V_O = 0.5\text{ V}$                  |      |                  | -50  | $\mu\text{A}$ |
| $I_{OZPU}$             | AO port                                         | $V_{CC} = 0\text{ to }2.1\text{ V}$ ,                                                      | $V_O = 0.5\text{ V to }2.7\text{ V}$  |      |                  | -50  | $\mu\text{A}$ |
| $I_{OZPD}$             | AO port                                         | $V_{CC} = 2.1\text{ V to }0$ ,                                                             | $V_O = 0.5\text{ V to }2.7\text{ V}$  |      |                  | -50  | $\mu\text{A}$ |
| $I_{CC}(5\text{ V})$   | AI port to $\overline{B}$ port                  | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.3\text{ V}$             | $I_O = 0$                             |      |                  | 145  | mA            |
|                        | $\overline{B}$ port to AO port                  |                                                                                            |                                       |      |                  | 130  |               |
|                        | Outputs disabled                                |                                                                                            |                                       |      |                  | 120  |               |
| $I_{CC}(3.3\text{ V})$ | $\overline{B}$ port to AO port                  | $V_{CC}(5\text{ V}) = 5.5\text{ V}$ ,<br>$V_{CC}(3.3\text{ V}) = 3.3\text{ V}$             | $I_O = 0$                             |      |                  | 1    | mA            |
| $C_i$                  | Control and AI inputs                           | $V_I = 0.5\text{ V or }2.5\text{ V}$                                                       |                                       |      | 6.5              |      | pF            |
| $C_o$                  | AO port                                         | $V_O = 0.5\text{ V or }2.5\text{ V}$                                                       |                                       |      | 3.5              |      | pF            |
| $C_{io}$               | $\overline{B}$ port per<br>IEEE Std 1194.1-1991 | $V_{CC}(5\text{ V}) = 0\text{ to }5.5\text{ V}$ ,                                          | $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$ |      |                  | 6.5  | pF            |

<sup>†</sup> All typical values are at  $V_{CC}(5\text{ V}) = 5\text{ V}$  and  $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>‡</sup> For I/O ports, the parameters  $I_{IH}$  and  $I_{IL}$  include the off-state output current.

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**live-insertion specifications over recommended operating free-air temperature range**

| PARAMETER                               |         | TEST CONDITIONS                                                            |                                                                                       | MIN  | MAX | UNIT |
|-----------------------------------------|---------|----------------------------------------------------------------------------|---------------------------------------------------------------------------------------|------|-----|------|
| I <sub>CC</sub> (BIAS V <sub>CC</sub> ) |         | V <sub>CC</sub> (5 V) = 0 to 4.5 V,<br>V <sub>CC</sub> (3.3 V) = 3.3 V     | V <sub>B</sub> = 0 to 2 V,<br>V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V | 450  |     | μA   |
|                                         |         | V <sub>CC</sub> (5 V) = 4.5 V to 5.5 V,<br>V <sub>CC</sub> (3.3 V) = 3.3 V |                                                                                       | 10   |     |      |
| V <sub>O</sub>                          | B̄ port | V <sub>CC</sub> (5 V) = 0,<br>V <sub>CC</sub> (3.3 V) = 0 V                | V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 5 V                                          | 1.62 | 2.1 | V    |
| I <sub>O</sub>                          | B̄ port | V <sub>CC</sub> (5 V) = 0,<br>V <sub>CC</sub> (3.3 V) = 0 V                | V <sub>B</sub> = 1 V,<br>V <sub>I</sub> (BIAS V <sub>CC</sub> ) = 4.5 V to 5.5 V      | −1   |     | μA   |
|                                         |         | V <sub>CC</sub> (5 V) = 0 to 2.2 V,<br>V <sub>CC</sub> (3.3 V) = 3.3 V     | OEB = 0 to 5 V                                                                        | 100  |     |      |
|                                         |         | V <sub>CC</sub> (5 V) = 0 to 5.5 V,<br>V <sub>CC</sub> (3.3 V) = 3.3 V     | OEB = 0 to 0.8 V                                                                      | 1    |     | mA   |

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

|                    |                 | MIN                                         | MAX | UNIT |
|--------------------|-----------------|---------------------------------------------|-----|------|
| $f_{\text{clock}}$ | Clock frequency |                                             | 90  | MHz  |
| $t_W$              | Pulse duration  | LE high                                     | 3   | ns   |
|                    |                 | CLK high or low                             | 3   |      |
| $t_{\text{su}}$    | Setup time      | AI or $\overline{B}$ before LE $\downarrow$ | 3.5 | ns   |
|                    |                 | AI or $\overline{B}$ before CLK $\uparrow$  | 3.5 |      |
| $t_h$              | Hold time       | AI or $\overline{B}$ after LE $\downarrow$  | 1   | ns   |
|                    |                 | AI or $\overline{B}$ after CLK $\uparrow$   | 0.7 |      |



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switching characteristics over recommended operating free-air temperature range,  
 $V_{CC}(5\text{ V}) = 5\text{ V} \pm 0.5\text{ V}$  and  $V_{CC}(3.3\text{ V}) = 3.3\text{ V}$  (see Figure 1)

| PARAMETER                                | FROM<br>(INPUT)                                                                                                             | TO<br>(OUTPUT)             | MIN | MAX  | UNIT |
|------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|----------------------------|-----|------|------|
| f <sub>max</sub>                         |                                                                                                                             |                            | 90  |      | MHz  |
| t <sub>PLH</sub>                         | AI                                                                                                                          | $\overline{\text{B}}$      | 1.8 | 6.2  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2.9 | 6.6  |      |
| t <sub>PLH</sub>                         | LEAB                                                                                                                        | $\overline{\text{B}}$      | 2.7 | 6.9  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 3.5 | 7.3  |      |
| t <sub>PLH</sub>                         | CLKAB                                                                                                                       | $\overline{\text{B}}$      | 2.3 | 6.4  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2.9 | 6.7  |      |
| t <sub>PLH</sub>                         | 2CLKAB<br>(no delay)                                                                                                        | $2\overline{\text{CLKAB}}$ | 2.3 | 6    | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2.9 | 6.7  |      |
| t <sub>PLH</sub>                         | 2CLKAB<br>(delay2)                                                                                                          | $2\overline{\text{CLKAB}}$ | 4.5 | 9.5  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 4.5 | 9.5  |      |
| t <sub>PLH</sub>                         | 2CLKAB<br>(delay3)                                                                                                          | $2\overline{\text{CLKAB}}$ | 9.3 | 15.4 | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 9.3 | 15.4 |      |
| t <sub>PLH</sub>                         | $\overline{\text{B}}$                                                                                                       | AO                         | 2   | 6.5  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2   | 6.5  |      |
| t <sub>PLH</sub>                         | LEBA                                                                                                                        | AO                         | 1.8 | 6.3  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 1.8 | 6.3  |      |
| t <sub>PLH</sub>                         | CLKBA                                                                                                                       | AO                         | 1.8 | 6.3  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 1.8 | 6.3  |      |
| t <sub>PLH</sub>                         | $2\overline{\text{CLKAB}}$<br>(delay1)                                                                                      | 2CLK                       | 5.7 | 12.3 | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 5.7 | 12.3 |      |
| t <sub>PLH</sub>                         | $2\overline{\text{CLKAB}}$<br>(no delay)                                                                                    | 2CLK                       | 2   | 6.5  | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2   | 6.5  |      |
| t <sub>PLH</sub>                         | OEB or $\overline{\text{OEB}}$                                                                                              | $\overline{\text{B}}$      | 2.6 | 7    | ns   |
| t <sub>PHL</sub>                         |                                                                                                                             |                            | 2.6 | 7    |      |
| t <sub>PZH</sub>                         | OEA or $\overline{\text{OEA}}$                                                                                              | AO                         | 1.4 | 5.5  | ns   |
| t <sub>PZL</sub>                         |                                                                                                                             |                            | 1.4 | 5.5  |      |
| t <sub>PHZ</sub>                         | OEA or $\overline{\text{OEA}}$                                                                                              | AO                         | 1.4 | 6.5  | ns   |
| t <sub>PLZ</sub>                         |                                                                                                                             |                            | 1.4 | 5.8  |      |
| t <sub>sk(p)</sub> <sup>†</sup>          | Pulse skew, AI to $\overline{\text{B}}$ or $\overline{\text{B}}$ to AO                                                      |                            | 1.6 |      | ns   |
|                                          | Pulse skew, $2\overline{\text{CLKAB}}$ to 2CLK                                                                              |                            | 1.8 |      |      |
| t <sub>sk(p)</sub>                       | Pulse skew, CLKAB to $\overline{\text{B}}$ or CLKBA to AO                                                                   |                            | 1.5 |      | ns   |
|                                          | Pulse skew, CLKAB to $2\overline{\text{CLKAB}}$                                                                             |                            | 1.4 |      |      |
| t <sub>sk(HL), t<sub>sk(LH)</sub>†</sub> | Output skew, AI to $\overline{\text{B}}$ or $\overline{\text{B}}$ to AO                                                     |                            | 1   |      | ns   |
| t <sub>sk(o)</sub> <sup>‡</sup>          | Output skew, nondelayed mode for $2\overline{\text{CLKAB}}$ , CLKAB to AO                                                   |                            | 1   |      | ns   |
|                                          | Output skew, nondelayed mode for $2\overline{\text{CLKAB}}$ , CLKAB to $\overline{\text{B}}$ and $2\overline{\text{CLKAB}}$ |                            | 1   |      |      |
| t <sub>sk(o)</sub> <sup>‡</sup>          | Output skew, nondelayed mode for $2\overline{\text{CLKAB}}$ , CLKAB to $\overline{\text{B}}$ and $2\overline{\text{CLKAB}}$ |                            | 1.5 |      | ns   |
| t <sub>t</sub>                           | Transition time, $\overline{\text{B}}$ outputs (1.3 V to 1.8 V)                                                             |                            | 0.5 | 4.6  | ns   |
|                                          | Transition time, AO outputs (10% to 90%)                                                                                    |                            | 0.4 | 4.2  |      |
| t <sub>PR</sub>                          | $\overline{\text{B}}$ -port input pulse rejection                                                                           |                            | 1   |      | ns   |

$^{\dagger}$  Skew values are applicable for through mode only, with single-output switching.

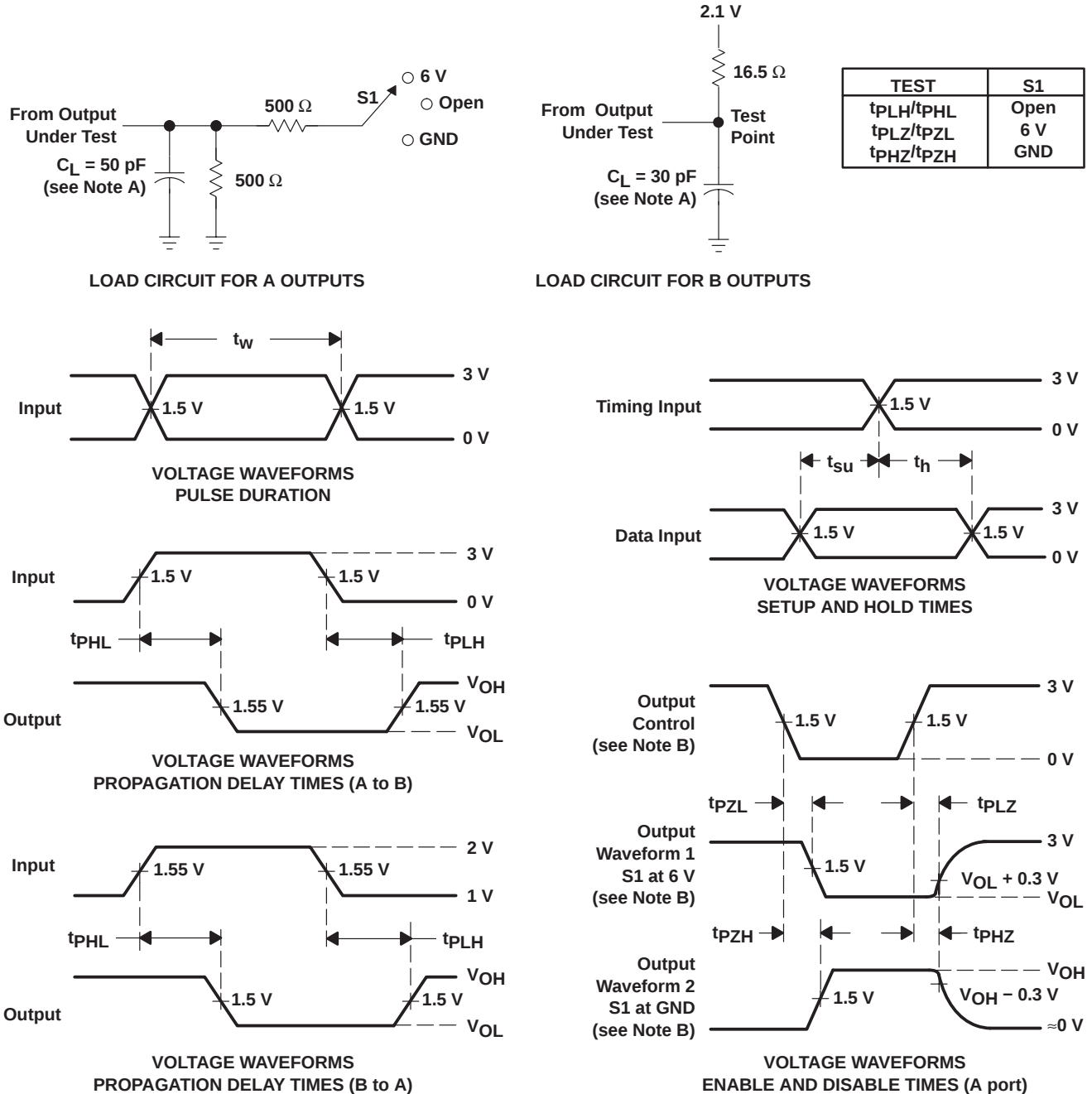
$^{\ddagger}$  Skew values are applicable for CLK mode only, with all outputs simultaneously switching high-to-low or low-to-high.

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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: TTL inputs:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns; BTL inputs:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 1$  ns,  $t_f \leq 1$  ns.
- D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins    | Package qty   Carrier  | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-------------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74FB1653PCA</a> | Active        | Production           | HLQFP (PCA)   100 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | FB1653              |
| SN74FB1653PCA.B               | Active        | Production           | HLQFP (PCA)   100 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | FB1653              |
| SN74FB1653PCAG4               | Active        | Production           | HLQFP (PCA)   100 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | FB1653              |
| SN74FB1653PCAG4.B             | Active        | Production           | HLQFP (PCA)   100 | 90   JEDEC TRAY (10+1) | Yes         | NIPDAU                               | Level-3-260C-168 HR               | 0 to 70      | FB1653              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

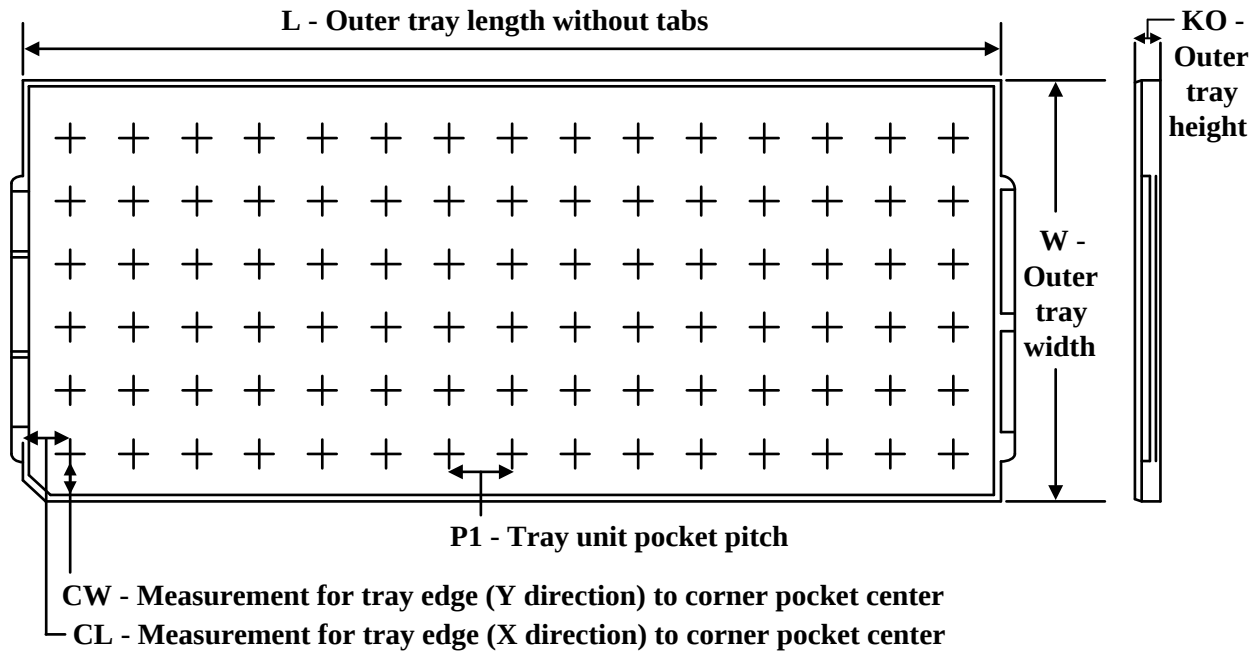
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TRAY**


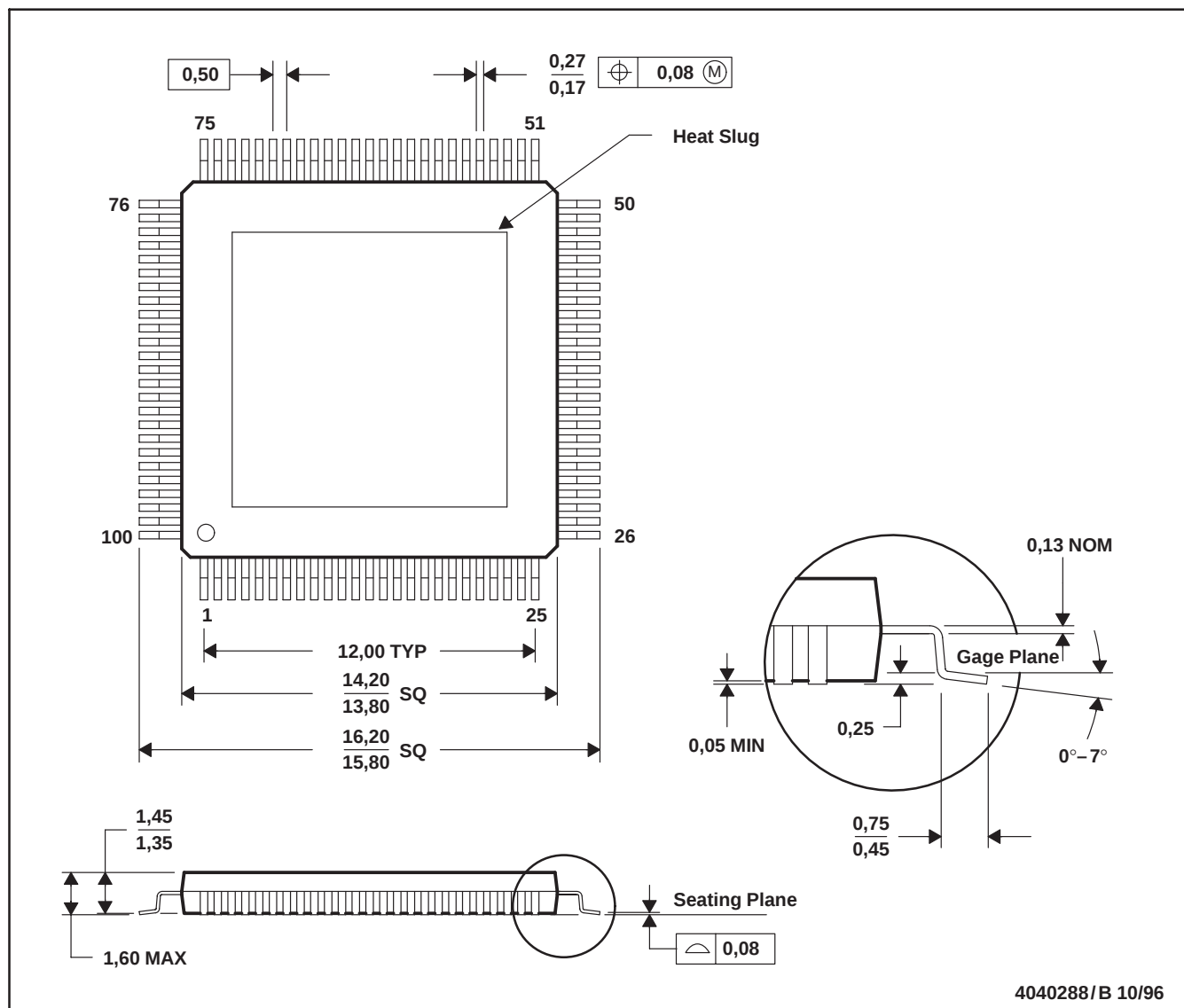
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device            | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| SN74FB1653PCA     | PCA          | HLQFP        | 100  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| SN74FB1653PCA.B   | PCA          | HLQFP        | 100  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| SN74FB1653PCAG4   | PCA          | HLQFP        | 100  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |
| SN74FB1653PCAG4.B | PCA          | HLQFP        | 100  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 20.3    | 15.4    | 15.45   |

## PCA (S-PQFP-G100)

## PLASTIC QUAD FLATPACK (DIE DOWN)



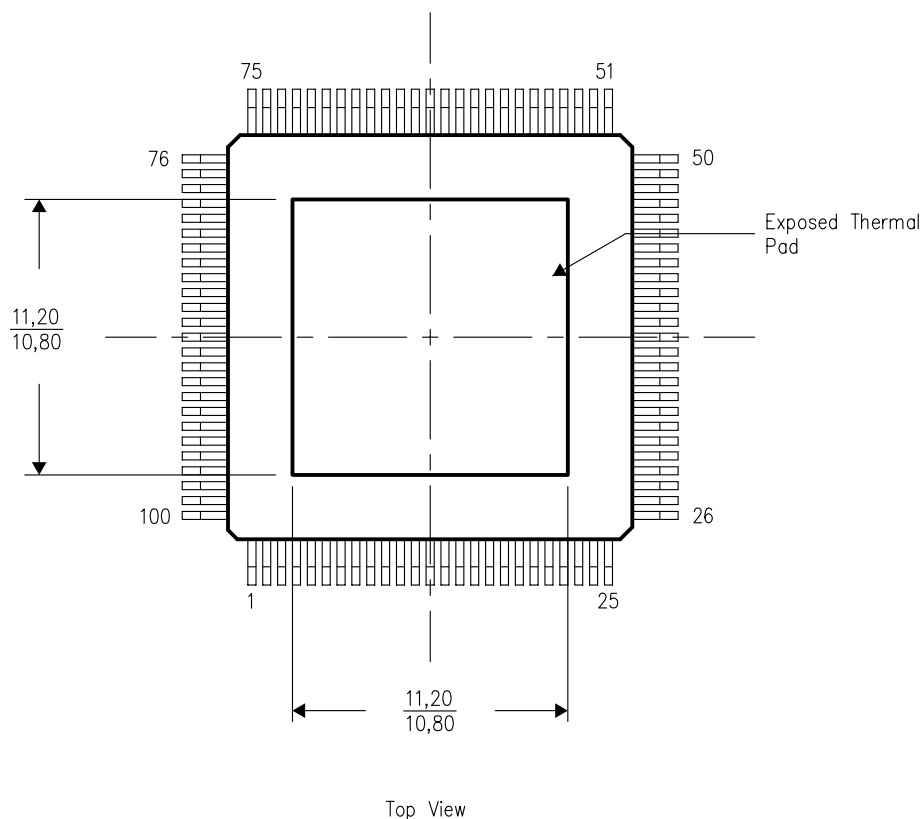
- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Thermally enhanced molded plastic package with a heat slug (HSL)
  - Falls within JEDEC MS-026

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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