

# SN74GTL2006

## 13-BIT GTL-/GTL/GTL+ TO LVTTL TRANSLATOR

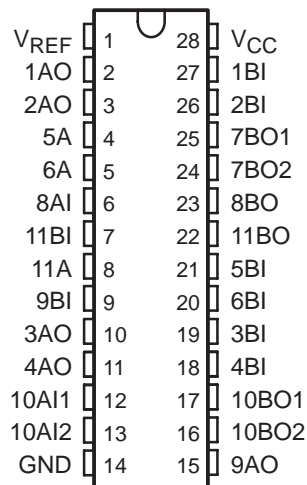
SCES619 – DECEMBER 2004

- Operates as GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator
- Series Termination on TTL Outputs of 30  $\Omega$
- Latch-Up Testing to JEDEC Standard JESD 78 Exceeds 500 mA
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### description

The SN74GTL2006 is a 13-bit translator to interface between the 3.3-V LVTTL chipset I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.

PW PACKAGE  
(TOP VIEW)



### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V <sub>REF</sub>	GTL reference voltage
2–6, 8, 10–13, 15	nAn	Data inputs/outputs (LVTTL)
7, 9, 16, 17–27	nBn	Data inputs/outputs (GTL-/GTL/GTL+)
14	GND	Ground (0 V)
28	V <sub>CC</sub>	Positive supply voltage

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tube	SN74GTL2006PW
		Tape and reel	SN74GTL2006PWR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design, guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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Function Tables

INPUTS 1BI/2BI/3BI/4BI/9BI	OUTPUTS 1AO/2AO/3AO/4AO/9AO
L	L
H	H

INPUT 8AI	OUTPUT 8BO
L	L
H	H

INPUTS		OUTPUTS 10BO1/10BO2
10AI1/10AI2	9BI	
L	L	L
L	H	L
H	L	L
H	H	H

INPUTS 5BI/6BI	INPUTS/OUTPUTS 5A/6A (OPEN DRAIN)	OUTPUTS 7BO1/7BO2
L	L	H <sup>†</sup>
H	L <sup>‡</sup>	L
H	H	H

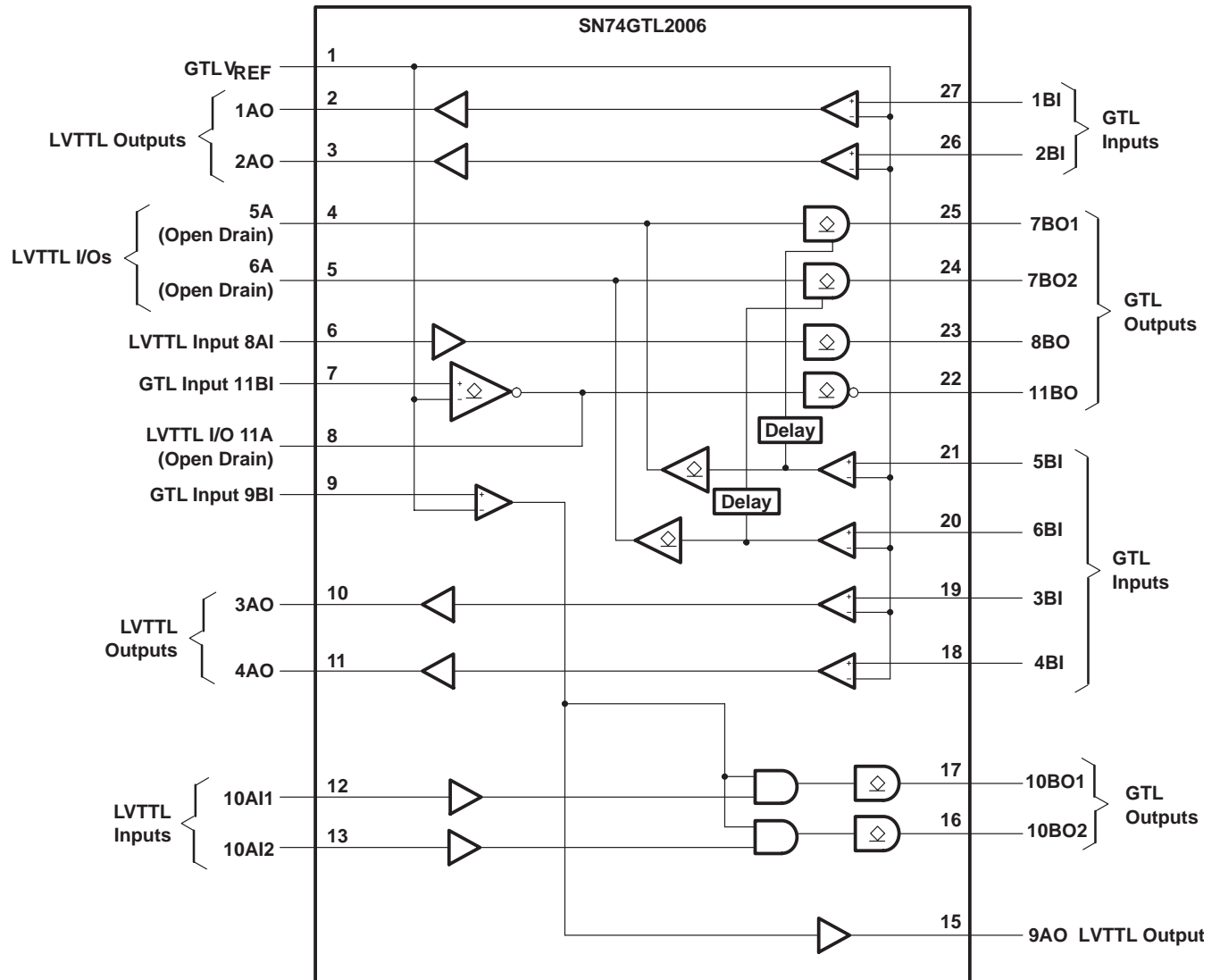
<sup>†</sup> The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (when 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

<sup>‡</sup> Open-drain input/output terminal is driven to a logic-low state by an external driver.

INPUT 11BI	INPUT/OUTPUT 11A (OPEN DRAIN)	OUTPUT 11BO
L	H	L
L	L <sup>‡</sup>	H
H	L	H

<sup>‡</sup> Open-drain input/output terminal is driven to a logic-low state by an external driver.

**logic symbol**



NOTE A: The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

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### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†‡</sup>

Supply voltage range, $V_{CC}$	–0.5 to 4.6 V
Input voltage range, $V_I$ (see Note 2): A port (LVTTTL)	–0.5 to 4.6 V
B port (GTL)	–0.5 to 4.6 V
Output voltage range, $V_O$ (output in OFF or HIGH state)(see Note 2): A port	–0.5 to 4.6 V
B port	–0.5 to 4.6 V
Input diode current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output diode current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Current into any output in the LOW state: A port	32 mA
B port	30 mA
Current into any output in the HIGH state, A port	–32 mA
Storage temperature range, $T_{stg}$	–60 to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>‡</sup> Voltages are referenced to GND (ground = 0 V).

- NOTES: 1. The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
V <sub>TT</sub>	Termination voltage	GTL−	0.85	0.9	V
		GTL	1.14	1.2	
		GTL+	1.35	1.5	
V <sub>REF</sub>	Reference voltage	Overall	0.5	2/3 V <sub>TT</sub>	V
		GTL−	0.5	0.6	
		GTL	0.76	0.8	
		GTL+	0.87	1	
V <sub>I</sub>	Input voltage	A port	0	3.3	V
		B port	0	V <sub>TT</sub>	
V <sub>IH</sub>	High-level input voltage	A port	2		V
		B port	V <sub>REF</sub> + 50 mV		
V <sub>IL</sub>	Low-level input voltage	A port	0.8		V
		B port	V <sub>REF</sub> − 50 mV		
I <sub>OH</sub>	High-level output current	A port	−16		mA
I <sub>OL</sub>	Low-level output current	A port	16		mA
		B port	15		
T <sub>A</sub>	Operating free-air temperature range		−40	85	°C



**electrical characteristics over recommended operating conditions**

PARAMETER		TEST CONDITIONS		–40°C TO 85°C			UNIT	
				MIN	TYP†	MAX		
VOH‡	A port	VCC = 3 V to 3.6 V, IOH = –100 µA		VCC – 0.2			V	
		VCC = 3 V, IOH = –16 mA		2.1				
VOL‡	A port	VCC = 3 V, IOL = 16 mA		0.8			V	
	B port	VCC = 3 V, IOL = 15 mA		0.4				
II	A port	VCC = 3.6 V	VI = VCC	±1			µA	
			VI = 0 V	±1				
	B port	VCC = 3.6 V, VI = VTT or GND		±1				
ICC	A or B port	VCC = 3.6 V, VI = VCC or GND, IO = 0		12			mA	
ΔICC§	A port or control inputs		VCC = 3.6 V, VI = VCC – 0.6 V		500			µA
CIO	A port	VO = 3 V or 0, VO = 3 V or 0		5			pF	
	B port	VO = VTT or 0, VO = VTT or 0		4				

† All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

§ This is the increase in supply current for each input that is at the specified LVTTTL voltage, rather than  $V_{CC}$  or GND.

**switching characteristics over recommended operating free-air temperature range**

PARAMETER		WAVEFORM	GTL–			GTL			GTL+			UNIT
			VCC = 3.3 V ± 0.3 V, VREF = 0.6 V			VCC = 3.3 V ± 0.3 V, VREF = 0.8 V			VCC = 3.3 V ± 0.3 V, VREF = 1 V			
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
tPLH	An to Bn	1	2	4	8	2	4	8	2	4	8	ns
tPHL			2	5.5	10	2	5.5	10	2	5.5	10	
tPLH	Bn to An	2	2	5.5	10	2	5.5	10	2	5.5	10	ns
tPHL			2	5.5	10	2	5.5	10	2	5.5	10	
tPLH	9BI to 10BOn	3	2	6	11	2	6	11	2	6	11	ns
tPHL			2	6	11	2	6	11	2	6	11	
tPLH	11BI to 11BO	3	2	8	13	2	8	13	2	8	13	ns
tPHL†			2	14	21	2	14	21	2	14	21	
tPLH	Bn to Bn	3	4	7	11	4	7	11	4	7	11	ns
tPHL			120	205	350	120	205	350	120	205	350	
tPLZ	Bn to An (I/O)	4	2	5	10	2	5	10	2	5	10	ns
tPZL			2	5	10	2	5	10	2	5	10	

† All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

¶ Includes ~7.6-ns RC rise time of test-load pullup on 11-A, 1.5-k $\Omega$  pullup, and 21-pF load on 11 A has approximately 23-ns RC rise time.

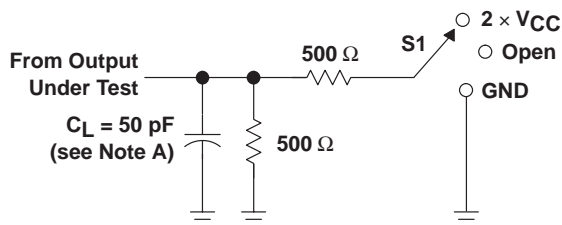
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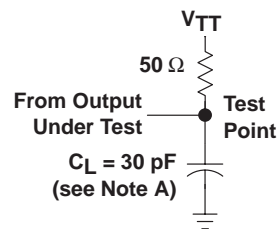
### PARAMETER MEASUREMENT INFORMATION

$V_{TT} = 1.2 \text{ V}$ ,  $V_{REF} = 0.8 \text{ V}$  FOR GTL AND  $V_{TT} = 1.5 \text{ V}$ ,  $V_{REF} = 1 \text{ V}$  FOR GTL+

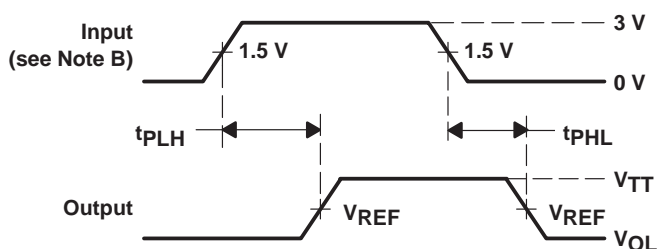


LOAD CIRCUIT FOR A OUTPUTS

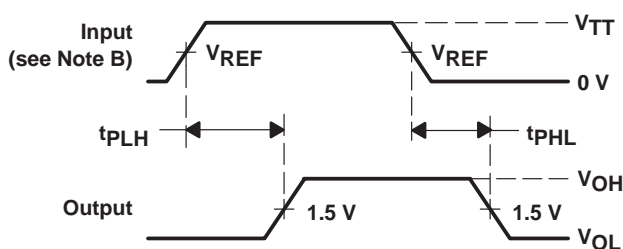
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$



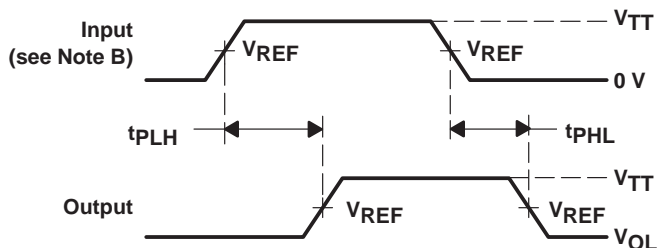
LOAD CIRCUIT FOR B OUTPUTS



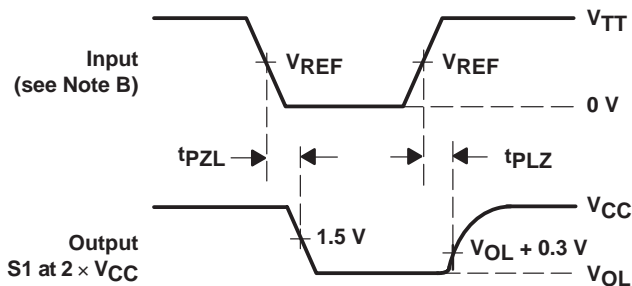
VOLTAGE WAVEFORM 1  
PROPAGATION DELAY TIMES  
(A port to B port)<sup>†</sup>



VOLTAGE WAVEFORM 2  
PROPAGATION DELAY TIMES  
(B port to A port)<sup>†</sup>



VOLTAGE WAVEFORM 3  
PROPAGATION DELAY TIMES  
(B port to B port)<sup>†</sup>



VOLTAGE WAVEFORM 4  
PROPAGATION DELAY TIMES  
(B port to A (I/O) port)<sup>†</sup>

<sup>†</sup> All control inputs are LVTTTL levels.

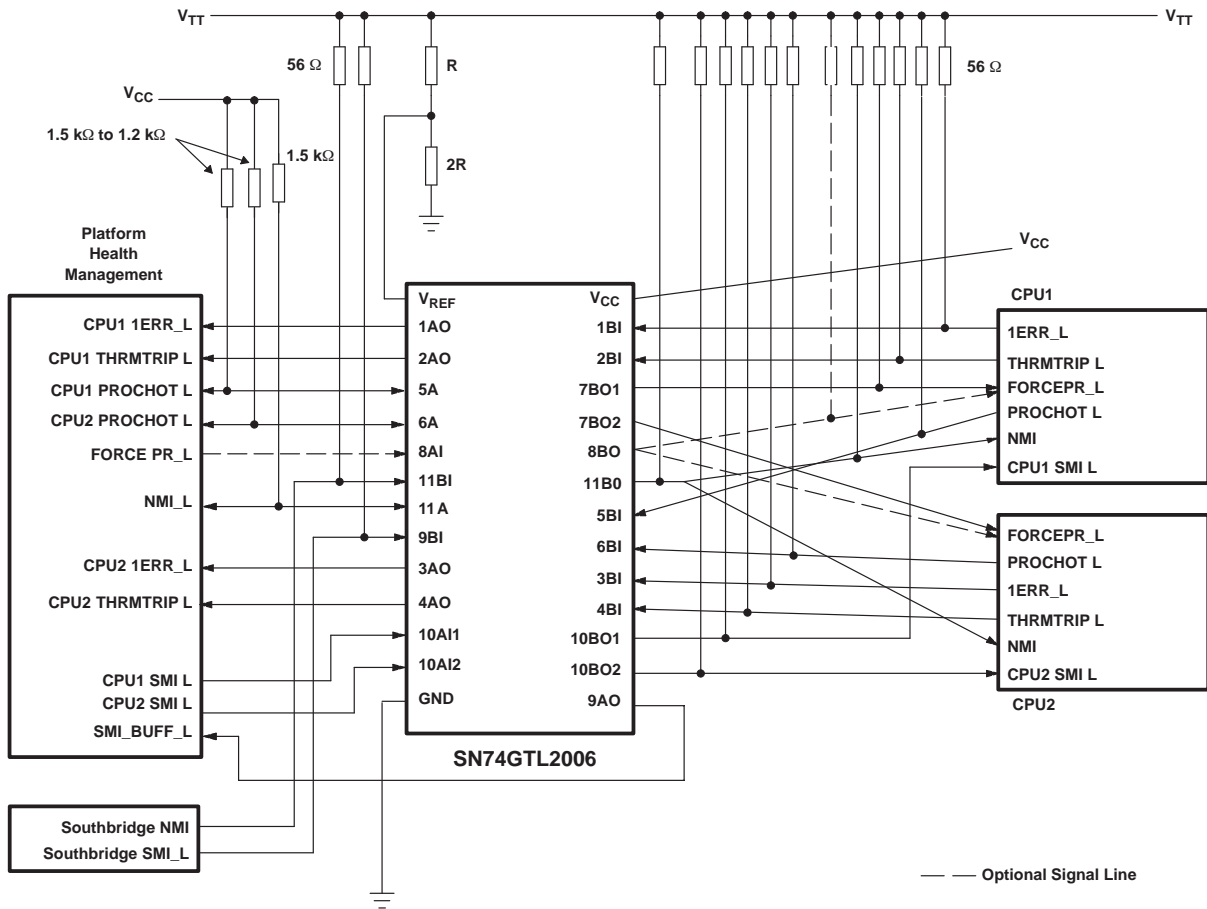
NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .

C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## APPLICATION INFORMATION



### frequently asked questions

**Question 1:** On SN74GTL2006 LVTTTL inputs, specifically 10AI1 and 10AI2, when the device is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTTL inputs high impedance when the device is powered down, and will there be any leakage?

**Answer 1:** When the device is powered down, the LVTTTL inputs are in a high-impedance state and do not leak to  $V_{DD}$  if they are pulled high while the device is powered down.

**Question 2:** Do all the LVTTTL inputs have the same powered-down characteristic?

**Answer 2:** Yes

**Question 3:** What is the condition of the other GTL I/O and LVTTTL output pins when the device is powered down?

**Answer 3:** The open-drain outputs, both GTL and LVTTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTTL totem-pole outputs, however, are not open-drain type outputs, and there will be current flow on these pins if they are pulled high when  $V_{DD}$  is at ground.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74GTL2006PWR</a>	Active	Production	TSSOP (PW)   28	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2006
SN74GTL2006PWR.B	Active	Production	TSSOP (PW)   28	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	GK2006

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTL2006PWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

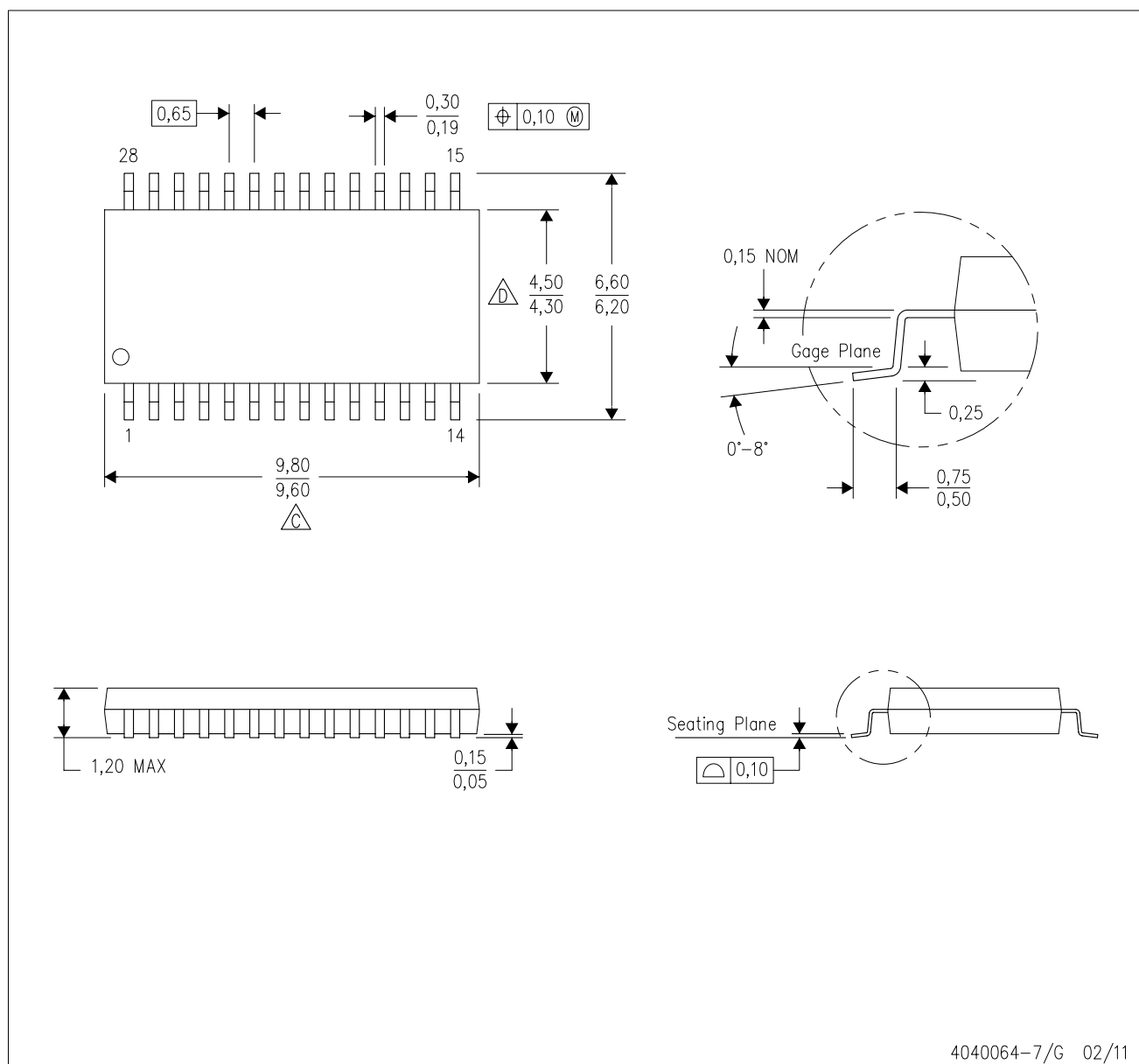


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTL2006PWR	TSSOP	PW	28	2000	353.0	353.0	32.0

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO–153

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