



SNx4HC164 8-Bit Parallel-Out Serial Shift Registers

1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up to 10 LSTTL Loads
- Low Power Consumption, 80- μ A Maximum I_{CC}
- Typical $t_{pd} = 20$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1- μ A Maximum
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Programmable Logic Controllers
- Appliances
- Video Display Systems
- Output Expander

3 Description

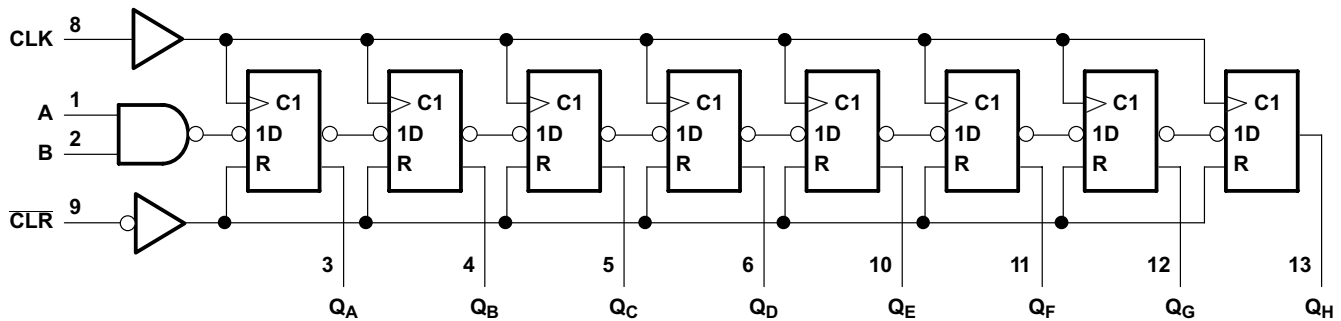
These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear (CLR) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum set-up time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|---------------------------|
| SN74HC164 | SOIC (14) | 8.65 mm \times 3.91 mm |
| | PDIP (14) | 19.30 mm \times 6.35 mm |
| | SO (14) | 10.30 mm \times 5.30 mm |
| | TSSOP (14) | 5.00 mm \times 4.40 mm |
| SN54HC164 | CDIP (14) | 19.94 mm \times 6.92 mm |
| | CFP (14) | 9.21 mm \times 6.29 mm |
| | LCCC (14) | 9.39 mm \times 9.39 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.



Table of Contents

| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 8 Parameter Measurement Information | 13 |
| 2 Applications | 1 | 9 Detailed Description | 14 |
| 3 Description | 1 | 9.1 Overview | 14 |
| 4 Revision History | 2 | 9.2 Functional Block Diagram | 14 |
| 5 Device Comparison Table | 3 | 9.3 Feature Description | 14 |
| 6 Pin Configuration and Functions | 4 | 9.4 Device Functional Modes | 14 |
| 7 Specifications | 6 | 10 Application and Implementation | 15 |
| 7.1 Absolute Maximum Ratings | 6 | 10.1 Application Information | 15 |
| 7.2 ESD Ratings | 6 | 10.2 Typical Application | 15 |
| 7.3 Recommended Operating Conditions | 6 | 11 Power Supply Recommendations | 17 |
| 7.4 Thermal Information | 7 | 12 Layout | 17 |
| 7.5 Electrical Characteristics, $T_A = 25^{\circ}\text{C}$ | 7 | 12.1 Layout Guidelines | 17 |
| 7.6 Electrical Characteristics, $T_A = -55^{\circ}\text{C}$ to 125°C | 7 | 12.2 Layout Example | 17 |
| 7.7 Electrical Characteristics, $T_A = -55^{\circ}\text{C}$ to 85°C | 8 | 13 Device and Documentation Support | 18 |
| 7.8 Timing Requirements, $T_A = 25^{\circ}\text{C}$ | 8 | 13.1 Documentation Support | 18 |
| 7.9 Timing Requirements, $T_A = -55^{\circ}\text{C}$ to 125°C | 9 | 13.2 Related Links | 18 |
| 7.10 Timing Requirements, $T_A = -55^{\circ}\text{C}$ to 85°C | 9 | 13.3 Community Resources | 18 |
| 7.11 Switching Characteristics, $T_A = 25^{\circ}\text{C}$ | 10 | 13.4 Trademarks | 18 |
| 7.12 Switching Characteristics, $T_A = -55^{\circ}\text{C}$ to 125°C .. | 10 | 13.5 Electrostatic Discharge Caution | 18 |
| 7.13 Switching Characteristics, $T_A = -55^{\circ}\text{C}$ to 85°C | 11 | 13.6 Glossary | 18 |
| 7.14 Typical Characteristics | 12 | 14 Mechanical, Packaging, and Orderable Information | 18 |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (October 2013) to Revision G | Page |
|--|------|
| • Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Added Military Disclaimer to <i>Features</i> list | 1 |
| • Added Handling Ratings table | 6 |

| Changes from Revision E (November 2010) to Revision F | Page |
|---|------|
| • Updated document to new TI data sheet format | 1 |
| • Removed Ordering Information table | 1 |
| • Updated operating temperature range | 6 |

5 Device Comparison Table

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SN74HC164D | SOIC (14) | 8.65 mm × 3.91 mm |
| SN74HC164N | PDIP (14) | 19.30 mm × 6.35 mm |
| SN74HC164NS | SO (14) | 10.30 mm × 5.30 mm |
| SN74HC164PW | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN54HC164J | CDIP (14) | 19.94 mm × 6.92 mm |
| SN54HC164W | CFP (14) | 9.21 mm × 6.29 mm |
| SN54HC164FK | LCCC (14) | 9.39 mm × 9.39 mm |

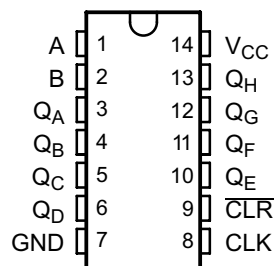
SN54HC164, SN74HC164

SCLS115G –DECEMBER 1982–REVISED SEPTEMBER 2015

www.ti.com

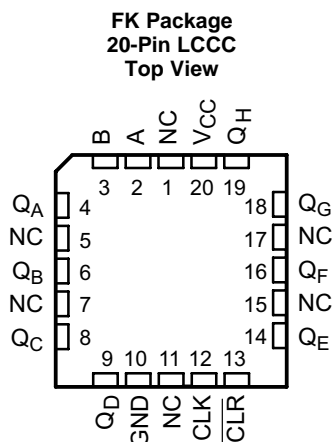
6 Pin Configuration and Functions

D, N, NS, J, W, or PW Package
14-Pin SOIC, PDIP, SO, CDIP, CFP, or TSSOP
Top View



Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|-------------------------|-----|----------------------|
| SOIC, PDIP, SO, CDIP, CFP, or TSSOP NO. | NAME | | |
| 1 | A | I | Gated Serial Input 1 |
| 2 | B | I | Gated Serial Input 2 |
| 3 | Q _A | O | Parallel Output |
| 4 | Q _B | O | Parallel Output |
| 5 | Q _C | O | Parallel Output |
| 6 | Q _D | O | Parallel Output |
| 7 | GND | - | Ground |
| 8 | CLK | I | Clock |
| 9 | $\overline{\text{CLR}}$ | I | Clear 1 Active-Low |
| 10 | Q _E | O | Parallel Output |
| 11 | Q _F | O | Parallel Output |
| 12 | Q _G | O | Parallel Output |
| 13 | Q _H | O | Parallel Output |
| 14 | V _{CC} | — | Power |



NC – No internal connection

Pin Functions

| PIN | | I/O | DESCRIPTION |
|----------|-------------------------|-----|----------------------|
| LCCC NO. | NAME | | |
| 1 | NC | — | No Connect |
| 2 | A | I | Gated Serial Input 1 |
| 3 | B | I | Gated Serial Input 2 |
| 4 | Q _A | O | Parallel Output |
| 5 | NC | — | No Connect |
| 6 | Q _B | O | Parallel Output |
| 7 | NC | — | No Connect |
| 8 | Q _C | O | Parallel Output |
| 9 | Q _D | O | Parallel Output |
| 10 | GND | — | Ground |
| 11 | NC | — | No Connect |
| 12 | CLK | I | Clock |
| 13 | $\overline{\text{CLR}}$ | I | Clear 1 Active-Low |
| 14 | Q _E | O | Parallel Output |
| 15 | NC | — | No Connect |
| 16 | Q _F | O | Parallel Output |
| 17 | NC | — | No Connect |
| 18 | Q _G | O | Parallel Output |
| 19 | Q _H | O | Parallel Output |
| 20 | VCC | — | Power |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNITS |
|-----------|--|-----------------------------|------|----------|-------|
| V_{CC} | Supply voltage | | -0.5 | 7 | V |
| I_{IK} | Input clamp current ⁽²⁾ | $V_I < 0$ or $V_I > V_{CC}$ | | ± 20 | mA |
| I_{OK} | Output clamp current ⁽²⁾ | $V_O < 0$ or $V_O > V_{CC}$ | | ± 20 | mA |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | | ± 25 | mA |
| | Continuous current through V_{CC} or GND | | | ± 50 | mA |
| T_{stg} | Storage temperature | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

| | | VALUE | UNIT |
|-------------|-------------------------|--|------------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ± 1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54HC164 | | | SN74HC164 | | | UNIT |
|---------------------------|-------------------------------------|------------------|-----|----------|-----------|-----|----------|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2$ V | | 1.5 | 1.5 | | | V |
| | | $V_{CC} = 4.5$ V | | 3.15 | 3.15 | | | |
| | | $V_{CC} = 6$ V | | 4.2 | 4.2 | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2$ V | | 0.5 | 0.5 | | | V |
| | | $V_{CC} = 4.5$ V | | 1.35 | 1.35 | | | |
| | | $V_{CC} = 6$ V | | 1.8 | 1.8 | | | |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta V^{(2)}$ | Input transition rise and fall time | $V_{CC} = 2$ V | | 1000 | 1000 | | | ns |
| | | $V_{CC} = 4.5$ V | | 500 | 500 | | | |
| | | $V_{CC} = 6$ V | | 400 | 400 | | | |
| T_A | Operating free-air temperature | -55 | | 125 | -40 | | 125 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).
- (2) If this device is used in the threshold region (from V_{IL} max = 0.5 V to V_{IH} min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_i = 1000$ ns and $V_{CC} = 2$ V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN54HC164 | | | SN74HC164 | | | | UNIT |
|---|-------------|------------|--------------|-------------|-------------|------------|---------------|------|
| | J (CDIP) | W (CFP) | FK (LCCC) | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | 14 PINS | 14 PINS | 20 PINS | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | — | — | — | 86 | 80 | 76 | 113 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics, T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|---|---------------------------|-----------------|------|-------|------|------|
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = −20 μA | 2 V | 1.9 | 1.998 | V | |
| | | | 4.5 V | 4.4 | 4.499 | | |
| | | | 6 V | 5.9 | 5.999 | | |
| | | I _{OH} = −4 mA | 4.5 V | 3.98 | 4.3 | | |
| | | I _{OH} = −5.2 mA | 6 V | 5.48 | 5.8 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | 0.002 | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | 0.17 | 0.26 | |
| | | I _{OL} = 5.2 mA | 6 V | | 0.15 | 0.26 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | nA |
| I _{CC} | V _I = V _{CC} or 0 | I _O = 0 | 6 V | | | 8 | μA |
| C _i | | | 2 V to 6 V | | 3 | 10 | pF |

7.6 Electrical Characteristics, T_A = –55°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | SN54HC164 | | | Recommended SN74HC164 | | | UNIT |
|-----------------|---|---------------------------|--------------------|-----------|-----|-------|-----------------------|-----|-------|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = –20 μA | 2 V | 1.9 | | | 1.9 | | | V |
| | | | 4.5 V | 4.4 | | | 4.4 | | | |
| | | | 6 V | 5.9 | | | 5.9 | | | |
| | | I _{OH} = –4 mA | 4.5 V | | 3.7 | | | 3.7 | | |
| | | I _{OH} = –5.2 mA | 6 V | | 5.2 | | | 5.2 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 μA | 2 V | | | 0.1 | | | 0.1 | V |
| | | | 4.5 V | | | 0.1 | | | 0.1 | |
| | | | 6 V | | | 0.1 | | | 0.1 | |
| | | I _{OL} = 4 mA | 4.5 V | | | 0.4 | | | 0.4 | |
| | | I _{OL} = 5.2 mA | 6 V | | | 0.4 | | | 0.4 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | | ±1000 | | | ±1000 | nA |
| I _{CC} | V _I = V _{CC} or 0 | | I _O = 0 | 6 V | | 160 | | | 160 | μA |
| C _i | | | 2 V to 6 V | | | 10 | | | 10 | pF |

SN54HC164, SN74HC164

SCLS115G –DECEMBER 1982–REVISED SEPTEMBER 2015

www.ti.com
7.7 Electrical Characteristics, $T_A = -55^{\circ}\text{C}$ to 85°C

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V_{CC} | SN74HC164 | | | UNIT |
|-----------|----------------------------|-----------------------------|------------|-----------|-----|------------|---------------|
| | | | | MIN | TYP | MAX | |
| V_{OH} | $V_I = V_{IH}$ or V_{IL} | $I_{OH} = -20\ \mu\text{A}$ | 2 V | 1.9 | | | V |
| | | | 4.5 V | 4.4 | | | |
| | | | 6 V | 5.9 | | | |
| | | $I_{OH} = -4\ \text{mA}$ | 4.5 V | 3.84 | | | |
| | | $I_{OH} = -5.2\ \text{mA}$ | 6 V | 5.34 | | | |
| V_{OL} | $V_I = V_{IH}$ or V_{IL} | $I_{OL} = 20\ \mu\text{A}$ | 2 V | | | 0.1 | V |
| | | | 4.5 V | | | 0.1 | |
| | | | 6 V | | | 0.1 | |
| | | $I_{OL} = 4\ \text{mA}$ | 4.5 V | | | 0.33 | |
| | | $I_{OL} = 5.2\ \text{mA}$ | 6 V | | | 0.33 | |
| I_I | $V_I = V_{CC}$ or 0 | | 6 V | | | ± 1000 | nA |
| I_{CC} | $V_I = V_{CC}$ or 0 | $I_O = 0$ | 6 V | | | 80 | μA |
| C_i | | | 2 V to 6 V | | | 10 | pF |

7.8 Timing Requirements, $T_A = 25^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | V_{CC} | MIN | NOM | MAX | UNIT |
|--------------------|--------------------------------------|----------|-----|-----|-----|------|
| f_{clock} | Clock frequency | 2 V | | | 6 | MHz |
| | | 4.5 V | | | 31 | |
| | | 6 V | | | 36 | |
| t_w | Pulse duration | 2 V | 100 | | | ns |
| | | 4.5 V | 20 | | | |
| | | 6 V | 17 | | | |
| | CLK high or low | 2 V | 80 | | | |
| | | 4.5 V | 16 | | | |
| | | 6 V | 14 | | | |
| t_{su} | Setup time before CLK \uparrow | 2 V | 100 | | | ns |
| | | 4.5 V | 20 | | | |
| | | 6 V | 17 | | | |
| | $\overline{\text{CLR}}$ inactive | 2 V | 100 | | | |
| | | 4.5 V | 20 | | | |
| | | 6 V | 17 | | | |
| t_h | Hold time, data after CLK \uparrow | 2 V | 5 | | | ns |
| | | 4.5 V | 5 | | | |
| | | 6 V | 5 | | | |

7.9 Timing Requirements, $T_A = -55^\circ\text{C}$ to 125°C

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | V_{CC} | SN54HC164 | | | RECOMMENDED SN74HC164 | | | UNIT |
|--------------------|--------------------------------------|----------|-----------|-----|-----|--------------------------|-----|-----|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| f_{clock} | Clock frequency | 2 V | | | 4.2 | | | 4.2 | MHz |
| | | 4.5 V | | | 21 | | | 21 | |
| | | 6 V | | | 25 | | | 25 | |
| t_w | $\overline{\text{CLR}}$ low | 2 V | 150 | | | 125 | | | ns |
| | | 4.5 V | 30 | | | 25 | | | |
| | | 6 V | 25 | | | 21 | | | |
| | CLK high or low | 2 V | 120 | | | 120 | | | |
| | | 4.5 V | 24 | | | 24 | | | |
| | | 6 V | 20 | | | 20 | | | |
| t_{su} | Data | 2 V | 150 | | | 125 | | | ns |
| | | 4.5 V | 30 | | | 25 | | | |
| | | 6 V | 25 | | | 25 | | | |
| | $\overline{\text{CLR}}$ inactive | 2 V | 150 | | | 125 | | | |
| | | 4.5 V | 30 | | | 25 | | | |
| | | 6 V | 25 | | | 25 | | | |
| t_h | Hold time, data after CLK \uparrow | 2 V | 5 | | | 5 | | | ns |
| | | 4.5 V | 5 | | | 5 | | | |
| | | 6 V | 5 | | | 5 | | | |

7.10 Timing Requirements, $T_A = -55^\circ\text{C}$ to 85°C

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | V_{CC} | SN74HC164 | | | UNIT |
|--------------------|--------------------------------------|----------|-----------|-----|-----|------|
| | | | MIN | NOM | MAX | |
| f_{clock} | Clock frequency | 2 V | | | 5 | MHz |
| | | 4.5 V | | | 25 | |
| | | 6 V | | | 28 | |
| t_w | $\overline{\text{CLR}}$ low | 2 V | 125 | | | ns |
| | | 4.5 V | 25 | | | |
| | | 6 V | 21 | | | |
| | CLK high or low | 2 V | 100 | | | |
| | | 4.5 V | 20 | | | |
| | | 6 V | 18 | | | |
| t_{su} | Data | 2 V | 125 | | | ns |
| | | 4.5 V | 25 | | | |
| | | 6 V | 21 | | | |
| | $\overline{\text{CLR}}$ inactive | 2 V | 125 | | | |
| | | 4.5 V | 25 | | | |
| | | 6 V | 21 | | | |
| t_h | Hold time, data after CLK \uparrow | 2 V | 5 | | | ns |
| | | 4.5 V | 5 | | | |
| | | 6 V | 5 | | | |

SN54HC164, SN74HC164

SCLS115G –DECEMBER 1982–REVISED SEPTEMBER 2015

www.ti.com
7.11 Switching Characteristics, $T_A = 25^\circ\text{C}$

over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------|-------------|----------|-----|-----|-----|------|
| f_{max} | | | 2 V | 6 | 10 | | MHz |
| | | | 4.5 V | 31 | 54 | | |
| | | | 6 V | 36 | 62 | | |
| t_{PHL} | \overline{CLR} | Any Q | 2 V | | 140 | 205 | ns |
| | | | 4.5 V | | 28 | 41 | |
| | | | 6 V | | 24 | 35 | |
| t_{pd} | CLK | Any Q | 2 V | | 115 | 175 | |
| | | | 4.5 V | | 23 | 35 | |
| | | | 6 V | | 20 | 30 | |
| t_t | | | 2 V | | 38 | 75 | ns |
| | | | 4.5 V | | 8 | 15 | |
| | | | 6 V | | 6 | 13 | |

7.12 Switching Characteristics, $T_A = -55^\circ\text{C}$ to 125°C

over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Figure 3](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN54HC164 | | | RECOMMENDED SN74HC164 | | | UNIT |
|-----------|------------------|-------------|----------|-----------|-----|-----|-----------------------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | | | 2 V | 4.2 | | | 4.2 | | | MHz |
| | | | 4.5 V | 21 | | | 21 | | | |
| | | | 6 V | 25 | | | 25 | | | |
| t_{PHL} | \overline{CLR} | Any Q | 2 V | | | 295 | | | 255 | ns |
| | | | 4.5 V | | | 59 | | | 51 | |
| | | | 6 V | | | 51 | | | 46 | |
| t_{pd} | CLK | Any Q | 2 V | | | 265 | | | 220 | |
| | | | 4.5 V | | | 53 | | | 44 | |
| | | | 6 V | | | 45 | | | 38 | |
| t_t | | | 2 V | | | 110 | | | 110 | ns |
| | | | 4.5 V | | | 22 | | | 22 | |
| | | | 6 V | | | 19 | | | 19 | |

7.13 Switching Characteristics, $T_A = -55^\circ\text{C}$ to 85°C

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN74HC164 | | | UNIT |
|-----------|------------------|-------------|----------|-----------|-----|-----|------|
| | | | | MIN | TYP | MAX | |
| f_{max} | | | 2 V | 5 | | | MHz |
| | | | 4.5 V | 25 | | | |
| | | | 6 V | 28 | | | |
| t_{PHL} | \overline{CLR} | Any Q | 2 V | | | 255 | ns |
| | | | 4.5 V | | | 51 | |
| | | | 6 V | | | 46 | |
| t_{pd} | CLK | Any Q | 2 V | | | 220 | |
| | | | 4.5 V | | | 44 | |
| | | | 6 V | | | 38 | |
| t_t | | | 2 V | | | 95 | ns |
| | | | 4.5 V | | | 19 | |
| | | | 6 V | | | 16 | |

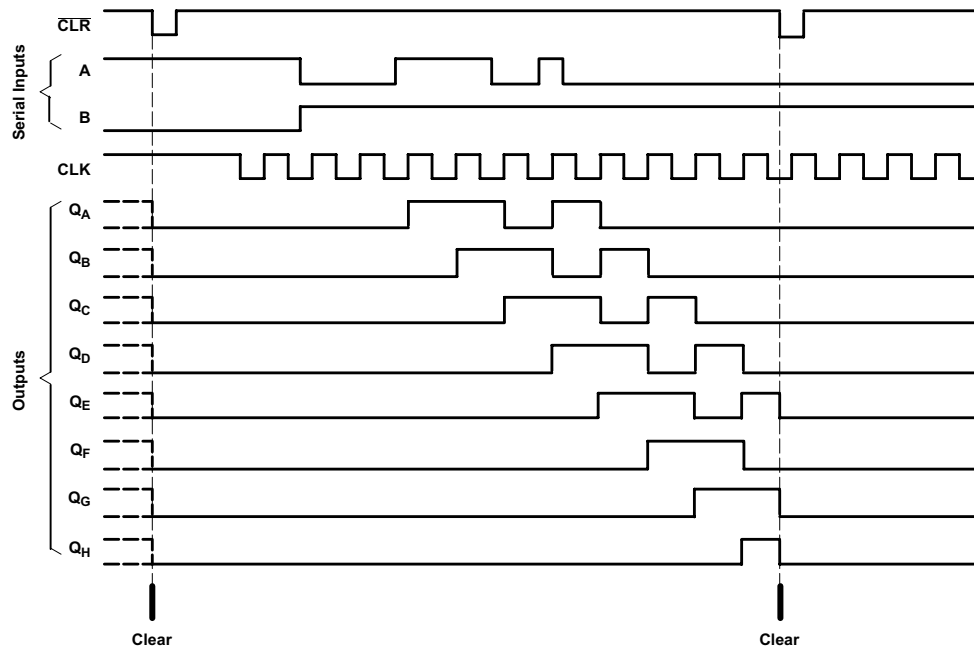
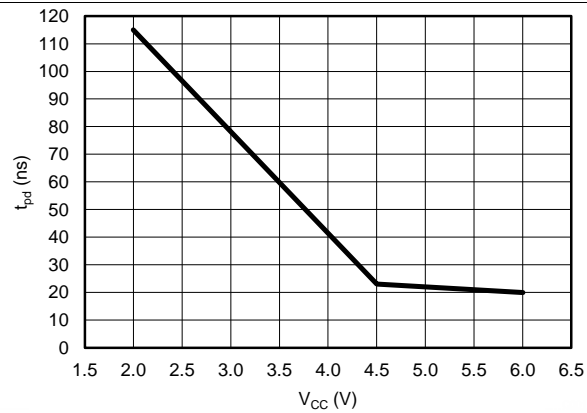


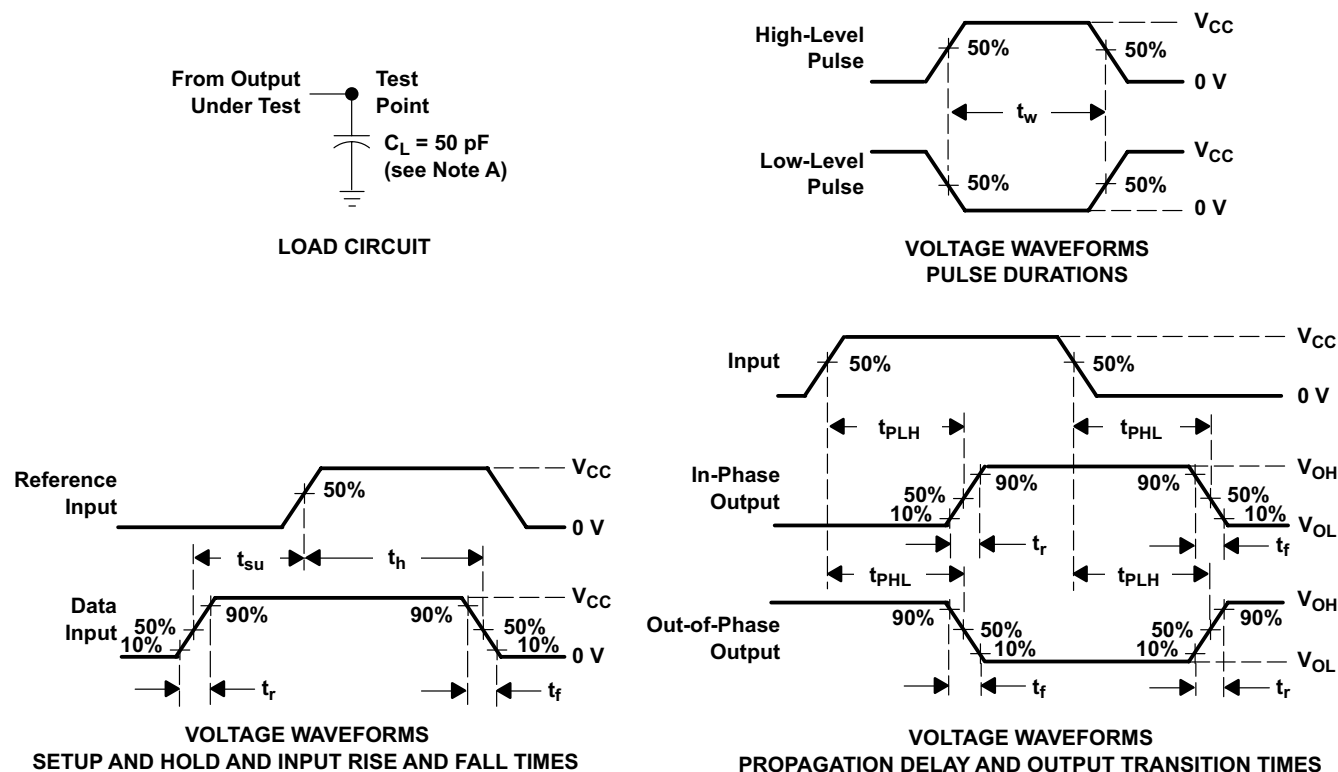
Figure 1. SN74HC164 Example Timing Diagram

SN54HC164, SN74HC164

SCLS115G –DECEMBER 1982–REVISED SEPTEMBER 2015

www.ti.com
7.14 Typical Characteristics
 $T_A = 25^\circ\text{C}$

Figure 2. Propagation Delay vs Supply Voltage at $T_A = 25^\circ\text{C}$

8 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

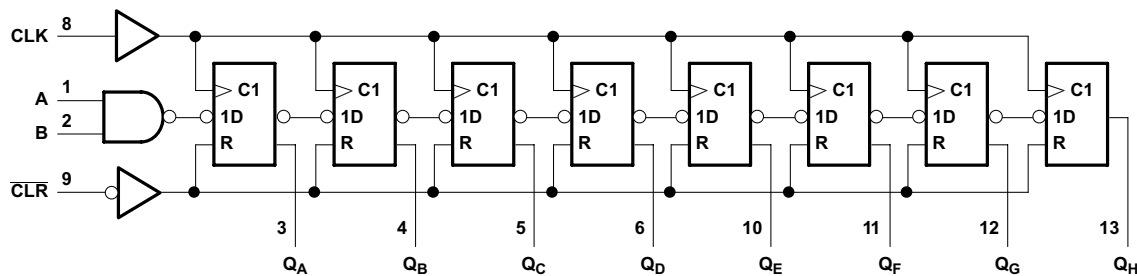
9 Detailed Description

9.1 Overview

The SN74HC164 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear (CLR). The device requires a high signal on both A and B in order to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the SN74HC164 is triggered on a positive or rising-edge signal, from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the ($A \bullet B$) input data line in the first register and propagate each register's data to the next register. The data of the last register, Q_H, will be discarded at each clock trigger. If a low signal is applied to the CLR pin of the SN74HC164, the device will set all registers to a value of 0 immediately.

9.2 Functional Block Diagram



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

9.3 Feature Description

The HC164 has a wide operating voltage range of 2 V to 6 V, outputs that can drive up to 10 LSTTL loads and Low Power Consumption, 80-μA maximum I. It is typically $t_{pd} = 20$ ns and has ± 4 -mA output drive at 5 V with low input current of 1-μA maximum. It also has AND-gated (enable/disable) serial inputs a fully buffered clock and serial inputs as well as a direct clear.

9.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC164.

Table 1. Function Table⁽¹⁾⁽²⁾

| INPUTS | | | | OUTPUTS | | | |
|-------------------------|-----|---|---|-----------------|-----------------|-----|-----------------|
| $\overline{\text{CLR}}$ | CLK | A | B | Q _A | Q _B | ... | Q _H |
| L | X | X | X | L | L | | L |
| H | L | X | X | Q _{A0} | Q _{B0} | | Q _{H0} |
| H | ↑ | H | H | H | Q _{An} | | Q _{Gn} |
| H | ↑ | L | X | L | Q _{An} | | Q _{Gn} |
| H | ↑ | X | L | L | Q _{An} | | Q _{Gn} |

- (1) Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
- (2) Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of CLK: Indicates a 1-bit shift.

10 Application and Implementation

10.1 Application Information

The SNx4HC164 is an 8-bit shift register that can be used as a deserializer in order to reduce the number of GPIO's needed when driving multiple LED's. In order to correctly display the proper output in the LED's a sink MOSFET was added to prevent the LED's from lighting up until the correct data or the proper clock signal has been achieved.

10.2 Typical Application

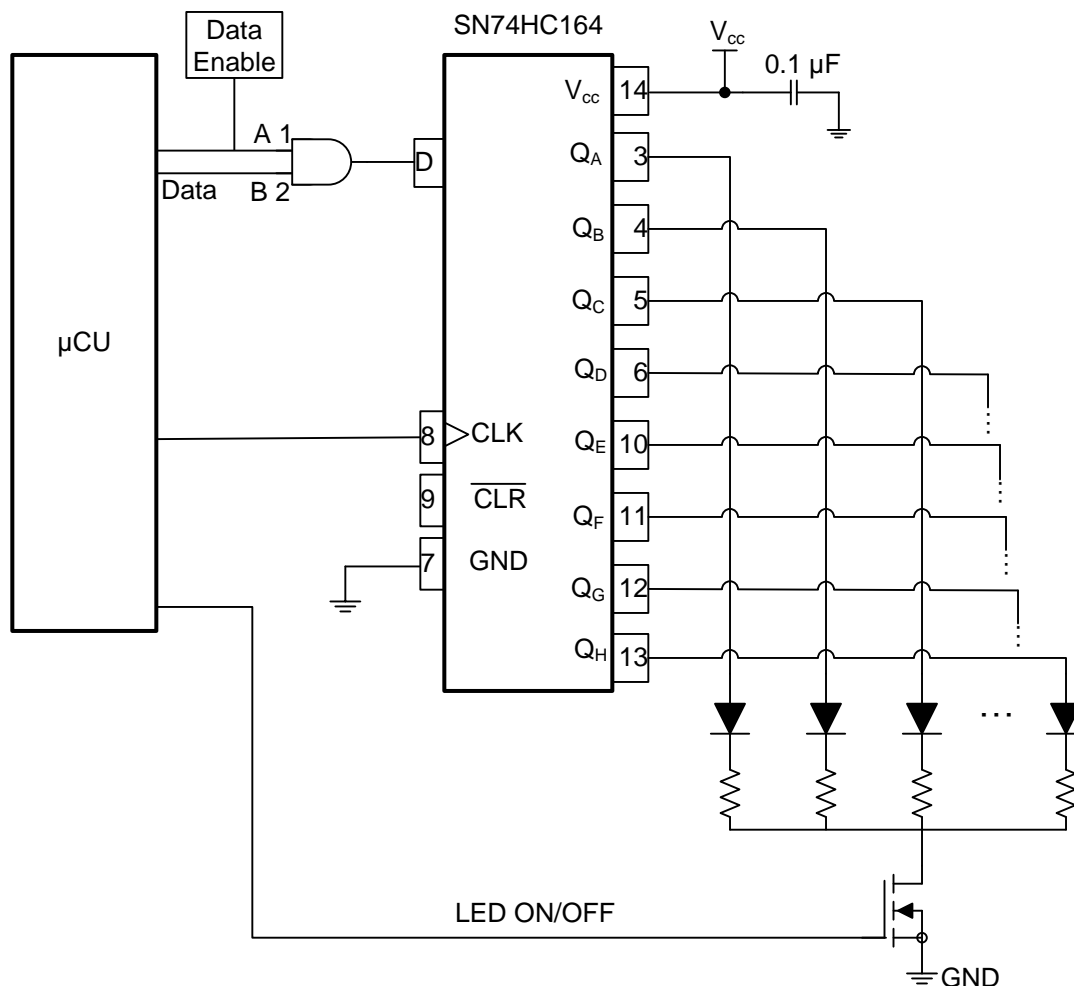


Figure 4. Typical Application Diagram

10.2.1 Design Requirements

Ensure that the incoming clock rising edge meets the criteria in [Recommended Operating Conditions](#).

10.2.2 Detailed Design Procedure

Ensure that input and output voltages do not exceed ratings in [Absolute Maximum Ratings](#).

Input voltage threshold information can be found in [Recommended Operating Conditions](#).

Detailed timing requirements can be found in [Timing Requirements](#), $T_A = 25^\circ\text{C}$.

Typical Application (continued)

10.2.3 Application Curve

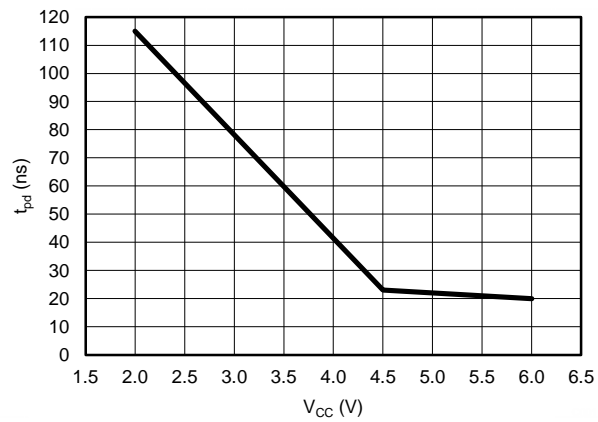


Figure 5. Propagation Delay vs Supply Voltage at T_A = 25°C

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin must have a good bypass capacitor in order to prevent power disturbance. For devices with a single supply, a 0.1- μF capacitor is recommended and if there are multiple V_{CC} pins then a 0.01- μF or 0.022- μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. [Figure 6](#) shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

12.2 Layout Example

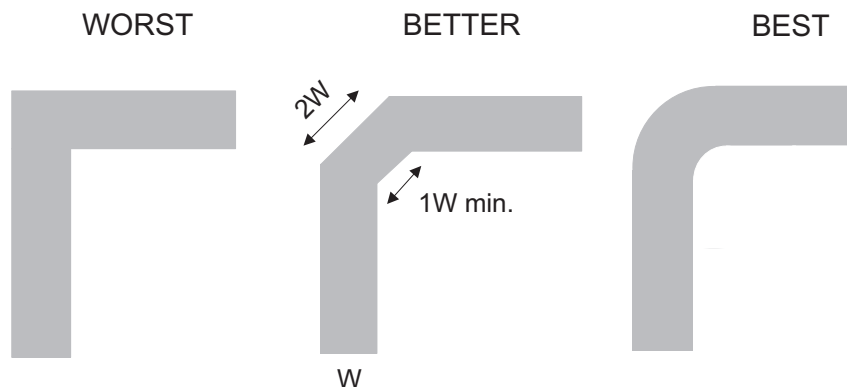


Figure 6. Trace Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54HC164 | Click here | Click here | Click here | Click here | Click here |
| SN74HC164 | Click here | Click here | Click here | Click here | Click here |

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------|
| 5962-8416201VCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8416201VC A SNV54HC164J |
| 5962-8416201VCA.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8416201VC A SNV54HC164J |
| 5962-8416201VDA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8416201VD A SNV54HC164W |
| 5962-8416201VDA.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8416201VD A SNV54HC164W |
| 84162012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84162012A SNJ54HC 164FK |
| 8416201CA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8416201CA SNJ54HC164J |
| SN54HC164J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC164J |
| SN54HC164J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC164J |
| SN74HC164D | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 125 | HC164 |
| SN74HC164DR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DRG3 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DRG3.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DRG4 | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DRG4.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164DT | Obsolete | Production | SOIC (D) 14 | - | - | Call TI | Call TI | -40 to 125 | HC164 |
| SN74HC164N | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74HC164N |
| SN74HC164N.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74HC164N |
| SN74HC164NE4 | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74HC164N |
| SN74HC164NE4.A | Active | Production | PDIP (N) 14 | 25 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74HC164N |
| SN74HC164NSR | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SN74HC164NSR.A | Active | Production | SOP (NS) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PW | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -40 to 125 | HC164 |
| SN74HC164PWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PWRE4 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PWRG4 | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PWRG4.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HC164 |
| SN74HC164PWT | Obsolete | Production | TSSOP (PW) 14 | - | - | Call TI | Call TI | -40 to 125 | HC164 |
| SNJ54HC164FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84162012A SNJ54HC 164FK |
| SNJ54HC164FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84162012A SNJ54HC 164FK |
| SNJ54HC164J | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8416201CA SNJ54HC164J |
| SNJ54HC164J.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8416201CA SNJ54HC164J |
| SNJ54HC164W | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8416201DA SNJ54HC164W |
| SNJ54HC164W.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8416201DA SNJ54HC164W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC164, SN54HC164-SP, SN74HC164 :

- Catalog : [SN74HC164](#), [SN54HC164](#)
- Military : [SN54HC164](#)
- Space : [SN54HC164-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC164DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC164DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC164DRG3 | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC164DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC164DRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74HC164NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74HC164NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HC164PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC164PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC164PWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

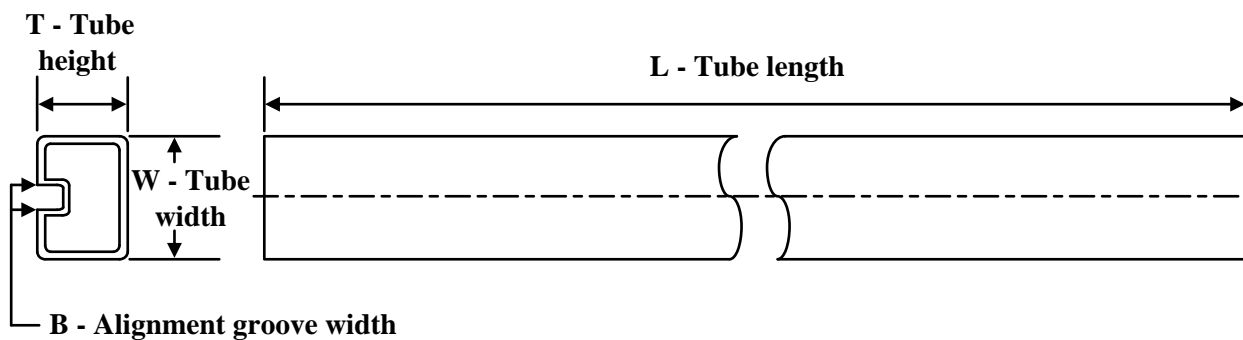
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC164DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC164DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC164DRG3 | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| SN74HC164DRG4 | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74HC164DRG4 | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74HC164NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC164NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC164PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC164PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC164PWRG4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8416201VDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-8416201VDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 84162012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74HC164N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164NE4 | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164NE4.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC164NE4.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC164FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC164FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC164W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HC164W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---------------|-------|-------|-------|-------|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J 14

GENERIC PACKAGE VIEW

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

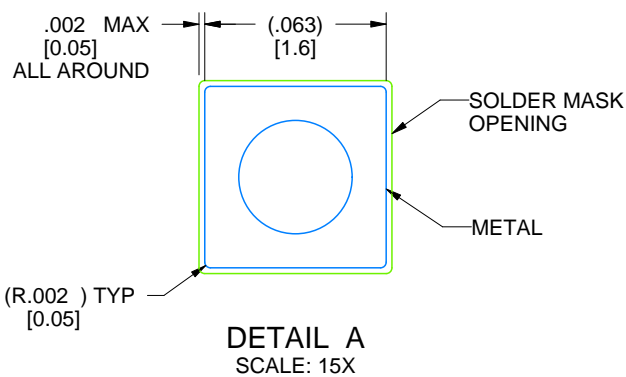
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025