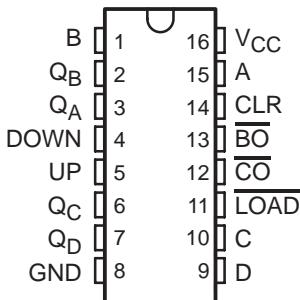


**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

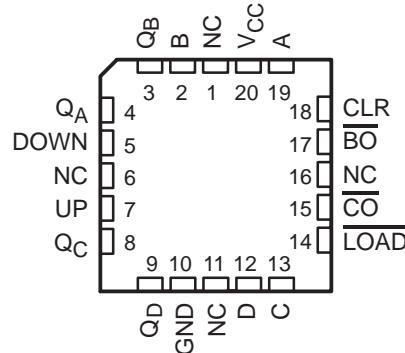
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 20$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max

SN54HC193 . . . J OR W PACKAGE  
SN74HC193 . . . D, N, NS, OR PW PACKAGE  
(TOP VIEW)



- Look-Ahead Circuitry Enhances Cascaded Counters
- Fully Synchronous in Count Modes
- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

SN54HC193 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

### description/ordering information

The 'HC193 devices are 4-bit synchronous, reversible, up/down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

### ORDERING INFORMATION

<b>T<sub>A</sub></b>	<b>PACKAGE<sup>†</sup></b>		<b>ORDERABLE PART NUMBER</b>	<b>TOP-SIDE MARKING</b>
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	PDIP - N	Tube of 25	SN74HC193N	SN74HC193N
	SOIC - D	Tube of 40	SN74HC193D	HC193
		Reel of 2500	SN74HC193DR	
		Reel of 250	SN74HC193DT	
	SOP - NS	Reel of 2000	SN74HC193NSR	HC193
	TSSOP - PW	Tube of 90	SN74HC193PW	HC193
		Reel of 2000	SN74HC193PWR	
		Reel of 250	SN74HC193PWT	
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	CDIP - J	Tube of 25	SNJ54HC193J	SNJ54HC193J
	CFP - W	Tube of 150	SNJ54HC193W	SNJ54HC193W
	LCCC - FK	Tube of 55	SNJ54HC193FK	SNJ54HC193FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54HC193, SN74HC193  
4-BIT SYNCHRONOUS UP/DOWN COUNTERS  
(DUAL CLOCK WITH CLEAR)**

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**description/ordering information (continued)**

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count (clock) input (UP or DOWN). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load (LOAD) input and entering the desired data at the data inputs. The output changes to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers simply by modifying the count length with the preset inputs.

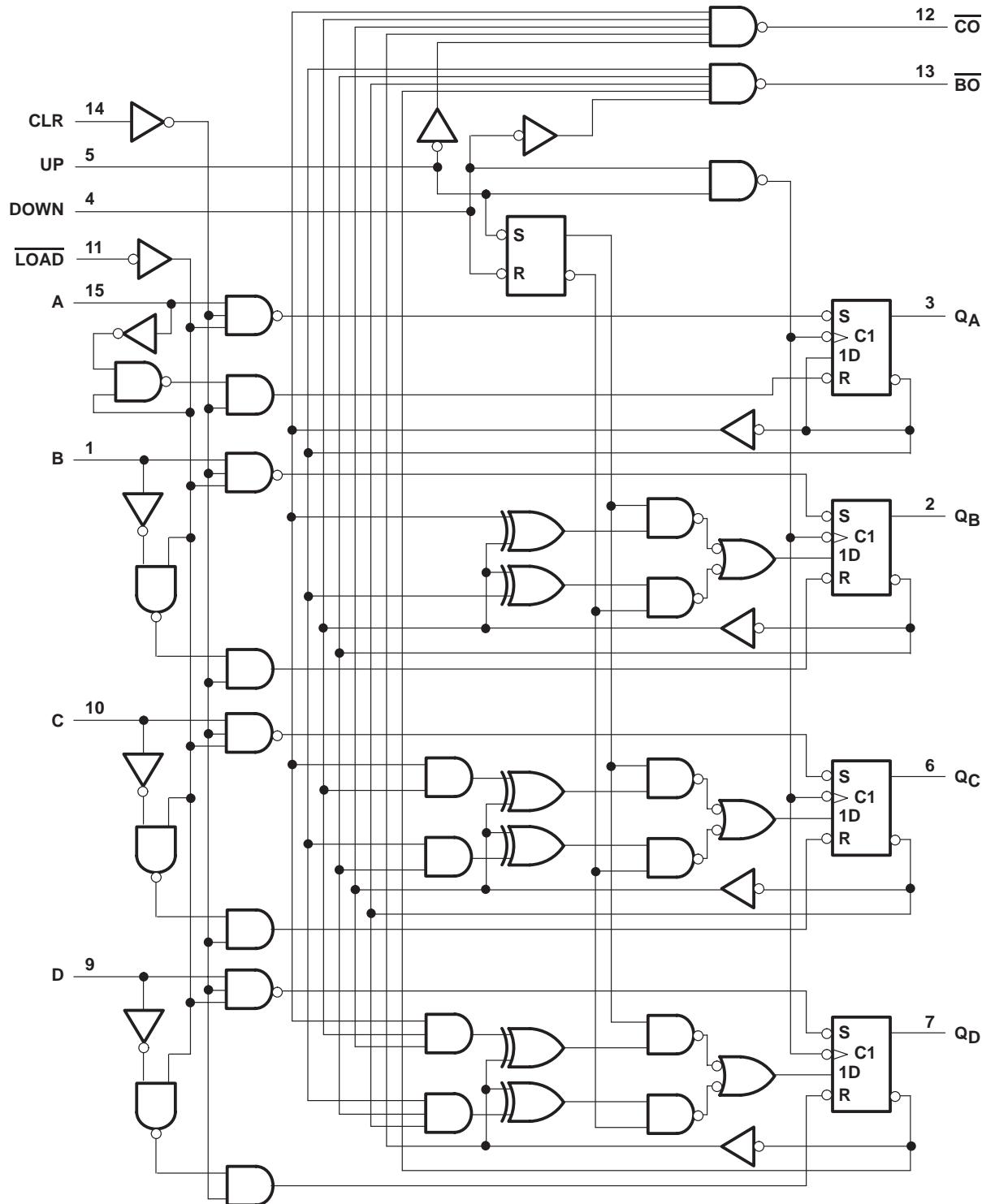
A clear (CLR) input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and LOAD inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow ( $\overline{BO}$ ) output produces a low-level pulse while the count is zero (all outputs low) and DOWN is low. Similarly, the carry ( $\overline{CO}$ ) output produces a low-level pulse while the count is maximum (9 or 15), and UP is low. The counters then can be cascaded easily by feeding  $\overline{BO}$  and  $\overline{CO}$  to DOWN and UP, respectively, of the succeeding counter.



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logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

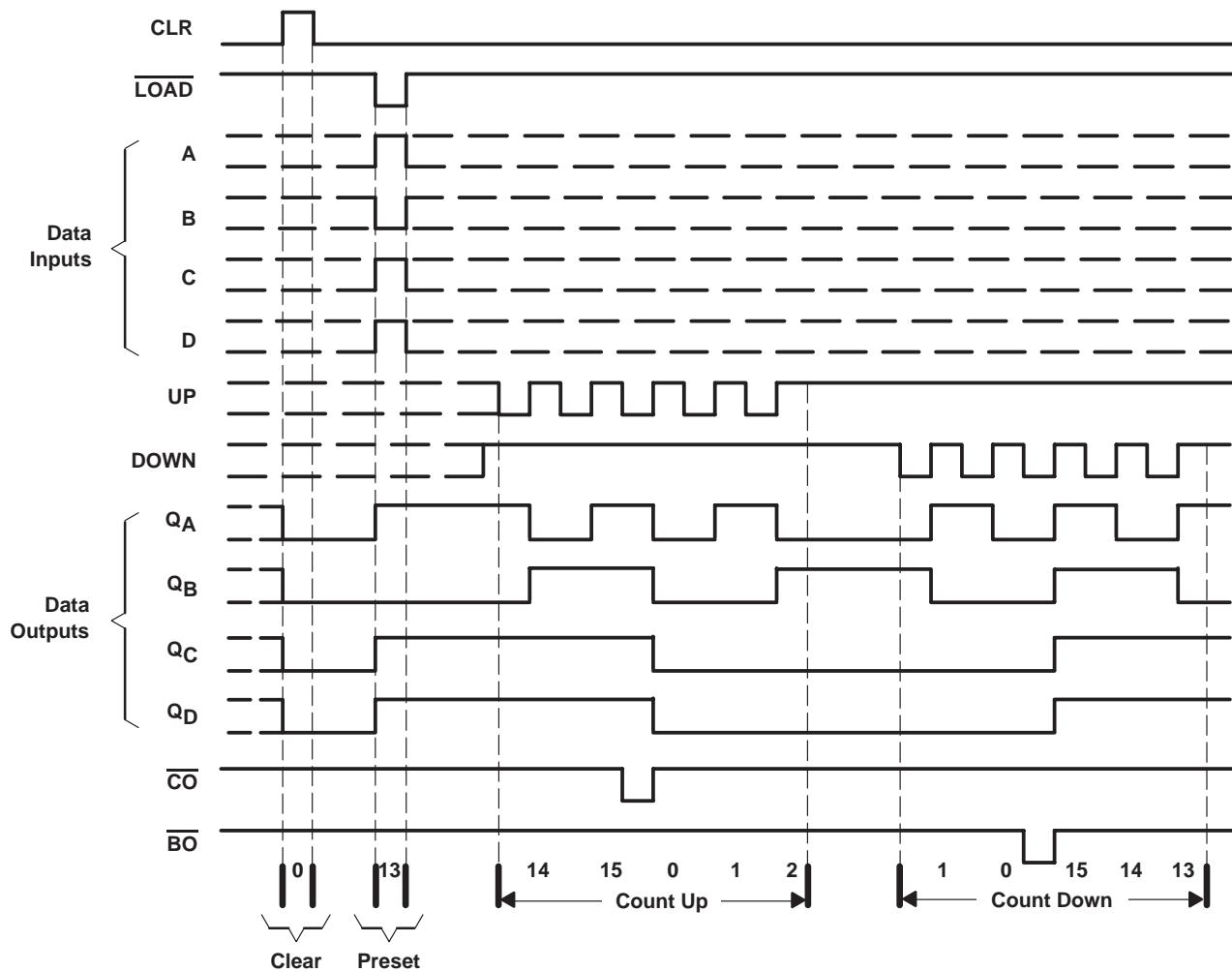
**SN54HC193, SN74HC193  
4-BIT SYNCHRONOUS UP/DOWN COUNTERS  
(DUAL CLOCK WITH CLEAR)**

SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

**typical clear, load, and count sequence**

The following sequence is illustrated below:

1. Clear outputs to 0
2. Load (preset) to binary 13
3. Count up to 14, 15, carry, 0, 1, and 2
4. Count down to 1, 0, borrow, 15, 14, and 13



NOTES: A. CLR overrides LOAD, data, and count inputs.  
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 3)**

		SN54HC193			SN74HC193			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5			V
		V <sub>CC</sub> = 4.5 V	3.15		3.15			
		V <sub>CC</sub> = 6 V	4.2		4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5		V
		V <sub>CC</sub> = 4.5 V		1.35		1.35		
		V <sub>CC</sub> = 6 V		1.8		1.8		
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
Δt/Δv <sup>†</sup>	Input transition rise/fall time	V <sub>CC</sub> = 2 V		1000		1000		ns
		V <sub>CC</sub> = 4.5 V		500		500		
		V <sub>CC</sub> = 6 V		400		400		
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	-	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

‡ If this device is used in the threshold region (from  $V_{IL\max} = 0.5\text{ V}$  to  $V_{IH\min} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_f = 1000\text{ ns}$  and  $VCC = 2\text{ V}$  does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC193	SN74HC193	UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 µA	2 V	1.9	1.998	1.9	1.9	V
			4.5 V	4.4	4.499	4.4	4.4	
			6 V	5.9	5.999	5.9	5.9	
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7	3.84	
		I <sub>OH</sub> = -5.2 mA	6 V	5.48	5.8	5.2	5.34	
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 µA	2 V	0.002	0.1	0.1	0.1	V
			4.5 V	0.001	0.1	0.1	0.1	
			6 V	0.001	0.1	0.1	0.1	
		I <sub>OL</sub> = 4 mA	4.5 V	0.17	0.26	0.4	0.33	
		I <sub>OL</sub> = 5.2 mA	6 V	0.15	0.26	0.4	0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1	±100		±1000	±1000	nA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8	160	80	µA
C <sub>i</sub>		2 V to 6 V		3	10	10	10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC193	SN74HC193	UNIT
			MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	4.2		2.8	3.3	MHz
		4.5 V	21		14	17	
		6 V	24		16	19	
t <sub>w</sub>	Pulse duration	CLR high	2 V	120	180	150	ns
			4.5 V	24	36	30	
			6 V	21	31	26	
	LOAD low		2 V	120	180	150	
			4.5 V	24	36	30	
			6 V	21	31	26	
	UP or DOWN high or low		2 V	120	180	150	
			4.5 V	24	36	30	
			6 V	21	31	26	
t <sub>su</sub>	Setup time	Data before LOAD inactive	2 V	110	165	140	ns
			4.5 V	22	33	28	
			6 V	19	28	24	
	CLR inactive before UP↑ or DOWN↑		2 V	110	165	140	
			4.5 V	22	33	28	
			6 V	19	28	24	
	LOAD inactive before UP↑ or DOWN↑		2 V	110	165	140	
			4.5 V	22	33	28	
			6 V	19	28	24	
t <sub>h</sub>	Hold time	Data after LOAD inactive	2 V	5	5	5	ns
			4.5 V	5	5	5	
			6 V	5	5	5	

SN54HC193, SN74HC193  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**  
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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC193	SN74HC193	UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{max}$			2 V	4.2	8		2.8	3.3	MHz
			4.5 V	21	55		14	17	
			6 V	24	60		16	19	
$t_{pd}$	UP	$\overline{CO}$	2 V	75	165		250	205	ns
			4.5 V	24	33		50	41	
			6 V	20	28		43	35	
	DOWN	$\overline{BO}$	2 V	75	165		250	205	
			4.5 V	24	33		50	41	
			6 V	20	28		43	35	
	UP or DOWN	Any Q	2 V	190	250		375	315	
			4.5 V	40	50		75	63	
			6 V	35	43		64	54	
	$\overline{LOAD}$	Any Q	2 V	190	260		390	325	
			4.5 V	40	52		78	65	
			6 V	35	44		66	55	
$t_{PHL}$	CLR	Any Q	2 V	170	240		360	300	ns
			4.5 V	36	48		72	60	
			6 V	31	41		61	51	
$t_t$		Any	2 V	38	75		110	95	ns
			4.5 V	8	15		22	19	
			6 V	6	13		19	16	

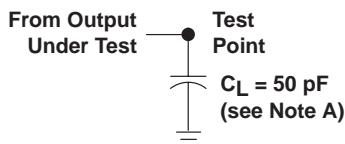
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load	50	pF

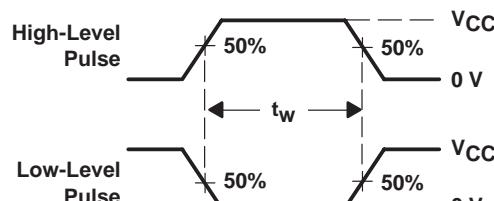
**SN54HC193, SN74HC193**  
**4-BIT SYNCHRONOUS UP/DOWN COUNTERS**  
**(DUAL CLOCK WITH CLEAR)**

SCLS122D - DECEMBER 1982 - REVISED OCTOBER 2003

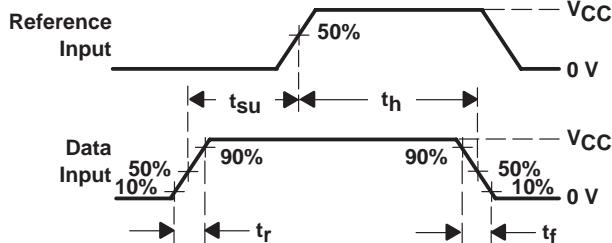
**PARAMETER MEASUREMENT INFORMATION**



LOAD CIRCUIT

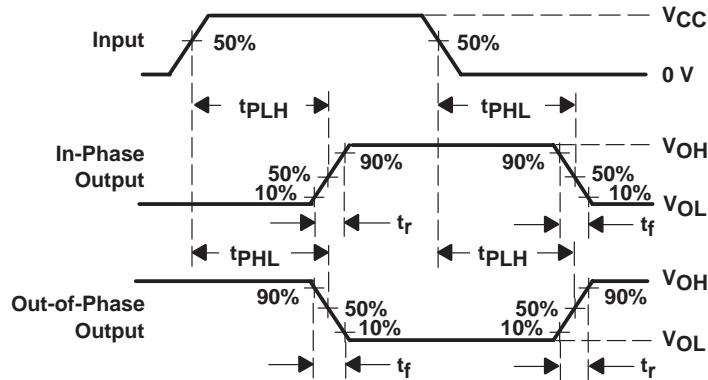


VOLTAGE WAVEFORMS  
PULSE DURATIONS



VOLTAGE WAVEFORMS

SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES:

- $C_L$  includes probe and test-fixture capacitance.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- For clock inputs,  $f_{\text{max}}$  is measured when the input duty cycle is 50%.
- The outputs are measured one at a time with one input transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8772401EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J
SN54HC193J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC193J
SN54HC193J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54HC193J
SN74HC193D	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	-40 to 85	HC193
SN74HC193DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193NE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN74HC193N
SN74HC193NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193PW	Obsolete	Production	TSSOP (PW)   16	-	-	Call TI	Call TI	-40 to 85	HC193
SN74HC193PWR	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SN74HC193PWR.A	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC193
SNJ54HC193J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J
SNJ54HC193J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8772401EA SNJ54HC193J

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

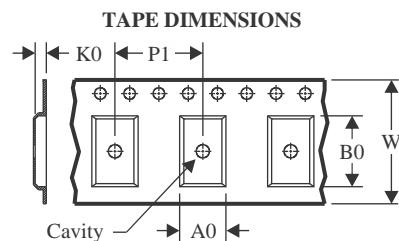
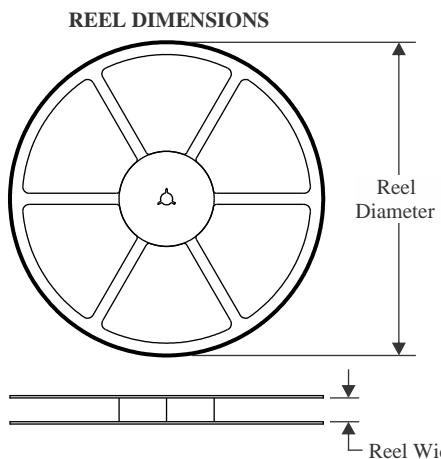
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC193, SN74HC193 :**

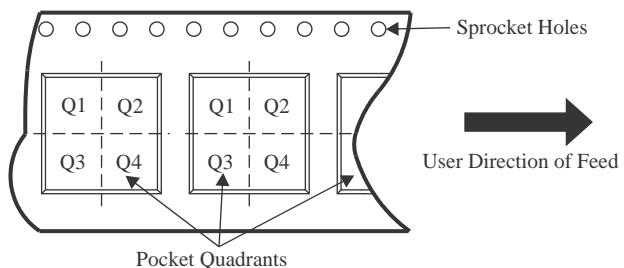
- Catalog : [SN74HC193](#)
- Automotive : [SN74HC193-Q1](#), [SN74HC193-Q1](#)
- Military : [SN54HC193](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

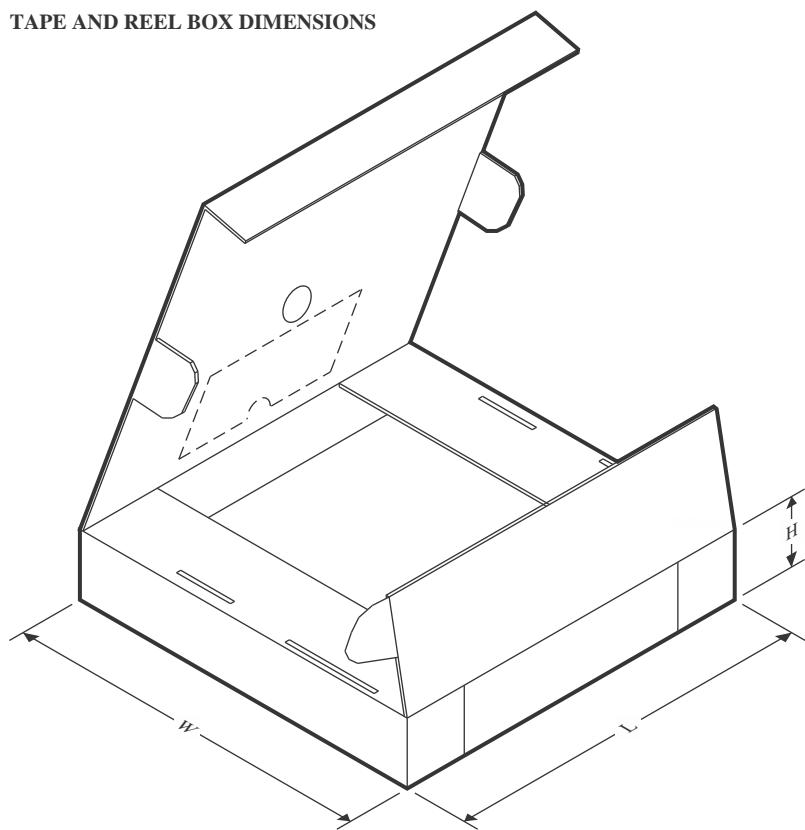
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


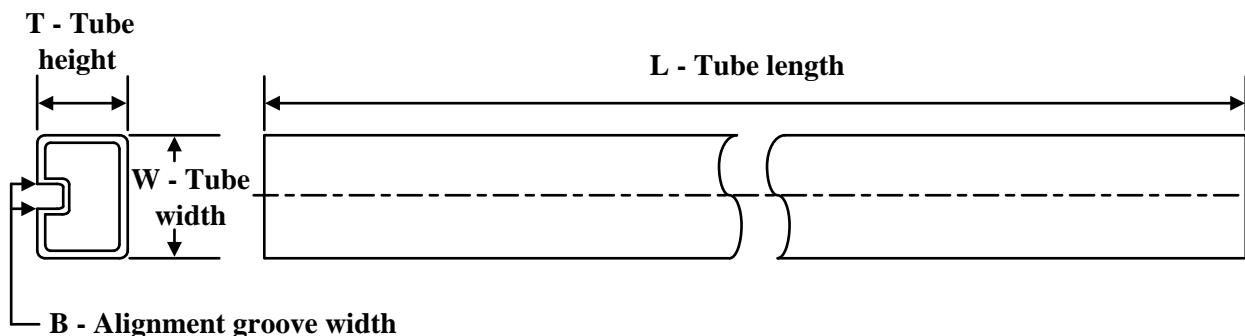
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC193DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC193NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74HC193PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC193DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74HC193NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74HC193PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

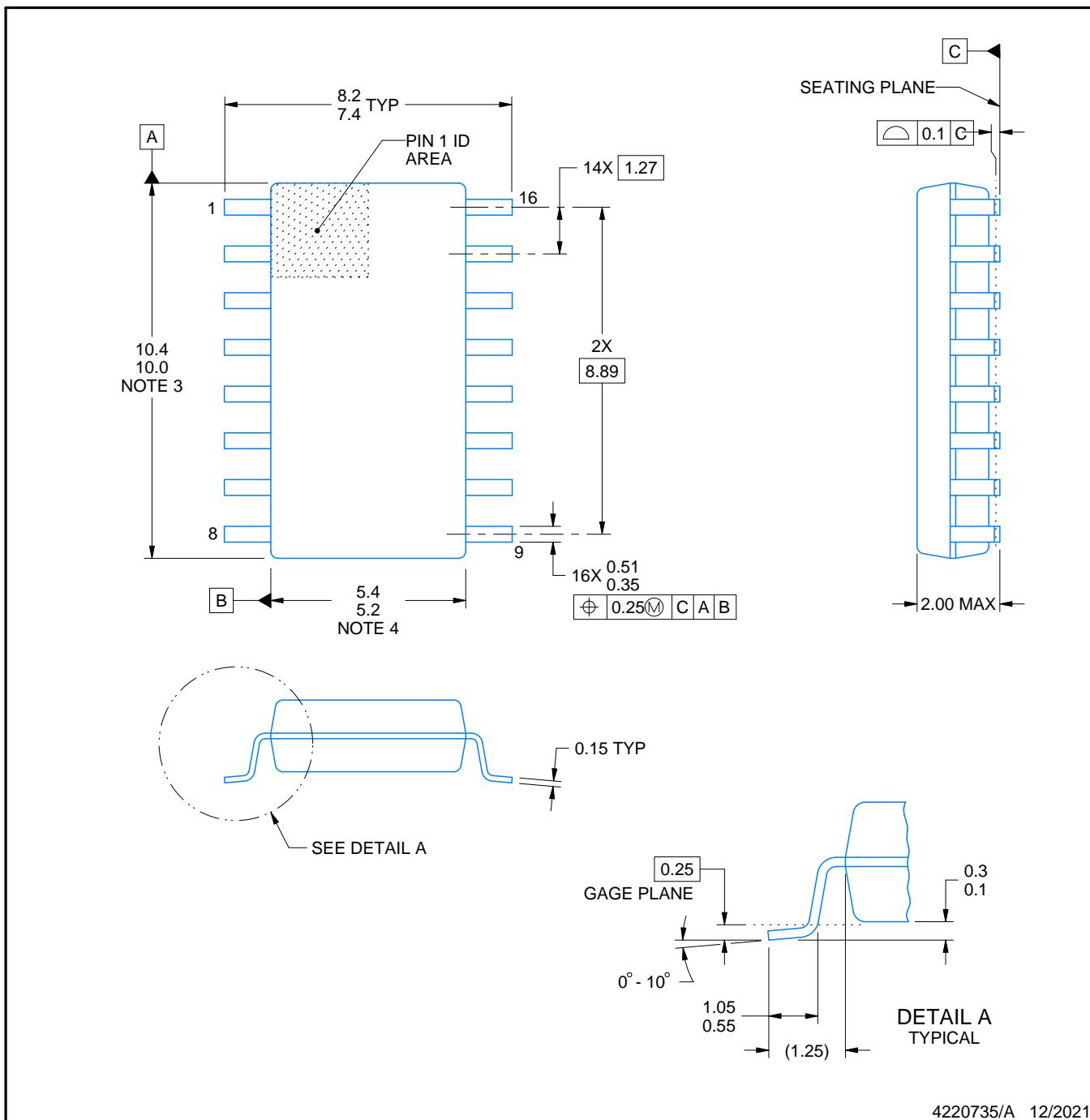
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
SN74HC193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74HC193NE4	N	PDIP	16	25	506	13.97	11230	4.32



# PACKAGE OUTLINE

## SOP - 2.00 mm max height

SOP



4220735/A 12/2021

### NOTES:

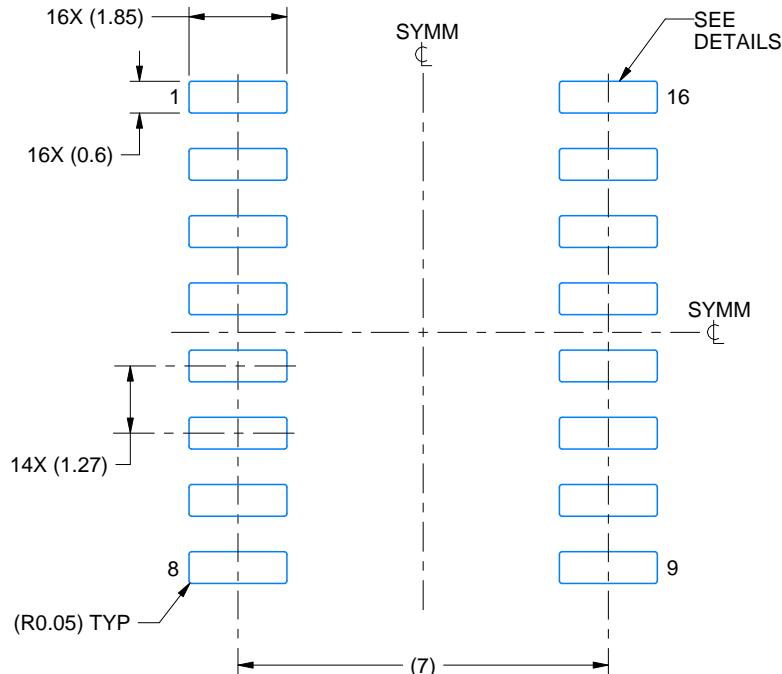
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

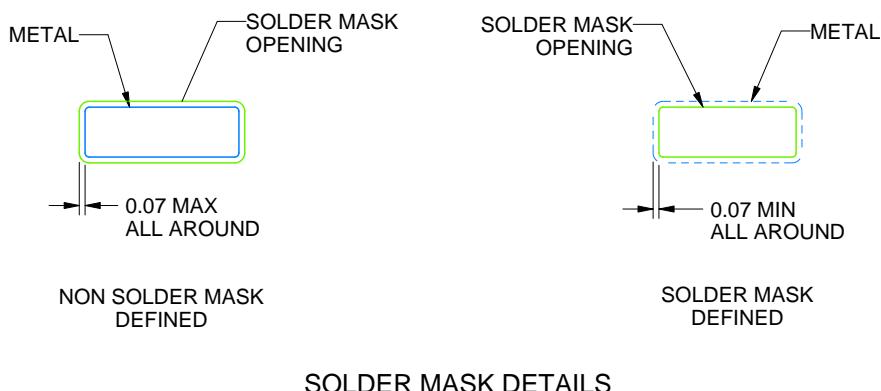
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

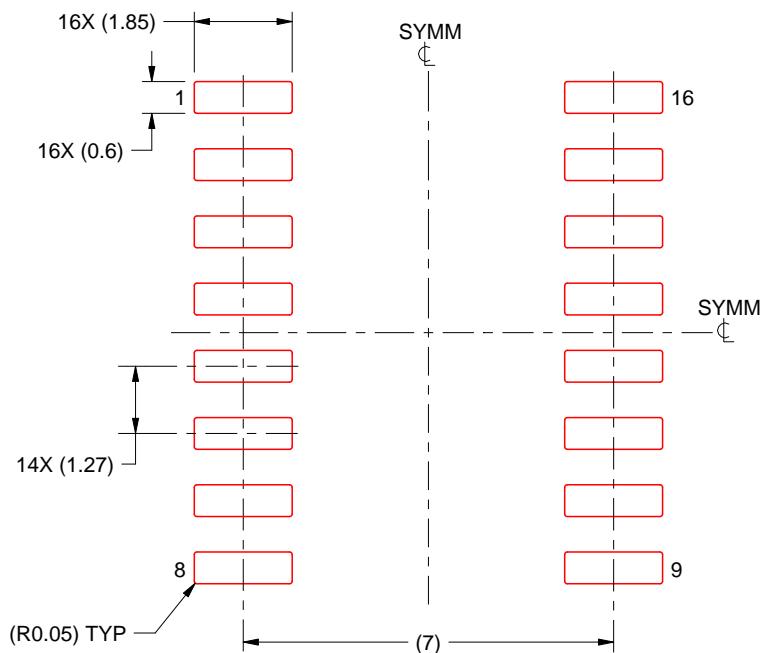
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

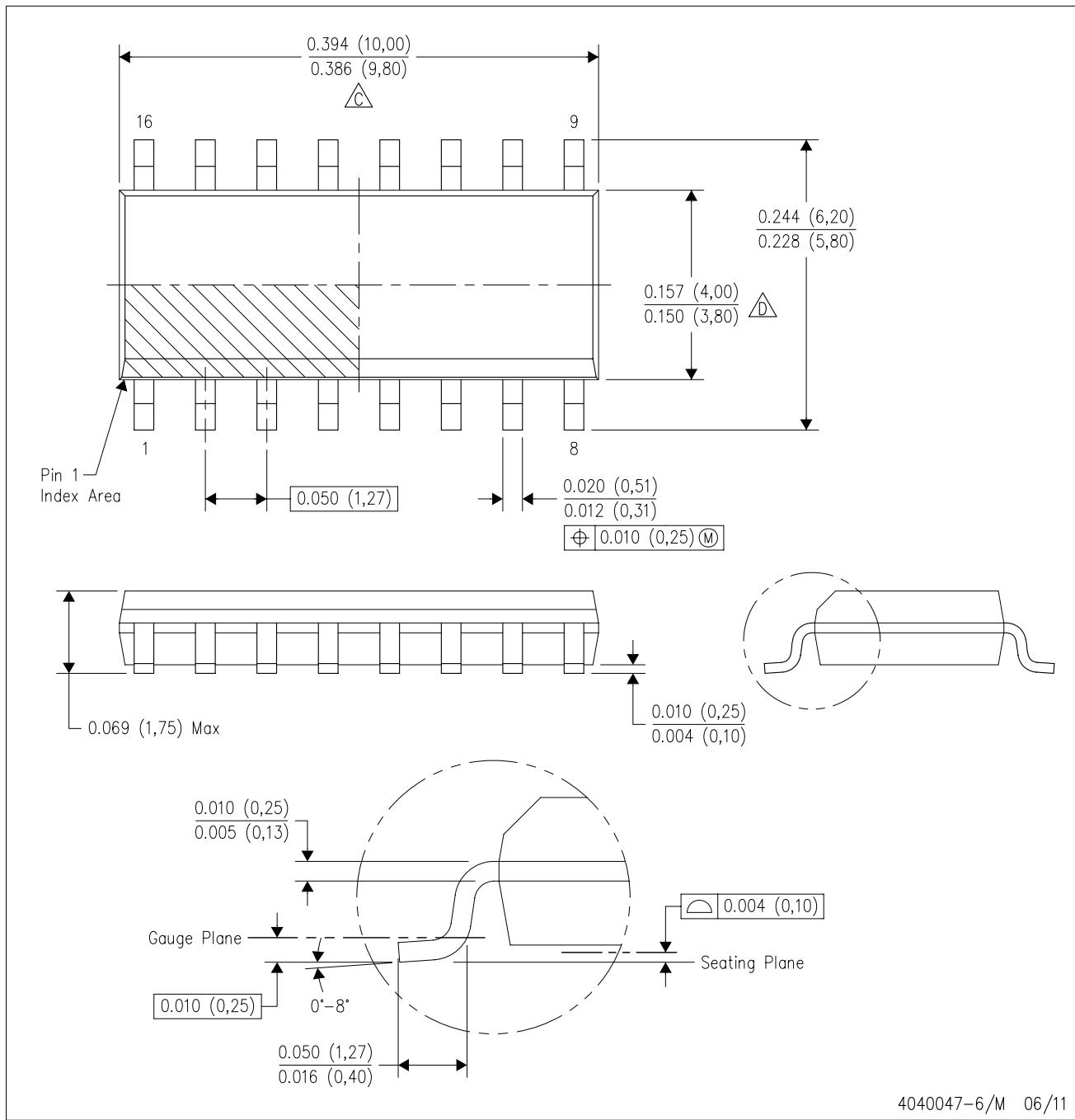
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

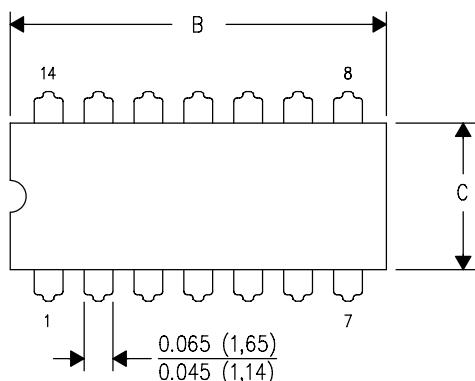
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

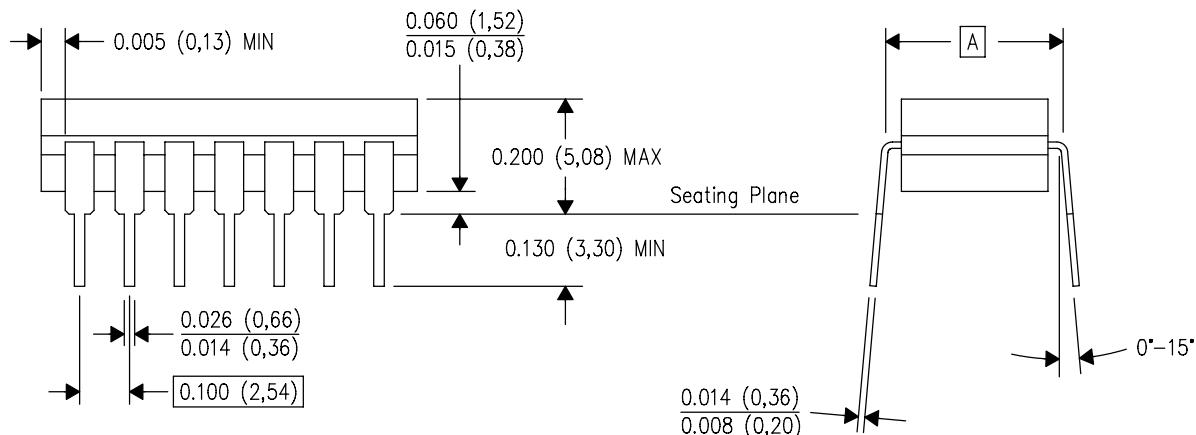
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

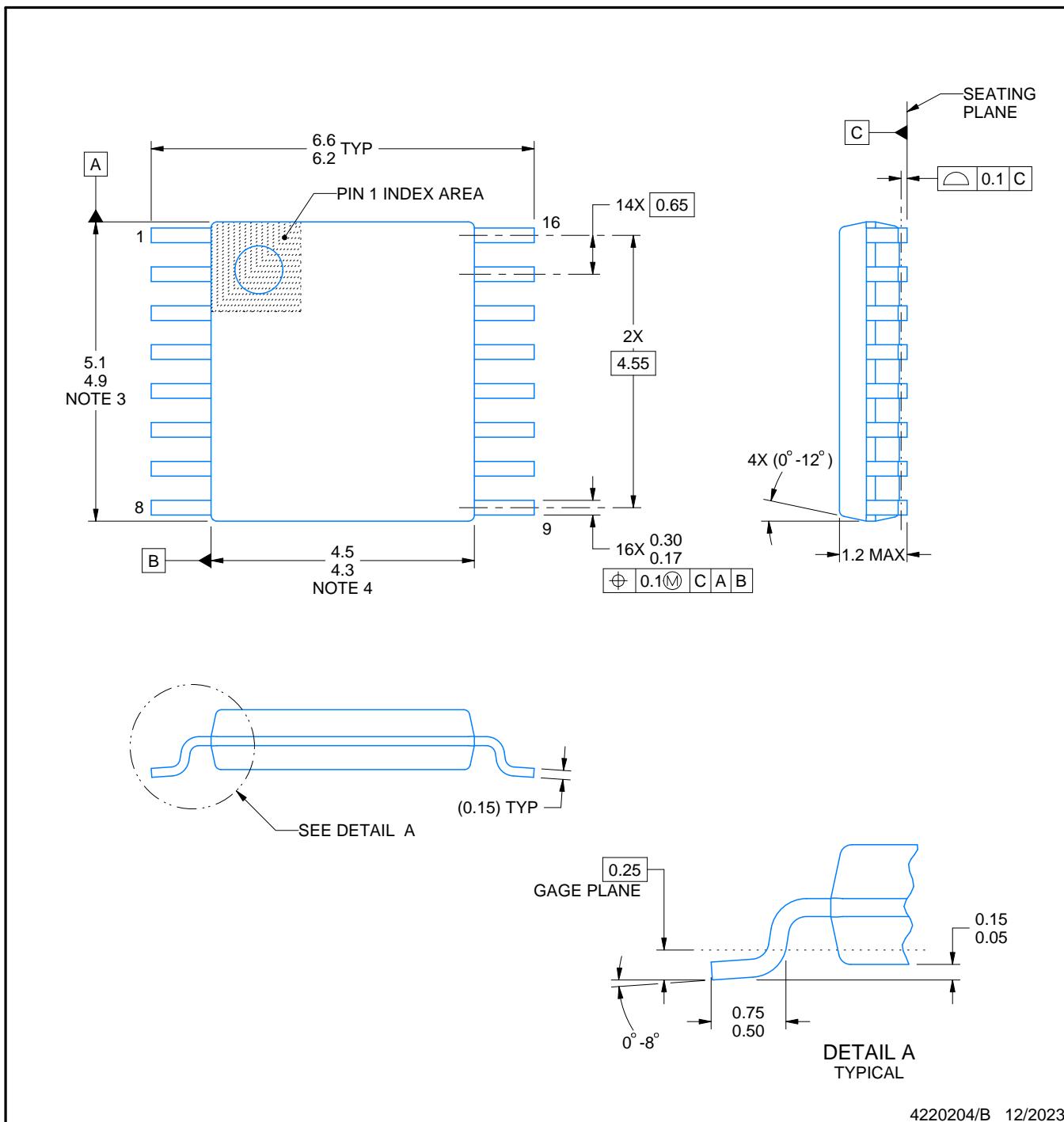
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

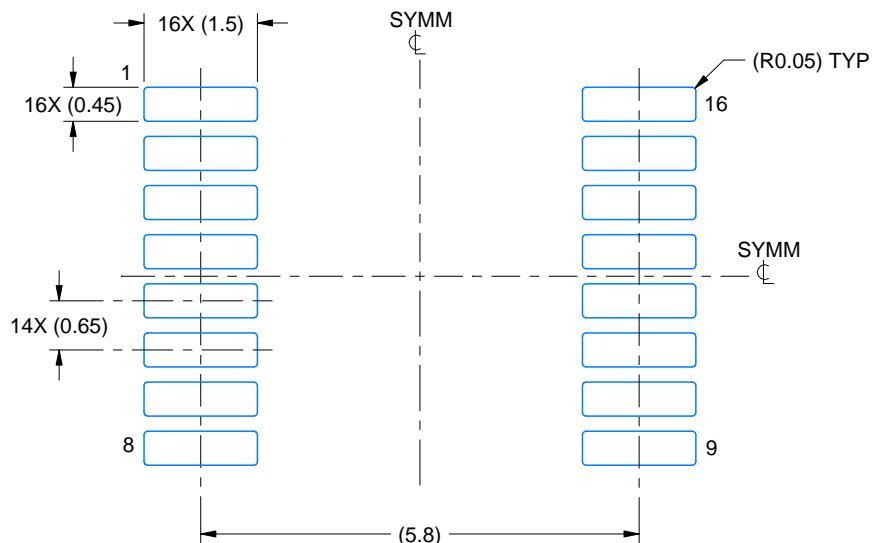
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

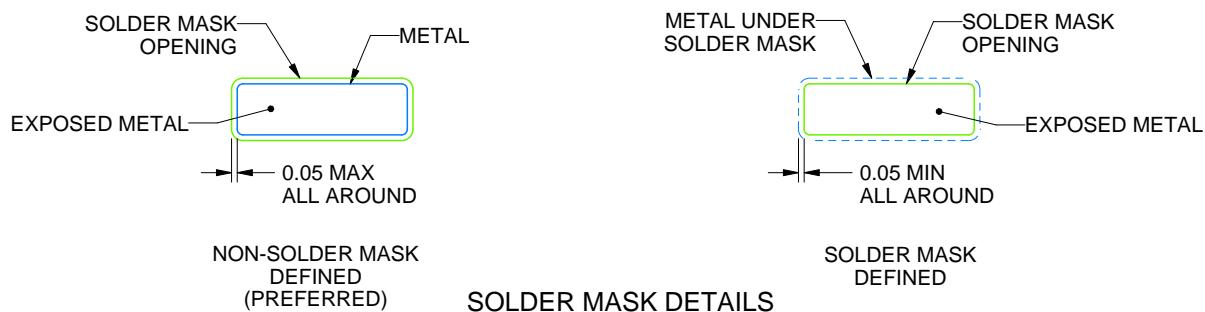
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

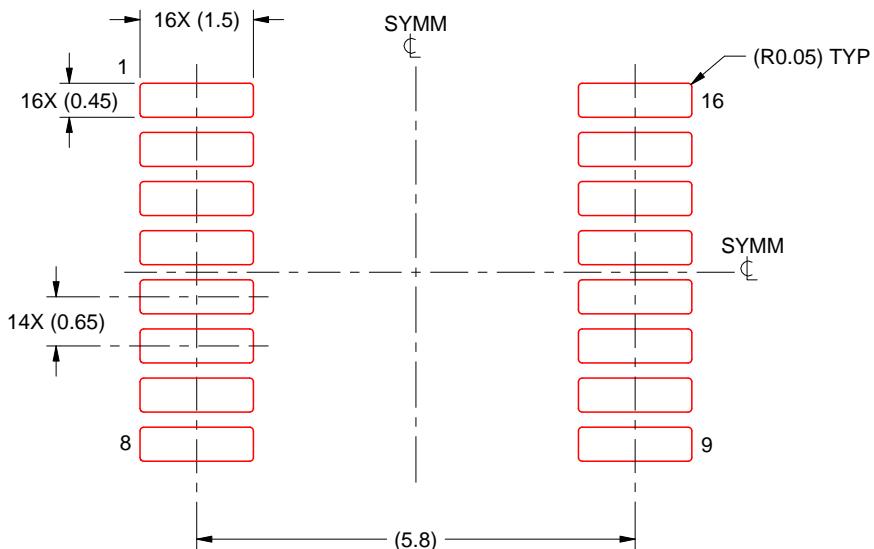
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

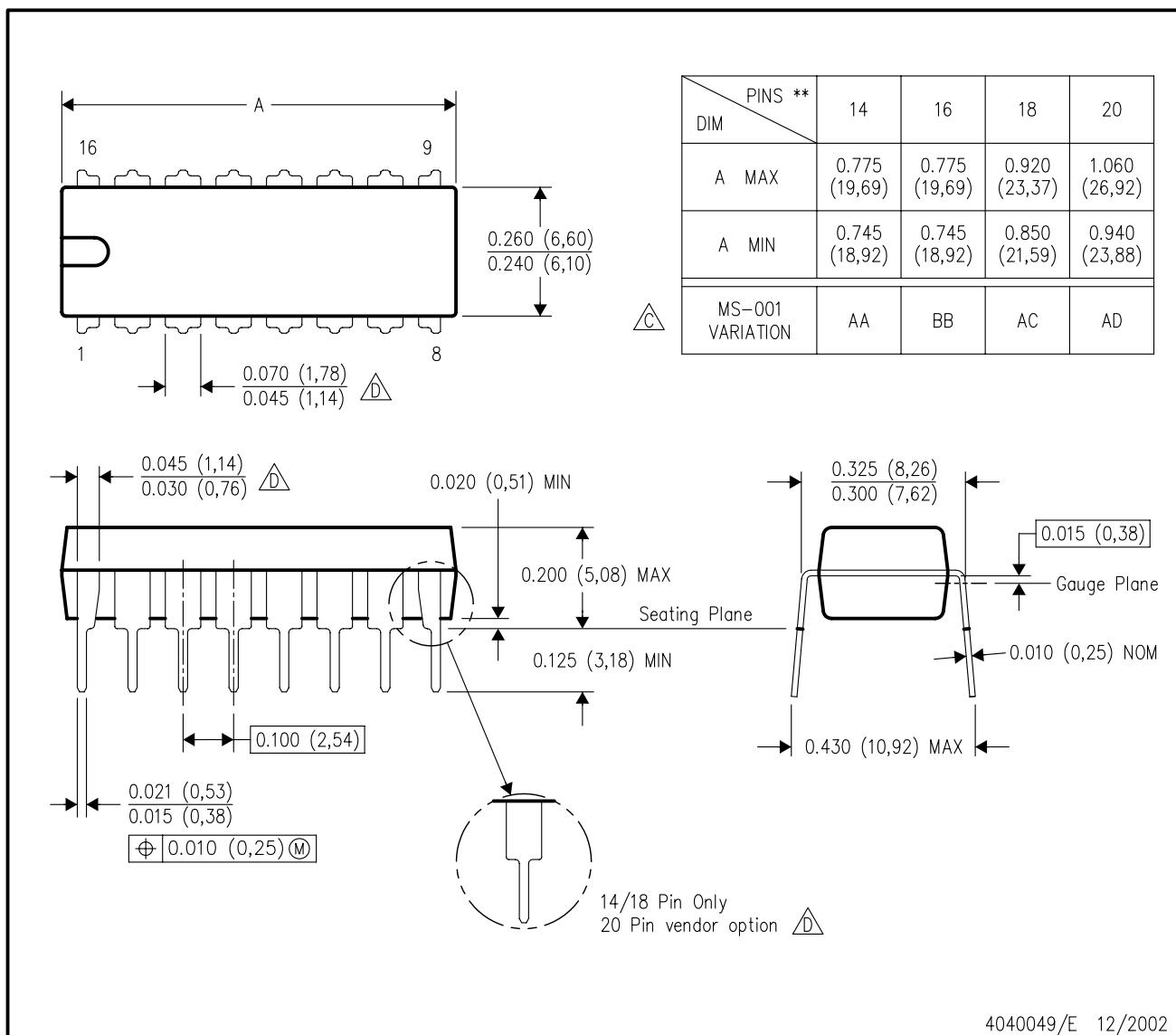
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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