# SNx4HC20 Dual 4-Input NAND Gates

## 1 Features

- Buffered inputs
- Wide operating voltage range: 2 V to 6 V
- Wide operating temperature range: –40°C to +85°C
- Supports fanout up to 10 LSTTL loads
- Significant power reduction compared to LSTTL logic ICs

## 2 Applications

- Alarm / tamper detect circuit
- S-R latch

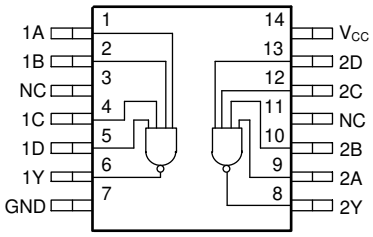
## 3 Description

This device contains two independent 4-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ in positive logic.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74HC20D | SOIC (14) | 8.70 mm × 3.90 mm |
| SN74HC20N | PDIP (14) | 19.30 mm × 6.40 mm |
| SN74HC20NS | SO (14) | 10.20 mm × 5.30 mm |
| SN74HC20PW | TSSOP (14) | 5.00 mm × 4.40 mm |
| SN54HC20J | CDIP (14) | 21.30 mm × 7.60 mm |
| SN54HC20W | CFP (14) | 9.20 mm × 6.29 mm |
| SN54HC20FK | LCCC (20) | 8.90 mm × 8.90 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Functional pinout**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (August 2003) to Revision G (April 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Updated to new data sheet standards | 1 |
| • $R_{\theta JA}$ increased for the D package from 86 to 133.6°C/W, increased for the PW package from 113°C/W, and decreased for the N package from 80 to 67.2°C/W | 4 |


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## 5 Pin Configuration and Functions

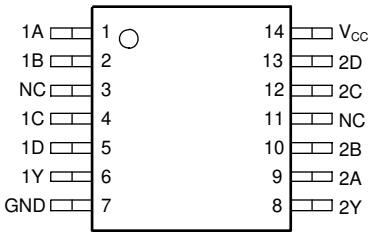



**Figure 5-1. D, N, NS, PW, J, or W Package 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, or CFP Top View**

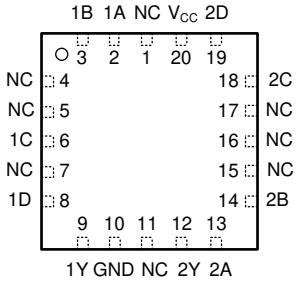



**Figure 5-2. FK Package 20-Pin LCCC Top View**

### Pin Functions

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | D, N, NS, PW, J, or W | FK | | |
| 1A | 1 | 2 | Input | Channel 1, Input A |
| 1B | 2 | 3 | Input | Channel 1, Input B |
| NC | 3, 11 | 1, 4, 5, 7, 11, 15, 16, 17 | — | Not internally connected |
| 1C | 4 | 6 | Input | Channel 1, Input C |
| 1D | 5 | 8 | Input | Channel 1, Input D |
| 1Y | 6 | 9 | Output | Channel 1, Output Y |
| GND | 7 | 10 | — | Ground |
| 2Y | 8 | 12 | Output | Channel 2, Output Y |
| 2A | 9 | 13 | Input | Channel 2, Input A |
| 2B | 10 | 14 | Input | Channel 2, Input B |
| 2C | 12 | 18 | Input | Channel 2, Input C |
| 2D | 13 | 19 | Input | Channel 2, Input D |
| $V_{CC}$ | 14 | 20 | — | Positive Supply |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current(2) | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current(2) | $V_O < 0$ or $V_O > V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature(3) | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

## 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5 | 6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 6 V | 4.2 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | | 0.5 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 6 V | | | 1.8 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $t_t$ | Input transition time | $V_{CC}$ = 2 V | | | 1000 | ns |
| | | $V_{CC}$ = 4.5 V | | | 500 | |
| | | $V_{CC}$ = 6 V | | | 400 | |
| $T_A$ | Operating free-air temperature | SN54HC00 | –55 | | 125 | °C |
| | | SN74HC00 | –40 | | 85 | |

## 6.3 Thermal Information

| THERMAL METRIC(1) | | SN74HC20 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | N (PDIP) | D (SOIC) | PW (TSSOP) | NS (SOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 67.2 | 133.6 | 151.7 | 122.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 55.3 | 89.0 | 79.4 | 81.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 46.9 | 89.5 | 94.7 | 83.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 35.3 | 45.5 | 25.2 | 45.4 | °C/W |


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| THERMAL METRIC[1] | | SN74HC20 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | N (PDIP) | D (SOIC) | PW (TSSOP) | NS (SOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | 14 PINS | |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 46.7 | 89.1 | 94.1 | 83.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.4 Electrical Characteristics - 74

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | -40°C to 85°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | | V |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | | |
| | | | $I_{OH}$ = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.84 | | | |
| | | | $I_{OH}$ = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.34 | | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.002 | 0.1 | | | 0.1 | V |
| | | | | 4.5 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | | 0.33 | |
| | | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | | 0.33 | |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or 0 | | 6 V | | ±0.1 | ±100 | | | ±1000 | nA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or 0 | $V_I$ = $V_{CC}$ or 0 | 6 V | | | 2 | | | 20 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | 3 | 10 | | | 10 | pF |

## 6.5 Electrical Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | Operating free-air temperature ($T_A$) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –55°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{OH}$ | High-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | | V |
| | | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | | |
| | | | | 6 V | 5.9 | 5.999 | | 5.9 | | | |
| | | | $I_{OH}$ = –4 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | | |
| | | | $I_{OH}$ = –5.2 mA | 6 V | 5.48 | 5.8 | | 5.2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 µA | 2 V | | 0.002 | 0.1 | | | 0.1 | V |
| | | | | 4.5 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | | 6 V | | 0.001 | 0.1 | | | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 V | | 0.17 | 0.26 | | | 0.4 | |
| | | | $I_{OL}$ = 5.2 mA | 6 V | | 0.15 | 0.26 | | | 0.4 | |

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over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | Operating free-air temperature ($T_A$) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –55°C to 125°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or 0 | | 6 V | | | ±0.1 | | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I = V_{CC}$ or 0 | $I_O = 0$ | 6 V | | | 2 | | | 40 | µA |
| $C_i$ | Input capacitance | | | 2 V to 6 V | | 3 | 10 | | | 10 | pF |

## 6.6 Switching Characteristics - 74

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | FROM | TO | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 25°C | | | –40°C to 85°C | | | |
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | A, B, C, or D | Y | 2 V | | 45 | 110 | | | 140 | ns |
| | | | | 4.5 V | | 14 | 22 | | | 28 | |
| | | | | 6 V | | 11 | 19 | | | 24 | |
| $t_t$ | Transition-time | | Y | 2 V | | 27 | 75 | | | 95 | ns |
| | | | | 4.5 V | | 9 | 15 | | | 19 | |
| | | | | 6 V | | 7 | 13 | | | 16 | |

## 6.7 Switching Characteristics - 54

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

| PARAMETER | | FROM | TO | TEST CONDITIONS | $V_{CC}$ | Operating free-air temperature ($T_A$) | | | Operating free-air temperature ($T_A$) | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 25°C | | | –55°C to 125°C | | | |
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Propagation delay | A, B, C, or D | Y | $C_L$ = 50 pF | 2 V | | 45 | 110 | | | 140 | ns |
| | | | | | 4.5 V | | 9 | 22 | | | 28 | |
| | | | | | 6 V | | 8 | 19 | | | 24 | |
| $t_t$ | Transition-time | | Y | $C_L$ = 50 pF | 2 V | | 27 | 75 | | | 95 | ns |
| | | | | | 4.5 V | | 9 | 15 | | | 19 | |
| | | | | | 6 V | | 7 | 13 | | | 16 | |

## 6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | No load | 2 V to 6 V | | 25 | | pF |

## 6.9 Typical Characteristics

$T_A$ = 25°C


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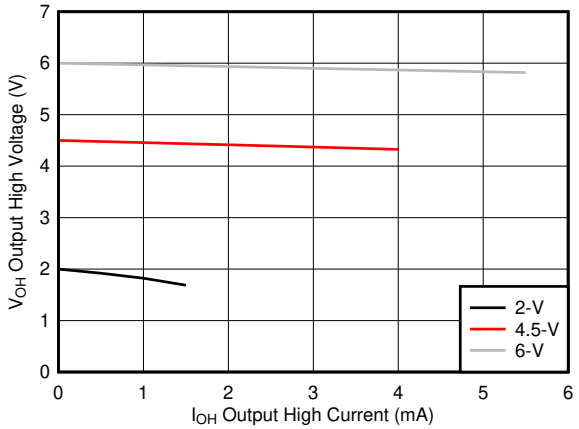



**Figure 6-1. Typical output voltage in the high state ($V_{OH}$)**

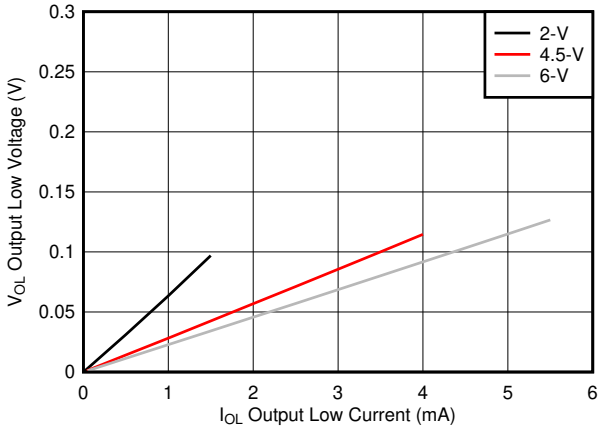
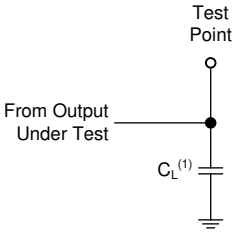



**Figure 6-2. Typical output voltage in the low state ($V_{OL}$)**

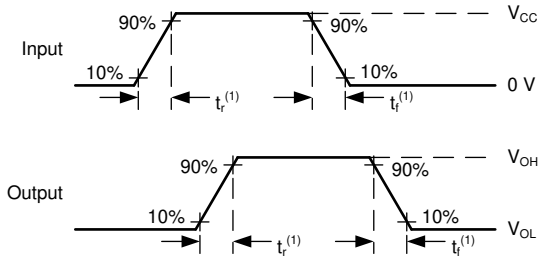
## 7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_t$ < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



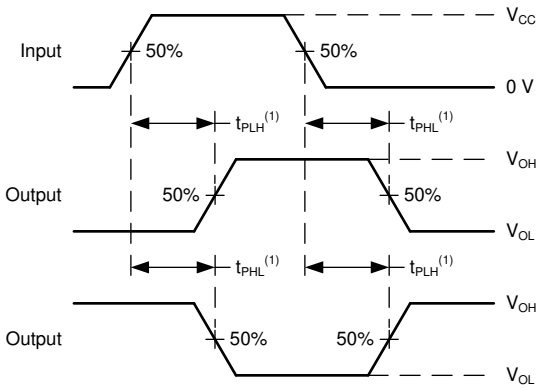

A. $C_L$ = 50 pF and includes probe and jig capacitance.

**Figure 7-1. Load Circuit**




A. $t_t$ is the greater of $t_r$ and $t_f$.

**Figure 7-2. Voltage Waveforms Transition Times**




A. The maximum between $t_{PLH}$ and $t_{PHL}$ is used for $t_{pd}$.

**Figure 7-3. Voltage Waveforms Propagation Delays**

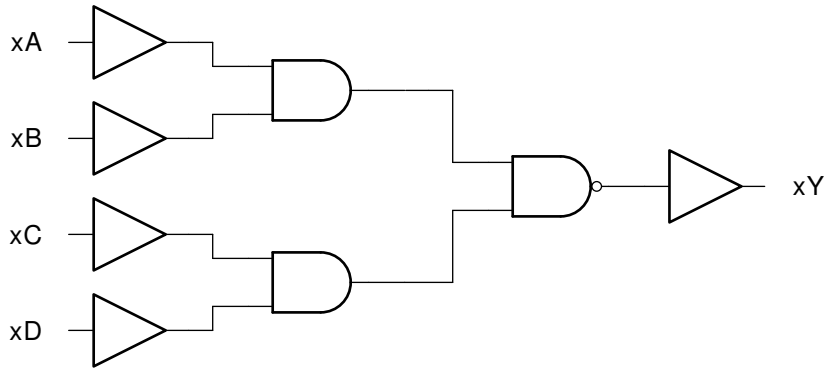

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# 8 Detailed Description

## 8.1 Overview

This device contains two independent 4-input NAND gates. Each gate performs the Boolean function $Y = \overline{A \bullet B \bullet C \bullet D}$ in positive logic.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74HC20 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics - 74* connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

### 8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics - 74*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics - 74*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

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### 8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 8-1.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

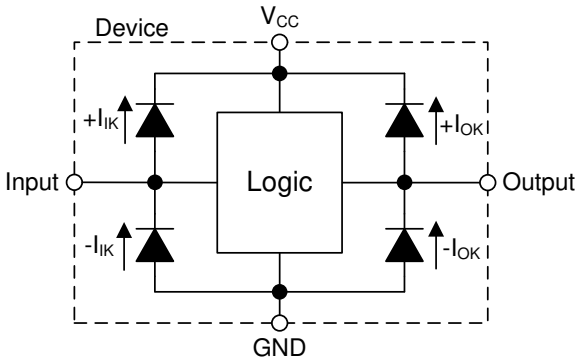



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

## 8.4 Device Functional Modes

**Table 8-1. Function Table**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| A | B | C | D | Y |
| H | H | H | H | L |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

In this application, two 4-input NAND gates are used to create an active-low SR latch as shown in *Figure 9-1*. Unused inputs can be tied together or to $V_{CC}$

This device is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the R input which returns the Q output back to LOW.

## 9.2 Typical Application

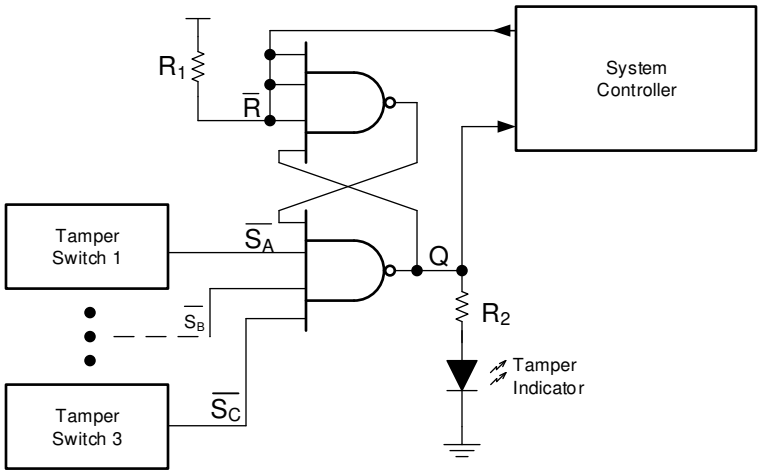



**Figure 9-1. Typical application schematic**

### 9.2.1 Design Requirements

#### *9.2.1.1 Power Considerations*

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics - 74*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HC20 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics - 74*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or $V_{CC}$ listed in the *Absolute Maximum Ratings*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and $C_{pd}$ Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

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**CAUTION**

The maximum junction temperature, $T_J$(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### *9.2.1.2 Input Considerations*

Unused inputs must be terminated to either $V_{CC}$ or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HC20, as specified in the *Electrical Characteristics - 74*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HC20 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *Recommended Operating Conditions*.

Refer to *Section 8.3* for additional information regarding the inputs for this device.

#### *9.2.1.3 Output Considerations*

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics - 74*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics - 74*.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to *Section 8.3* for additional information regarding the outputs for this device.

### 9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in *Section 11*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HC20 to the receiving device.
3. Ensure the resistive load at the output is larger than ($V_{CC}$ / $I_O$(max)) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

### 9.2.3 Application Curves

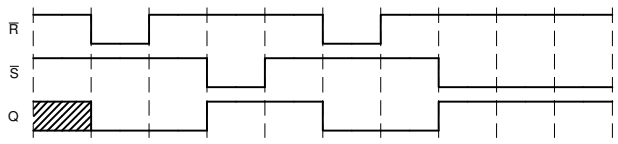



**Figure 9-2. Typical application timing diagram**


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## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Figure 11-1*.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### 11.2 Layout Example

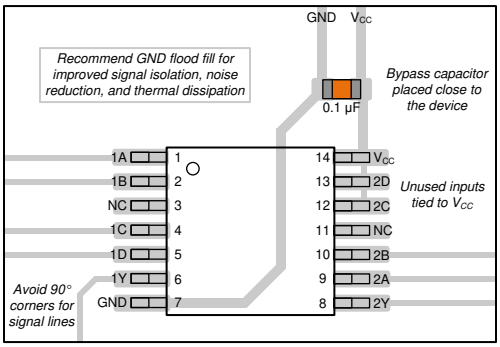



**Figure 11-1. Example layout for the SN74HC20**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

## 12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-8403901VCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8403901VC A SNV54HC20J |
| 5962-8403901VCA.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8403901VC A SNV54HC20J |
| 84039012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84039012A SNJ54HC 20FK |
| 8403901CA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901CA SNJ54HC20J |
| 8403901DA | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901DA SNJ54HC20W |
| JM38510/65003BCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65003BCA |
| JM38510/65003BCA.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65003BCA |
| M38510/65003BCA | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 65003BCA |
| SN54HC20J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC20J |
| SN54HC20J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54HC20J |
| SN74HC20D | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC20 |
| SN74HC20DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20DR1G4 | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20DR1G4.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC20N |
| SN74HC20N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC20N |
| SN74HC20NSR | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20NSR.A | Active | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20PW | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC20 |
| SN74HC20PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | HC20 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74HC20PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC20 |
| SN74HC20PWT | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 85 | HC20 |
| SNJ54HC20FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84039012A SNJ54HC 20FK |
| SNJ54HC20FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 84039012A SNJ54HC 20FK |
| SNJ54HC20J | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901CA SNJ54HC20J |
| SNJ54HC20J.A | Active | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901CA SNJ54HC20J |
| SNJ54HC20W | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901DA SNJ54HC20W |
| SNJ54HC20W.A | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8403901DA SNJ54HC20W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54HC20, SN54HC20-SP, SN74HC20 :**

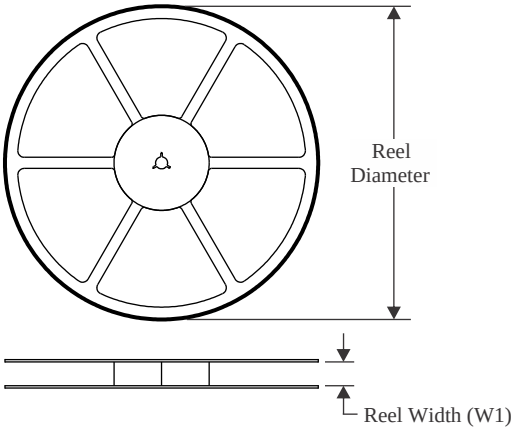
- Catalog : SN74HC20, SN54HC20
- Military : SN54HC20
- Space : SN54HC20-SP

NOTE: Qualified Version Definitions:

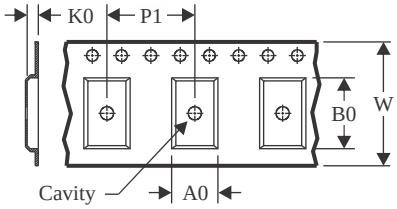
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

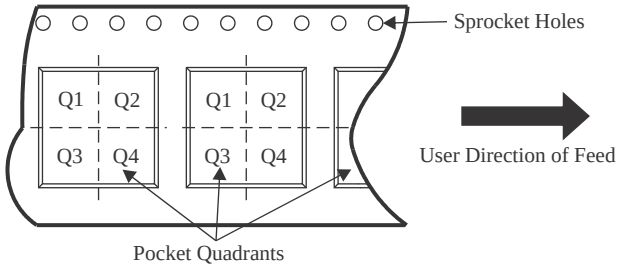



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

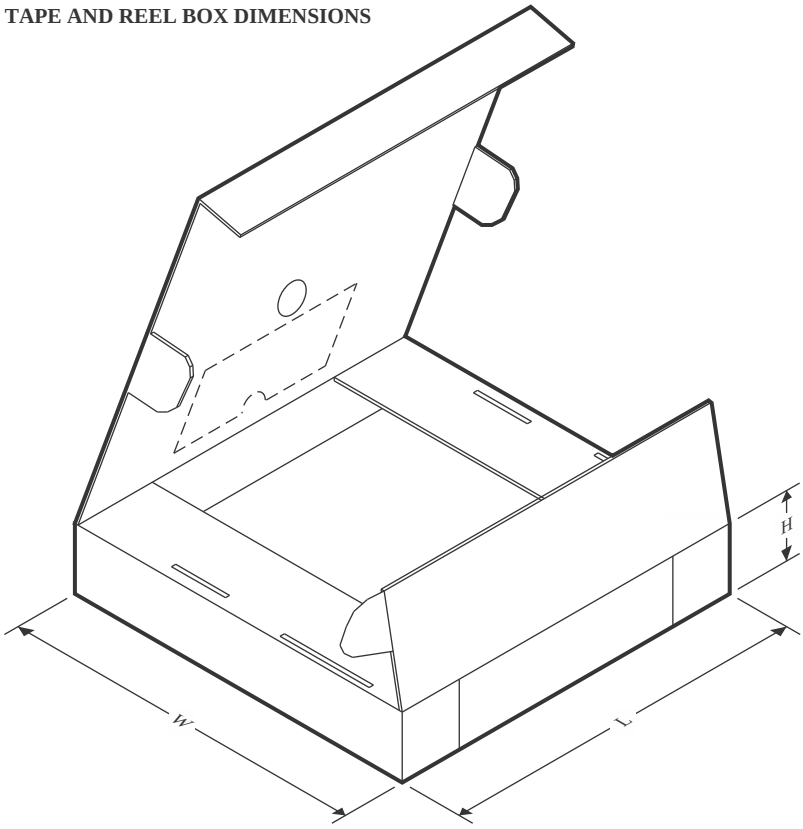
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74HC20NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.45 | 10.55 | 2.5 | 12.0 | 16.2 | Q1 |
| SN74HC20PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74HC20PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

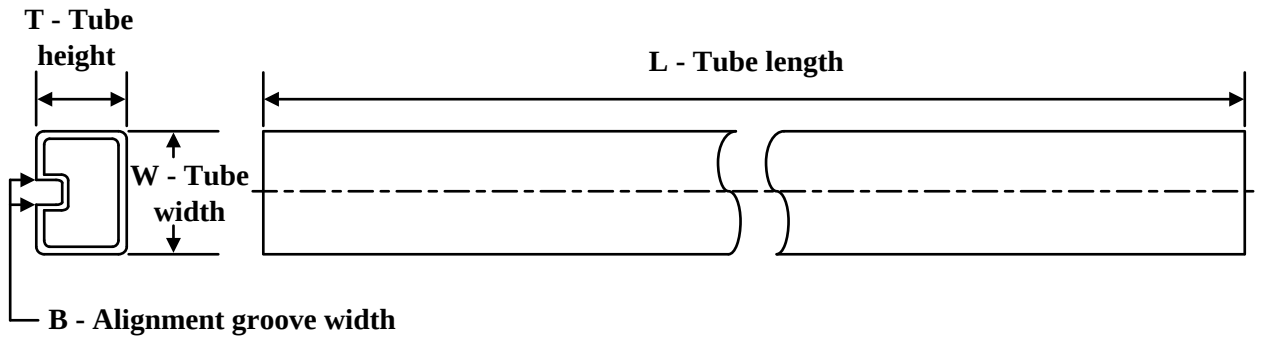
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

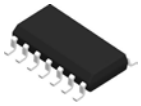
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74HC20NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC20PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74HC20PWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 84039012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8403901DA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HC20N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC20N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC20N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC20N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HC20FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC20FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HC20W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54HC20W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

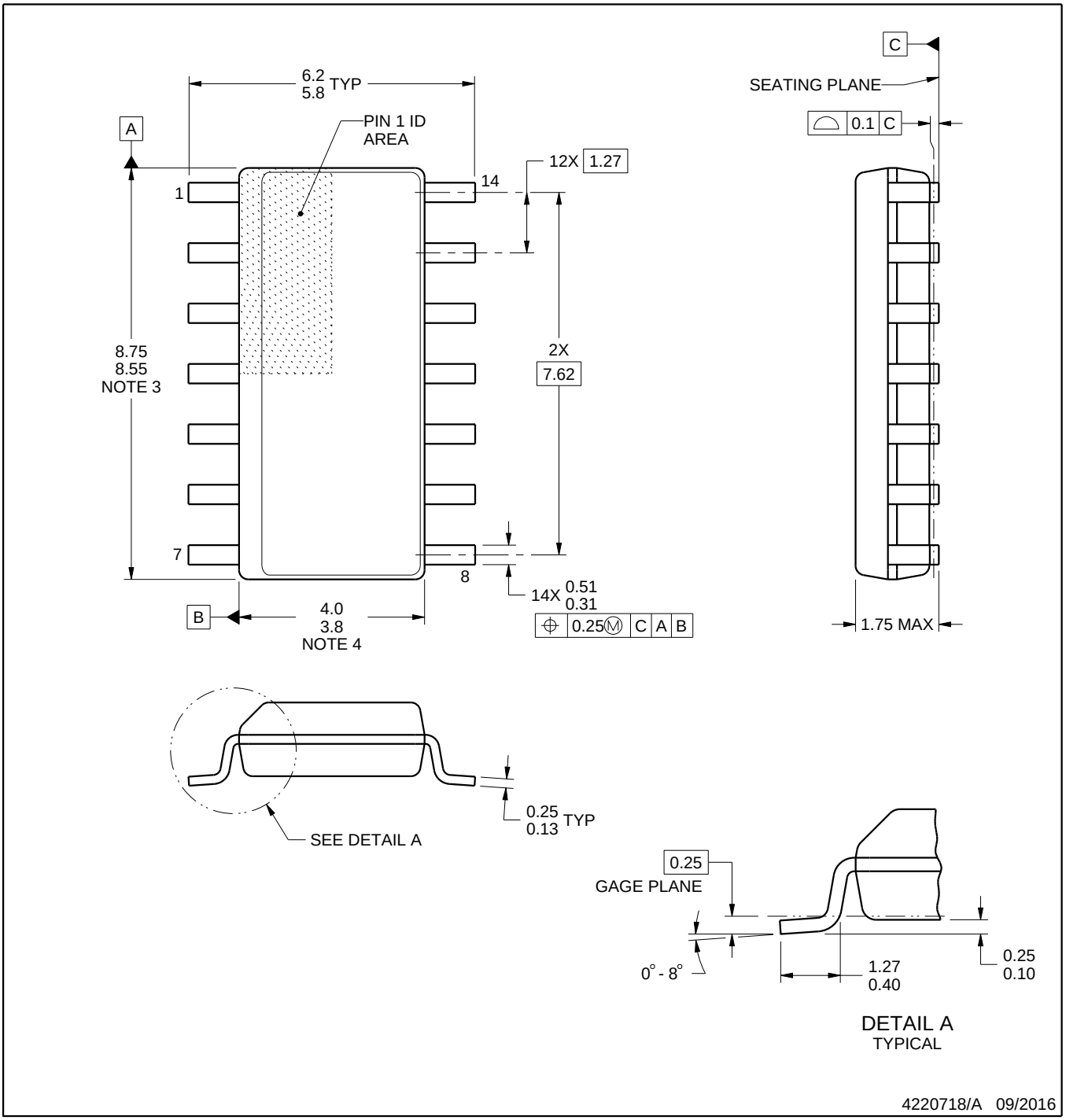


# PACKAGE OUTLINE

## D0014A

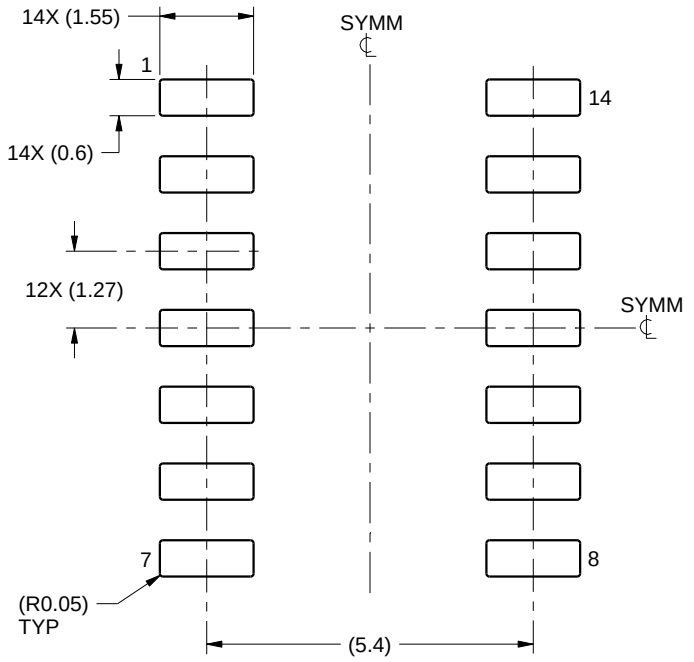
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

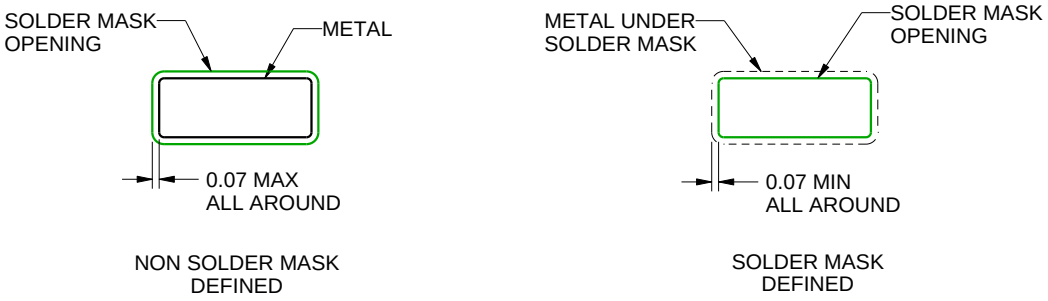



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

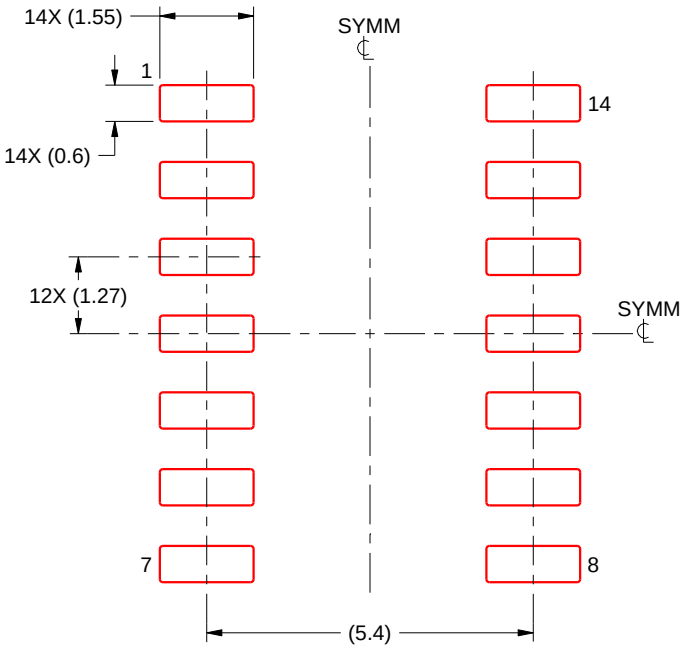
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

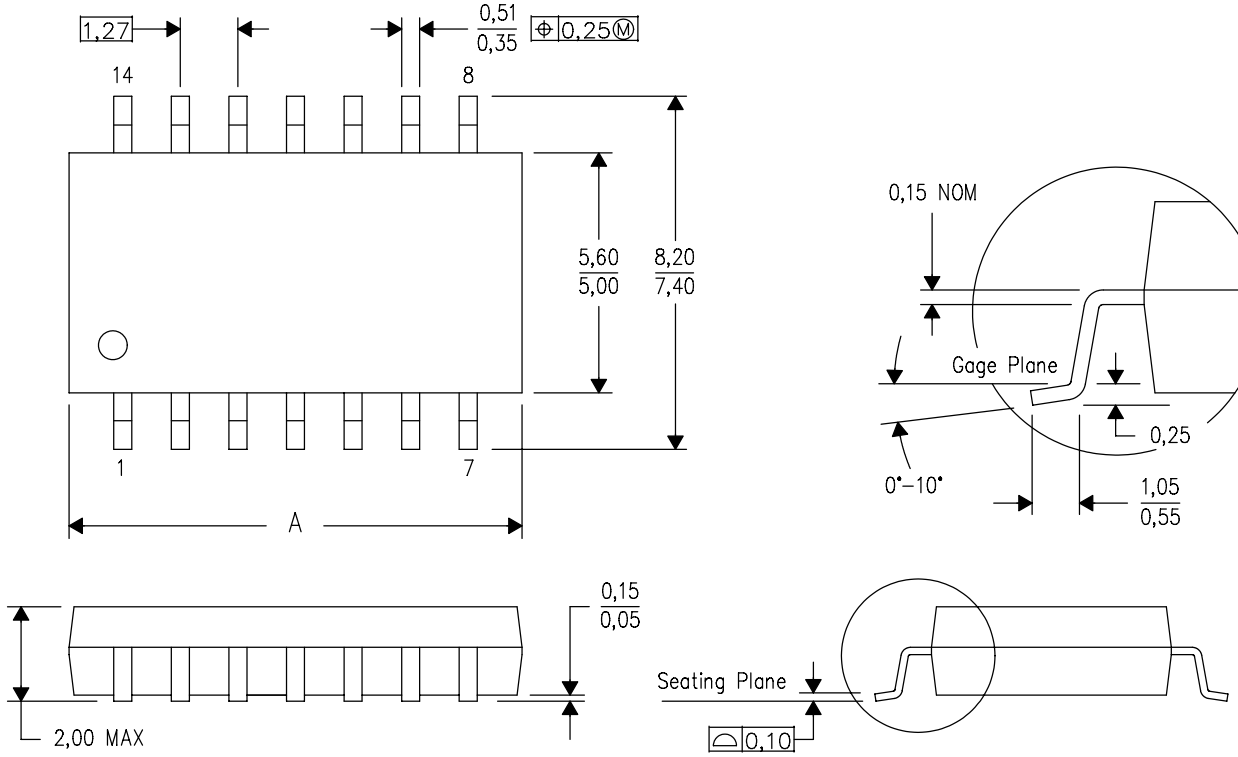
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

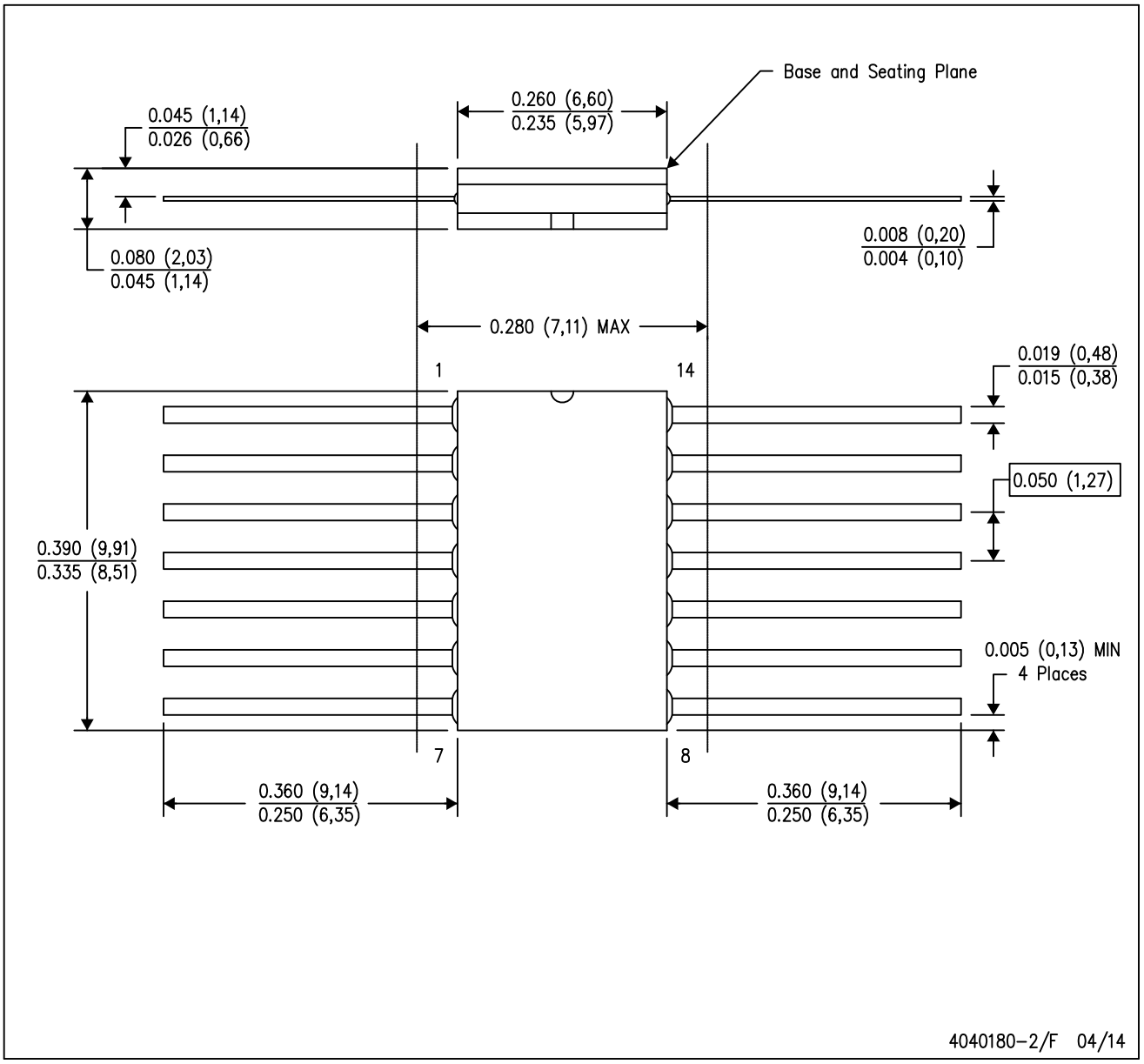



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

# GENERIC PACKAGE VIEW

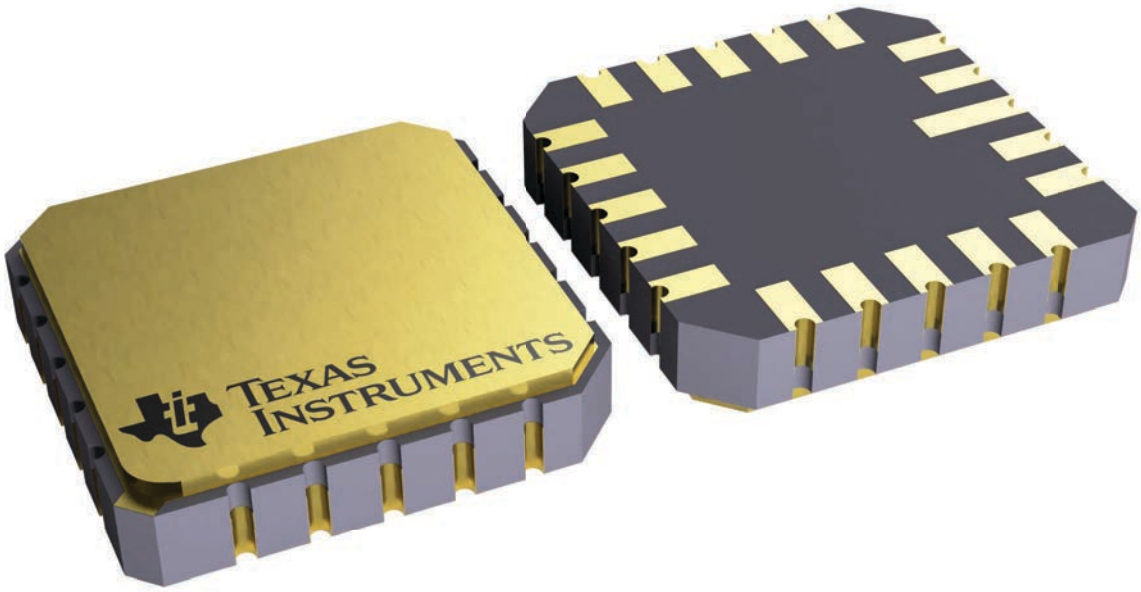
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

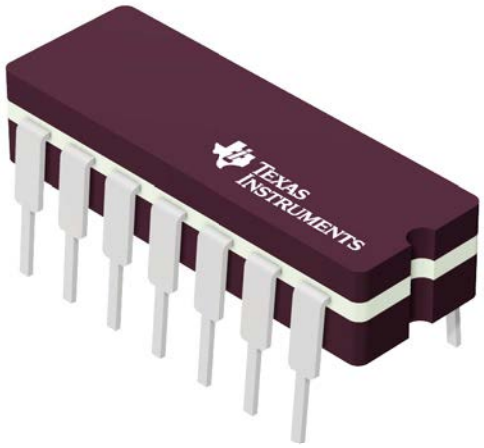



4229370VA\

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

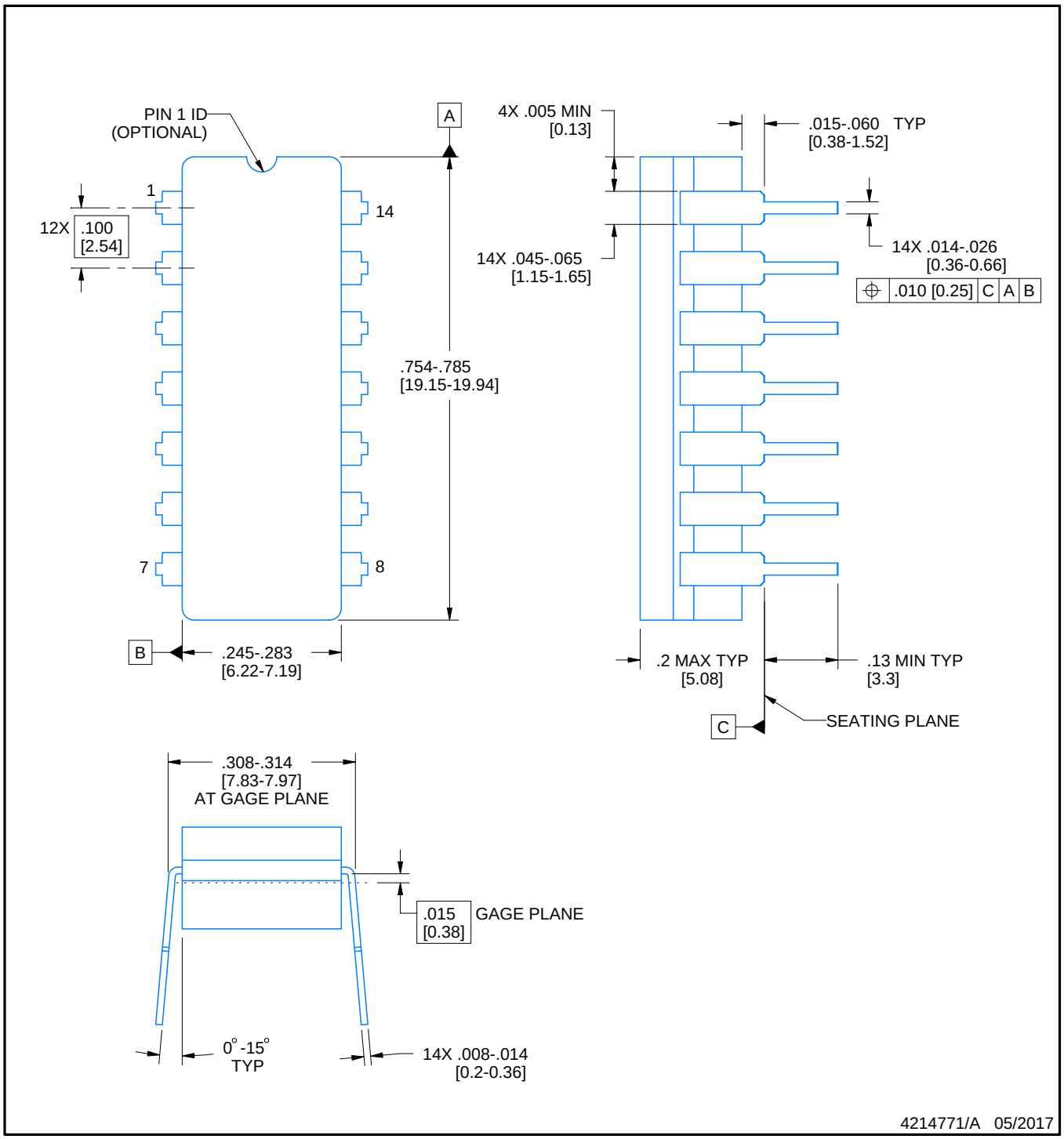


# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

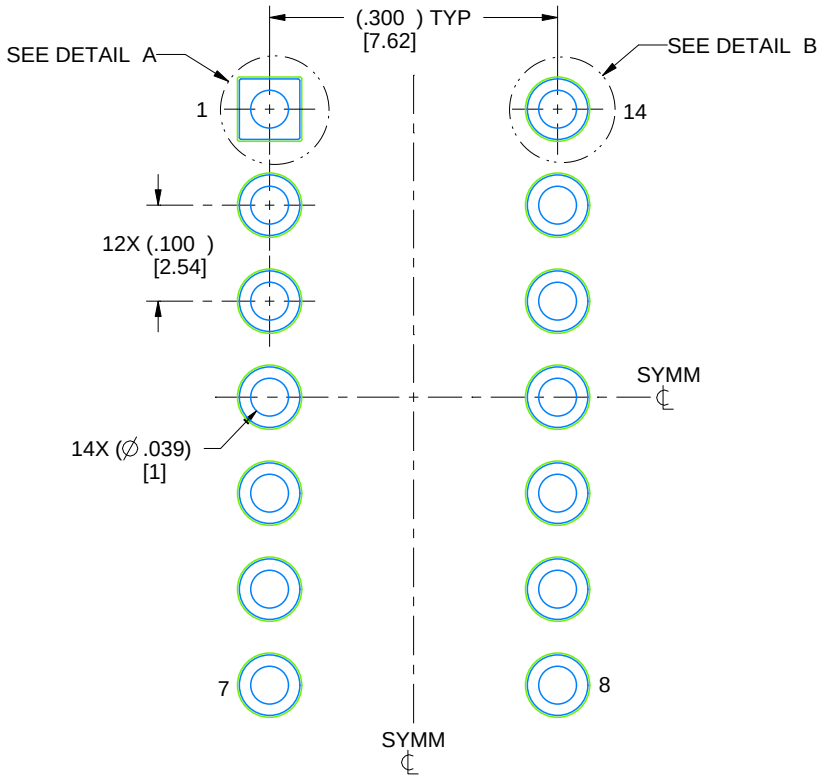
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

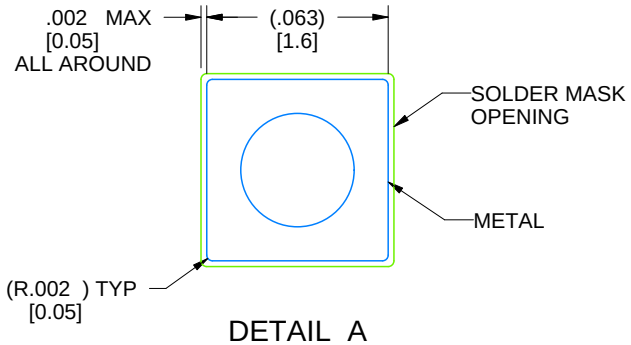
## J0014A

## CDIP - 5.08 mm max height

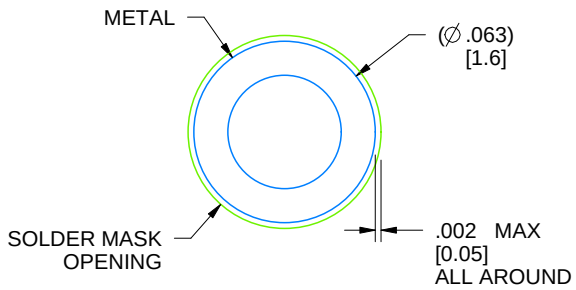
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



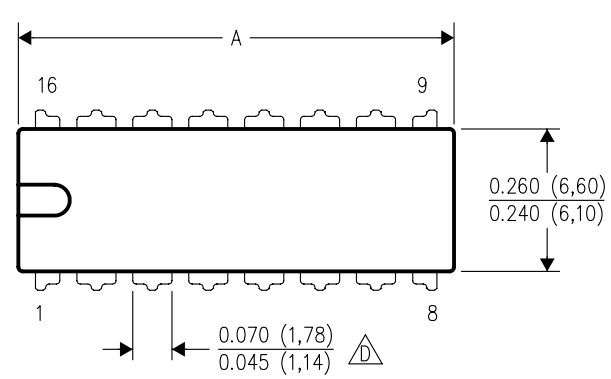

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

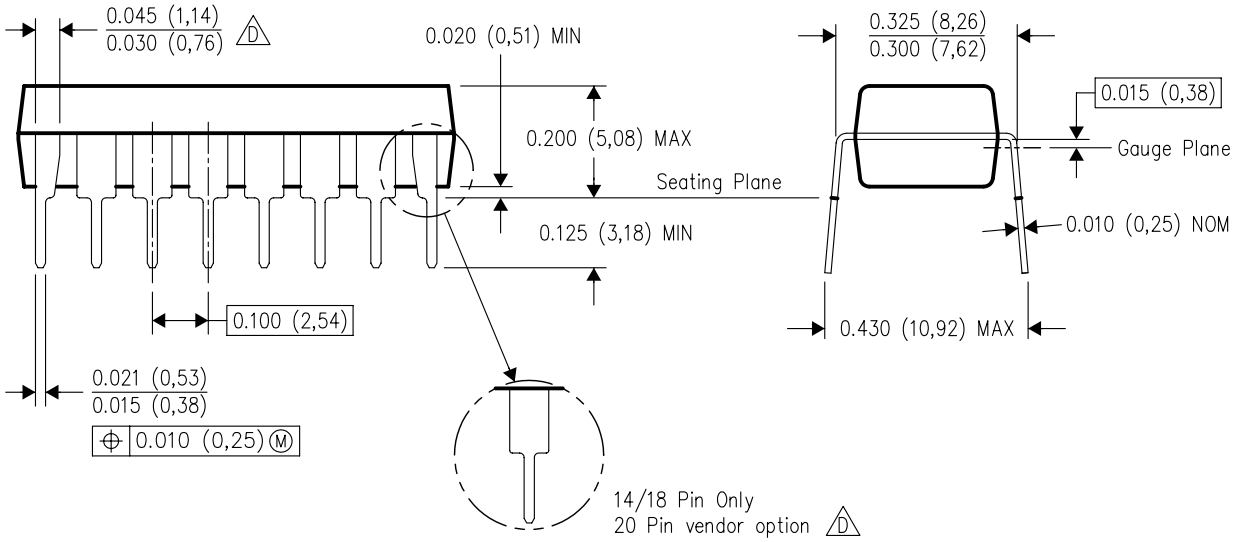
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

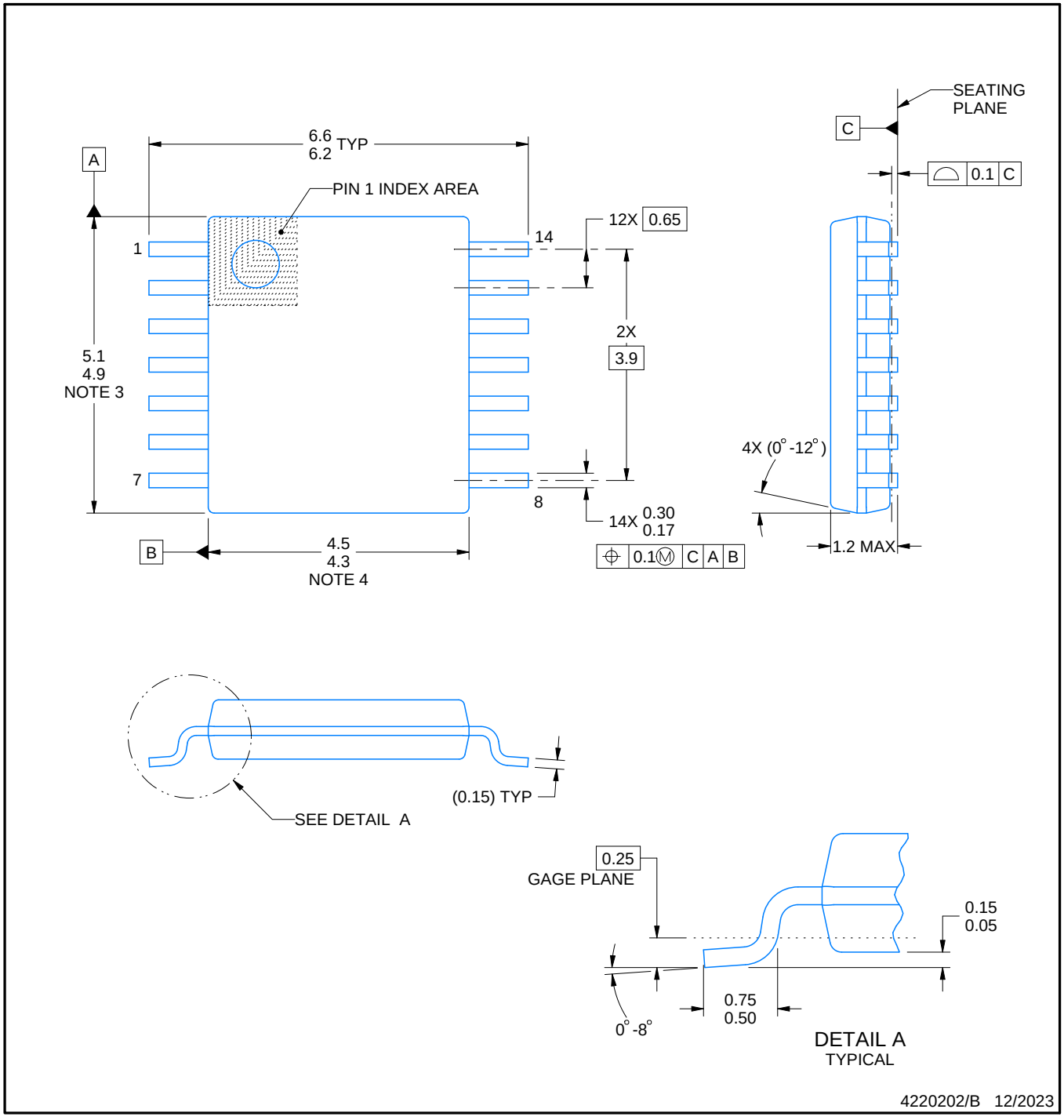
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

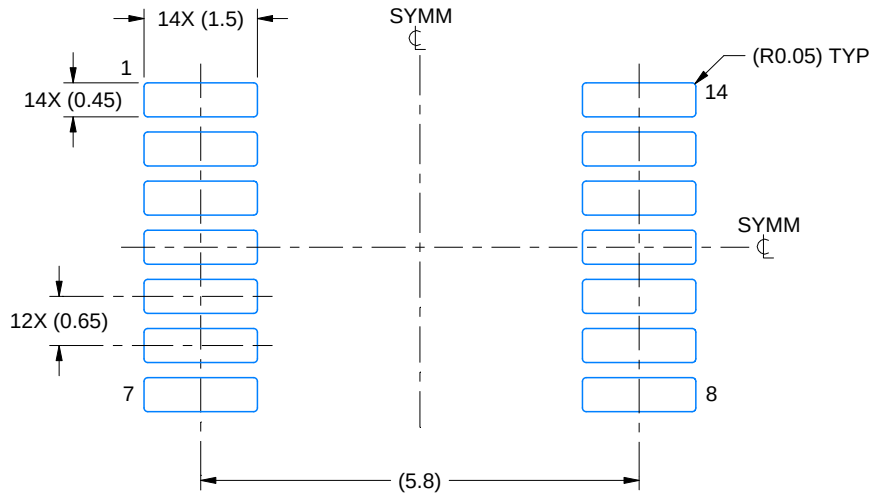
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

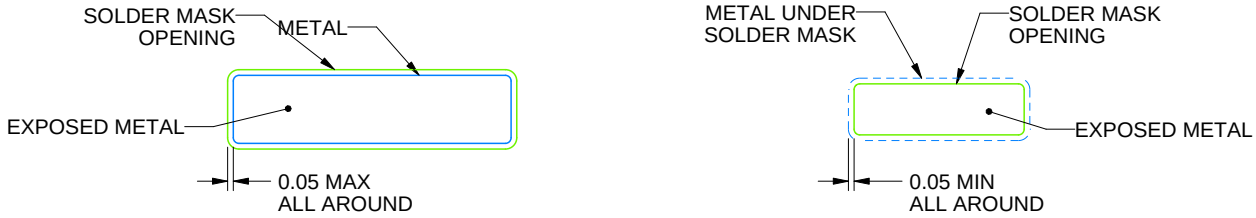



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

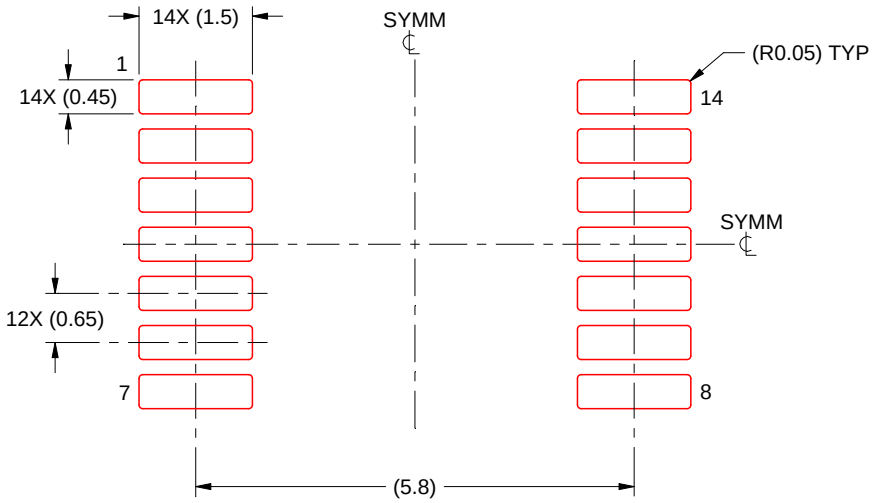



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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