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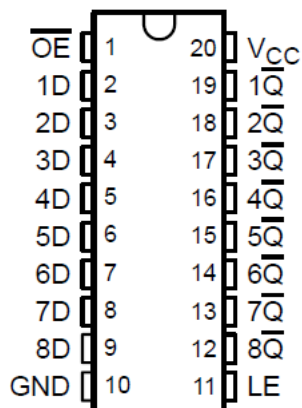
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3 Revision History

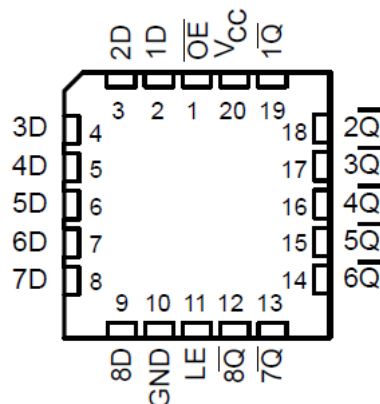
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (January 2022) to Revision E (July 2022) | Page |
|--|-------------|
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6.... | 4 |
| Changes from Revision C (March 2003) to Revision D (January 2022) | Page |
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | 1 |

4 Pin Configuration and Functions



DW or N package
20-Pin SOIC or PDIP
Top View



FK Package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|------------------|---|--|------|-----|------|
| V _{CC} | Supply voltage range | | –0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | | ±20 | mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | | ±20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±35 | mA |
| | Continuous current through V _{CC} or GND | | | ±70 | mA |
| T _J | Junction temperature | | | 150 | °C |
| T _{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

| | | | SN54HC563 | | | SN74HC563 | | | UNIT |
|-----------------|---------------------------------------|-------------------------|-----------|-----|-----------------|-----------|-----|-----------------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 2 | 5 | 6 | 2 | 5 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | | | 1.5 | | | V |
| | | V _{CC} = 4.5 V | 3.15 | | | 3.15 | | | |
| | | V _{CC} = 6 V | 4.2 | | | 4.2 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | | 0.5 | | | 0.5 | V |
| | | V _{CC} = 4.5 V | | | 1.35 | | | 1.35 | |
| | | V _{CC} = 6 V | | | 1.8 | | | 1.8 | |
| V _I | Input voltage | | 0 | | V _{CC} | 0 | | V _{CC} | V |
| V _O | Output voltage | | 0 | | V _{CC} | 0 | | V _{CC} | V |
| t _t | Input transition (rise and fall) time | V _{CC} = 2 V | | | 1000 | | | 1000 | ns |
| | | V _{CC} = 4.5 V | | | 500 | | | 500 | |
| | | V _{CC} = 6 V | | | 400 | | | 400 | |
| T _A | Operating free-air temperature | | –55 | | 125 | –40 | | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

| THERMAL METRIC | | DW (SOIC) | N (PDIP) | UNIT |
|------------------------|---|-----------|----------|------|
| | | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 109.1 | 84.6 | °C/W |
| R _{θJC (top)} | Junction-to-case (top) thermal resistance | 76 | 72.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 77.6 | 65.3 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 51.5 | 55.3 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 77.1 | 65.2 | °C/W |
| R _{θJC (bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HC563 | | SN74HC563 | | UNIT |
|-----------------|---|---------------------------|-----------------|-----------------------|-------|------|-----------|-------|-----------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = –20 µA | 2 V | 1.9 | 1.998 | | 1.9 | | 1.9 | | V |
| | | | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | |
| | | | 6 V | 5.9 | 5.999 | | 5.9 | | 5.9 | | |
| | | I _{OH} = –6 mA | 4.5 V | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| | | I _{OH} = –7.8 mA | 6 V | 5.48 | 5.8 | | 5.2 | | 5.34 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 µA | 2 V | | 0.002 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | | 6 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | | I _{OL} = 6 mA | 4.5 V | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| | | I _{OL} = 7.8 mA | 6 V | | 0.15 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 6 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{OZ} | V _O = V _{CC} or 0 | | 6 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | µA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 6 V | | | 8 | | 160 | | 80 | µA |
| C _i | | | 2 V to 6 V | | 3 | 10 | | 10 | | 10 | pF |

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HC563 | | SN74HC563 | | UNIT |
|-----------------|-----------------------------|-----------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 2 V | 80 | | 120 | | 100 | | ns |
| | | 4.5 V | 16 | | 24 | | 20 | | |
| | | 6 V | 14 | | 20 | | 17 | | |
| t _{su} | Setup time, data before LE↓ | 2 V | 50 | | 75 | | 63 | | ns |
| | | 4.5 V | 10 | | 15 | | 13 | | |
| | | 6 V | 9 | | 13 | | 11 | | |
| t _h | Hold time, data after LE↓ | 2 V | 5 | | 5 | | 5 | | ns |
| | | 4.5 V | 5 | | 5 | | 5 | | |
| | | 6 V | 5 | | 5 | | 5 | | |

5.6 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC563 | | SN74HC563 | | UNIT |
|-----------|-----------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | D | \bar{Q} | 2 V | | 77 | 175 | | 265 | | 220 | ns |
| | | | 4.5 V | | 26 | 35 | | 53 | | 44 | |
| | | | 6 V | | 23 | 30 | | 45 | | 37 | |
| | LE | Any \bar{Q} | 2 V | | 90 | 175 | | 265 | | 220 | |
| | | | 4.5 V | | 27 | 35 | | 53 | | 44 | |
| | | | 6 V | | 23 | 30 | | 45 | | 37 | |
| t_{en} | \bar{OE} | Any \bar{Q} | 2 V | | 70 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 24 | 30 | | 45 | | 38 | |
| | | | 6 V | | 21 | 26 | | 38 | | 32 | |
| t_{dis} | \bar{OE} | Any \bar{Q} | 2 V | | 47 | 150 | | 225 | | 190 | ns |
| | | | 4.5 V | | 23 | 30 | | 45 | | 38 | |
| | | | 6 V | | 21 | 26 | | 38 | | 32 | |
| t_t | | Any \bar{Q} | 2 V | | 28 | 60 | | 90 | | 75 | ns |
| | | | 4.5 V | | 8 | 12 | | 18 | | 15 | |
| | | | 6V | | 6 | 10 | | 15 | | 13 | |

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

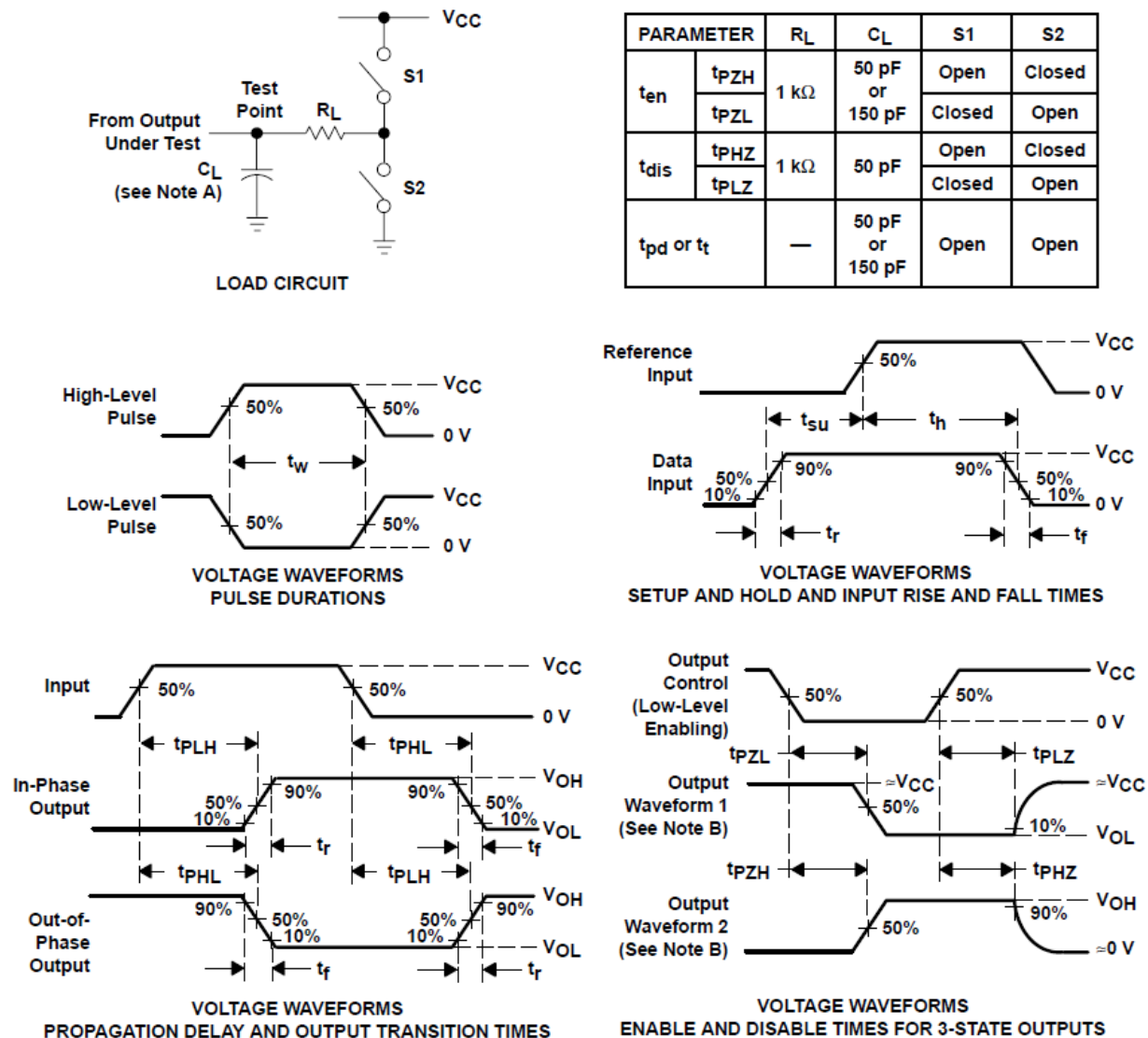
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HC563 | | SN74HC563 | | UNIT |
|-----------|-----------------|----------------|----------|--------------------------|-----|-----|-----------|-----|-----------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | D | \bar{Q} | 2 V | | 95 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 33 | 40 | | 60 | | 50 | |
| | | | 6 V | | 29 | 34 | | 51 | | 43 | |
| | LE | Any \bar{Q} | 2 V | | 103 | 225 | | 335 | | 285 | |
| | | | 4.5 V | | 33 | 45 | | 67 | | 57 | |
| | | | 6 V | | 29 | 38 | | 57 | | 48 | |
| t_{en} | \bar{OE} | Any \bar{Q} | 2 V | | 85 | 200 | | 300 | | 250 | ns |
| | | | 4.5 V | | 29 | 40 | | 60 | | 50 | |
| | | | 6 V | | 26 | 34 | | 51 | | 43 | |
| t_t | | Any \bar{Q} | 2 V | | 60 | 210 | | 315 | | 265 | ns |
| | | | 4.5 V | | 17 | 42 | | 63 | | 53 | |
| | | | 6 V | | 14 | 36 | | 53 | | 45 | |

5.8 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|-----------------|-----|------|
| C_{pd} | Power dissipation capacitance per latch | No load | 50 | pF |

6 Parameter Measurement Information



- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

These 8-bit transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

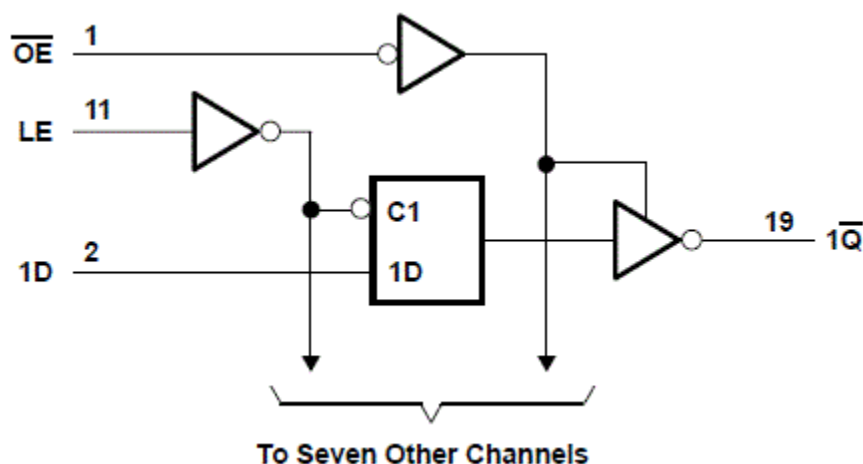
While the latch-enable (LE) input is high, the Q outputs follow the complements of the data (D) inputs. When LE is taken low, the outputs are latched at the inverses of the levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

7.2 Functional Block Diagram



7.3 Device Functional Modes

**Table 7-1. Function Table
(Each Latch)**

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|------------------|
| \overline{OE} | LE | D | |
| L | H | H | L |
| L | H | L | H |
| L | L | X | \overline{Q}_0 |
| H | X | X | Z |

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74HC563DW | Obsolete | Production | SOIC (DW) 20 | - | - | Call TI | Call TI | -40 to 85 | HC563 |
| SN74HC563DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC563 |
| SN74HC563DWR.A | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HC563 |
| SN74HC563N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC563N |
| SN74HC563N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74HC563N |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HC563DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HC563DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|--------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74HC563N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HC563N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| DIM | | | | |
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A**PACKAGE OUTLINE****SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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