SN74HCS00 Quadruple 2-Input NAND Gates With Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2V to 6V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
  - Typical I_{CC} of 100nA
  - Typical input leakage current of ±100nA
- ±7.8mA output drive at 5V
- Extended ambient temperature range: –40°C to +125°C, T_A

2 Applications

- Alarm or tamper detect circuit
- S-R latch

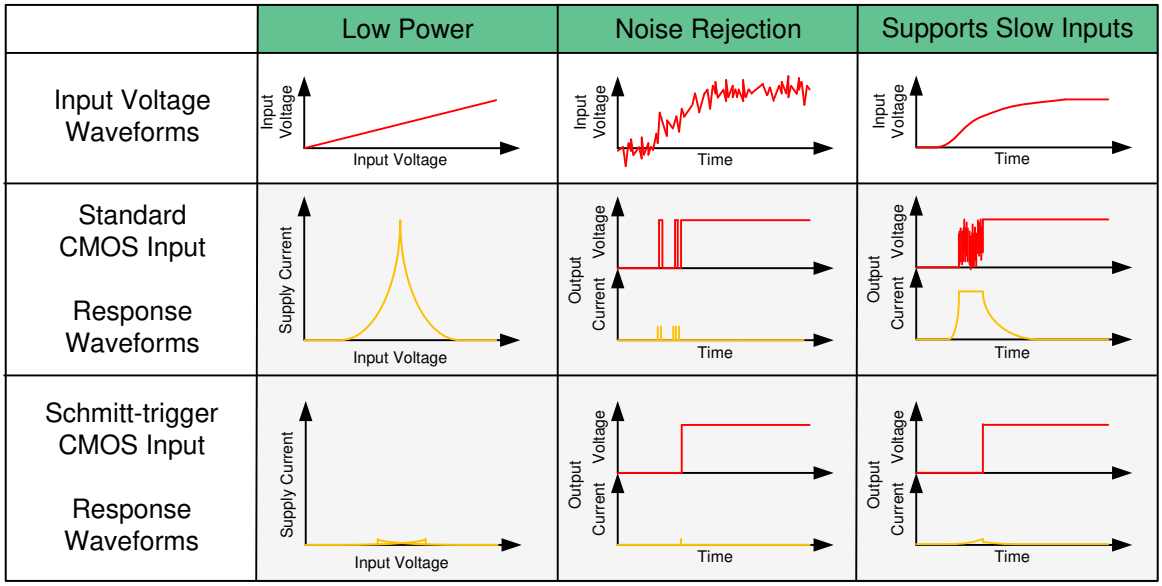
3 Description

This device contains four independent 2-input NAND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74HCS00PW	PW (TSSOP, 14)	5.00mm × 6.40mm
SN74HCS00D	D (SOIC, 14)	8.65mm × 6.00mm
SN74HCS00BQA	BQA (WQFN, 14)	3.00mm × 2.50mm
SN74HCS00DYY	DYY (SOT-23, 14)	4.20mm × 3.26mm

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Benefits of Schmitt-Trigger Inputs

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

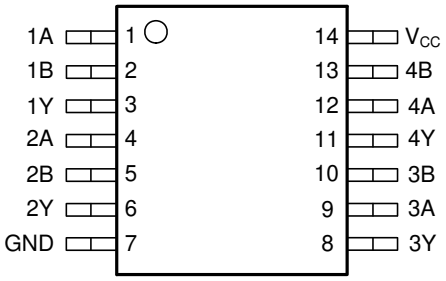

Figure 4-1. D, DYY, or PW Package 14-Pin SOIC, SOT-23, or TSSOP Top View

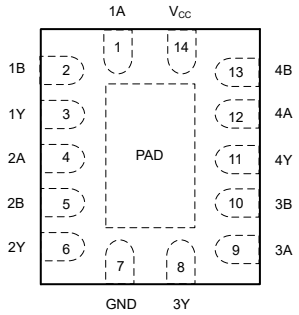

Figure 4-2. BQA Package 14-Pin WQFN Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
1Y	3	O	Channel 1, Output Y
2A	4	I	Channel 2, Input A
2B	5	I	Channel 2, Input B
2Y	6	O	Channel 2, Output Y
GND	7	—	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4B	13	I	Channel 4, Input B
V_{CC}	14	—	Positive Supply
Thermal Pad[2]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable
(2) BQA Package only.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5V$ or $V_I > V_{CC} + 0.5V$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < –0.5V$ or $V_O > V_{CC} + 0.5V$		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±35	mA
	Continuous current through V_{CC} or GND			±70	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Verified by design.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–55		125	°C

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5.4 Thermal Information

THERMAL METRIC[1]		SN74HCS00				UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	DYY (SOT)	
		14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	109.7	236.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	111.0	143.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	77.9	146.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	20.2	29.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	77.8	145.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	56.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2V	1.13	1.26	1.37	V
				4.5V	2.31	2.47	2.66	
				6V	2.99	3.18	3.44	
V_{T-}	Negative switching threshold			2V	0.55	0.62	0.71	V
				4.5V	1.21	1.36	1.5	
				6V	1.56	1.79	1.99	
ΔV_T	V_{T+} - V_{T-}			2V	0.54	0.64	0.71	V
				4.5V	0.94	1.11	1.27	
				6V	1.20	1.38	1.57	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20µA	2V to 6V	V_{CC} - 0.1	V_{CC} - 0.002		V
			I_{OH} = -6mA	4.5V	4.0	4.3		
			I_{OH} = -7.8mA	6V	5.4	5.75		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20µA	2V to 6V		0.002	0.1	V
			I_{OL} = 4mA	4.5V		0.18	0.30	
			I_{OL} = 7.8mA	6V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6V		0.1	2	µA
C_i	Input capacitance			2V to 6V			5	pF
C_{pd}	Power dissipation capacitance per gate	No load		2V to 6V		10		pF

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5.6 Switching Characteristics

C_L = 50pF; over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).
See *Parameter Measurement Information*

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A or B	Y	2V		15	36	ns
				4.5V		7	13	
				6V		5	12	
t_t	Transition-time		Y	2V		9	16	ns
				4.5V		5	9	
				6V		4	8	

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5.7 Typical Characteristics

T_A = 25°C

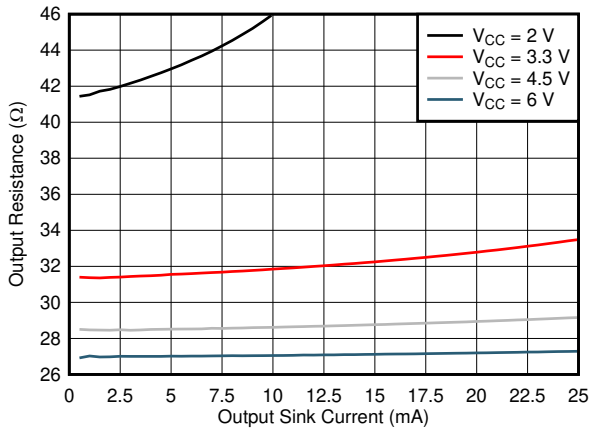

Figure 5-1. Output Driver Resistance in Low State

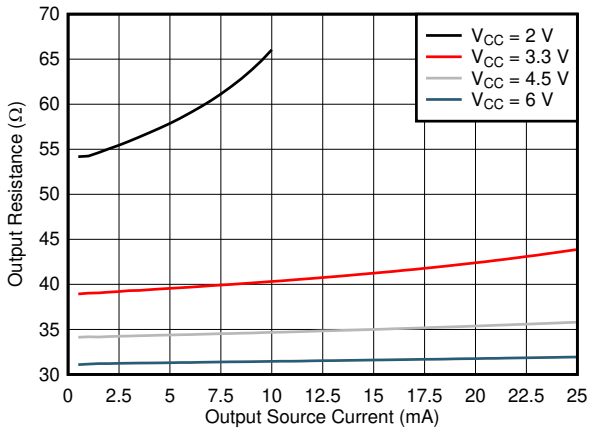

Figure 5-2. Output Driver Resistance in High State

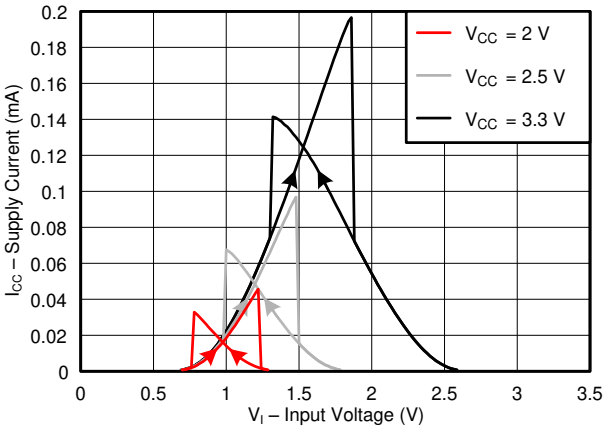

Figure 5-3. Typical Supply Current vs Input Voltage Across Common Supply Values (2V to 3.3V)

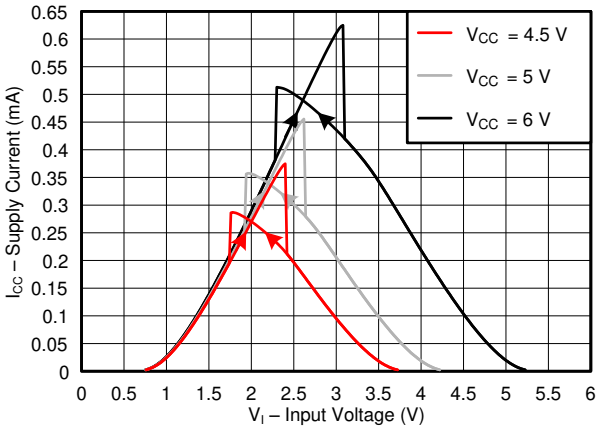

Figure 5-4. Typical Supply Current vs Input Voltage Across Common Supply Values (4.5V to 6V)

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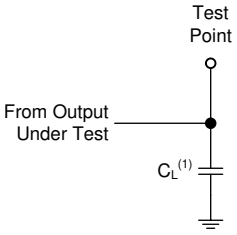
6 Parameter Measurement Information

- Phase relationships between waveforms are selected arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.
- The outputs are measured one at a time, with one input transition per measurement.



A. C_L = 50pF and includes probe and jig capacitance.

Figure 6-1. Load Circuit

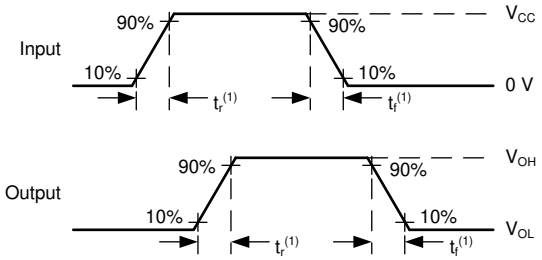
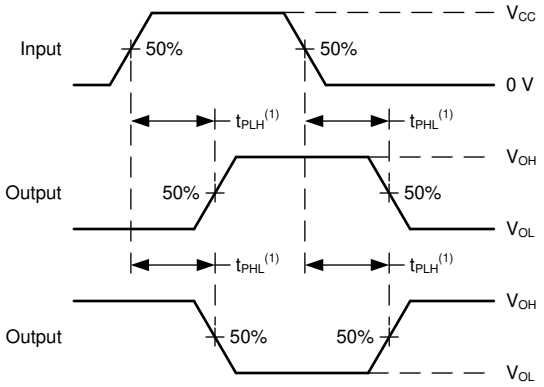


Figure 6-2. Voltage Waveforms Transition Times



A. The maximum between t_{PLH} and T_{PHL} is used for t_{pd}.

Figure 6-3. Voltage Waveforms Propagation Delays

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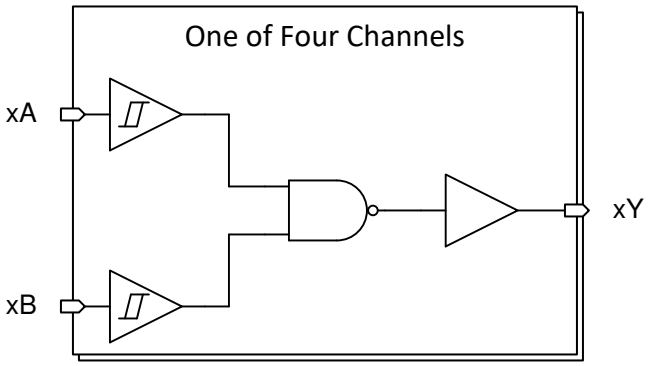
7 Detailed Description

7.1 Overview

This device contains four independent 2-input NAND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = \overline{A \bullet B}$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device can create fast edges into light loads so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the output power of the device to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, properly terminating unused inputs is recommended. Driving the inputs slowly also increases the dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see Understanding Schmitt Triggers.

7.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

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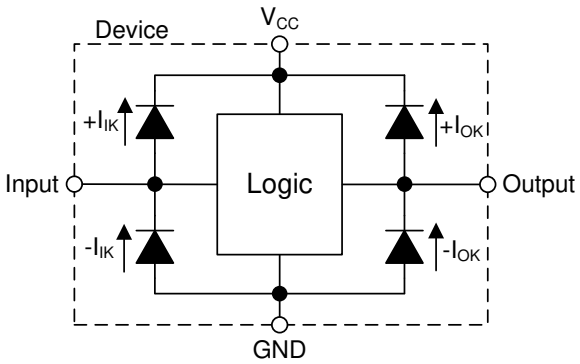

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74HCS00.

Table 7-1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, two 2-input NAND gates are used to create an active-low SR latch as shown in Figure 8-1. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74HCS00 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs LOW, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a LOW signal to the $\overline{R}$ input which returns the Q output back to LOW.

The inputs of this active-low SR latch can often be driven by open-drain outputs which can produce slow input transition rates when the inputs transition from LOW to Hi-Z. This makes the SN74HCS00 designed for the application because the device has Schmitt-trigger inputs that do not have input transition rate requirements.

8.2 Typical Application

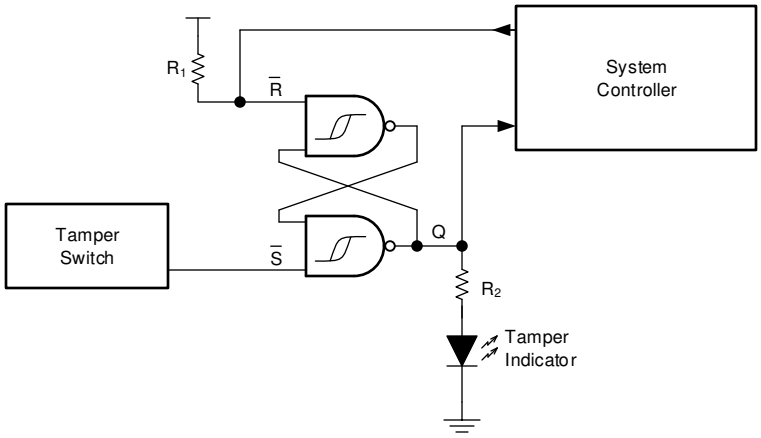

Figure 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

- All signals in the system operate at 5V
- Avoid unstable state by not having LOW signals on both inputs
- Q output is HIGH when $\overline{S}$ is LOW
  - Q output remains High until $\overline{R}$ is LOW

8.2.1.1 Power Considerations

Verify that the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS00 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*. The logic device can only source or sink as much current as is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *Absolute Maximum Ratings*.

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The SN74HCS00 can drive a load with a total capacitance less than or equal to 50pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however do not exceed 50pF.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, T_J(max) listed in the *Absolute Maximum Ratings*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross V_{t-}(min) to be considered a logic LOW, and V_{t+}(max) to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or the inputs can be connected with a pullup or pulldown resistor if the input is to be used sometimes, but not always. A pullup resistor is used for a default state of HIGH, and a pulldown resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS00, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10kΩ resistor value is often used due to these factors.

The SN74HCS00 has no input signal transition rate requirements because the devices has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the ΔV_T(min) in the *Electrical Characteristics*. This hysteresis value provides the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output decreases the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output increases the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that can be in the opposite states, even for a very short time period, must never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do no connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; however, this limit provides optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS00 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This verifies that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates; however, the power consumption and thermal increase can be calculated using the steps provided in the CMOS Power Consumption and Cpd Calculation application note.

8.2.3 Application Curves

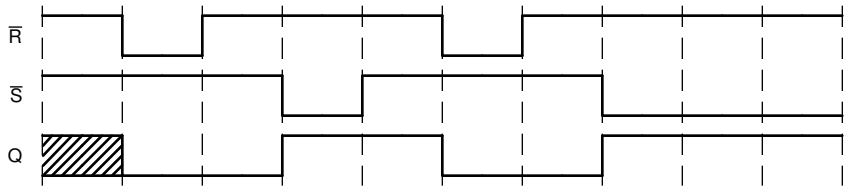

Figure 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. Multiple bypass capacitors can be placed in parallel to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results, as shown in the following layout example.

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8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or VCC, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

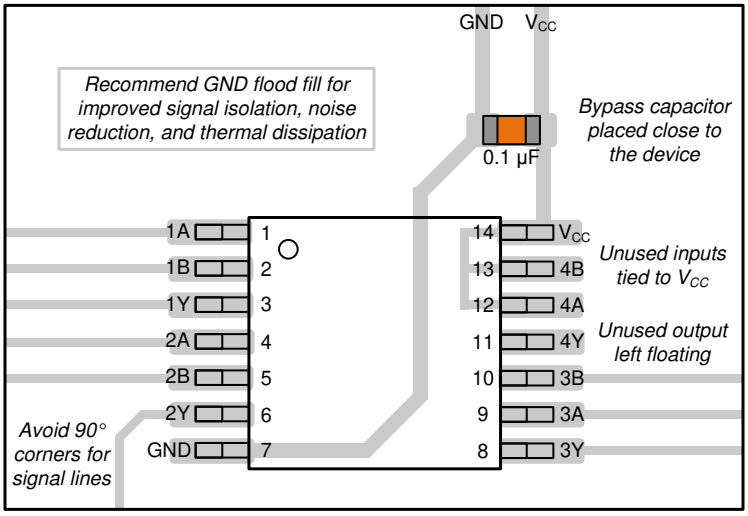

Figure 8-3. Example Layout for the SN74HCS00

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *HCMOS Design Considerations* application report
- Texas Instruments, *CMOS Power Consumption and CPD Calculation* application report
- Texas Instruments, *Designing with Logic* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 13, 2026 to September 29, 2026 (from Revision D (March 2026) to Revision E (October 2026)) **Page**

- Changed V_{T+} limits at 2V V_{CC} from 1.18V (min), 1.3V (max) to 1.13V (min), 1.37V (max) 5
- Added V_{T+} typical values at 2V V_{CC} 5
- Changed V_{T+} limits at 4.5V V_{CC} from 2.39V (min), 2.58V (max) to 2.31V (min), 2.66V (max) 5
- Added V_{T+} typical values at 4.5V V_{CC} 5
- Changed V_{T+} limits at 6V V_{CC} from 3.11V (min), 3.32V (max) to 2.99V (min), 3.44V (max) 5
- Added V_{T+} typical values at 6V V_{CC} 5
- Changed V_{T-} limits at 2V V_{CC} from 0.61V (min), 0.66V (max) to 0.55V (min), 0.71V (max) 5
- Added V_{T-} typical values at 2V V_{CC} 5
- Changed V_{T-} limits at 4.5V V_{CC} from 1.31V (min), 1.42V (max) to 1.21V (min), 1.50V (max) 5
- Added V_{T-} typical values at 4.5V V_{CC} 5

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- Changed V_{T-} limits at 6V V_{CC} from 1.72V (min), 1.87V (max) to 1.56V (min), 1.99V (max)....5
- Added V_{T-} typical values at 6V V_{CC} 5
- Changed ΔV_T limits at 2V V_{CC} from 0.2V (min), 1.0V (max) to 0.55V (min), 0.67V (max)....5
- Added ΔV_T typical values at 2V V_{CC} 5
- Changed ΔV_T limits at 4.5V V_{CC} from 1.04V (min), 1.21V (max) to 0.94V (min), 1.27V (max)....5
- Added ΔV_T typical values at 4.5V V_{CC} 5
- Changed ΔV_T limits at 6V V_{CC} from 1.34V (min), 1.49V (max) to 1.20V (min), 1.57V (max)....5
- Added ΔV_T typical values at 6V V_{CC} 5

Changes from December 13, 2021 to March 13, 2026 (from Revision C (December 2021) to Revision D (March 2026)) **Page**

- Changed V_{T+} limits at 2V V_{CC} from 0.7V (min), 1.5V (max) to 1.18V (min), 1.3V (max) 5
- Changed V_{T+} limits at 4.5V V_{CC} from 1.7V (min), 3.15V (max) to 2.39V (min), 2.58V (max) 5
- Changed V_{T+} limits at 6V V_{CC} from 2.1V (min), 4.2V (max) to 3.11V (min), 3.32V (max) 5
- Changed V_{T-} limits at 2V V_{CC} from 0.3V (min), 1.0V (max) to 0.61V (min), 0.66V (max)....5
- Changed V_{T-} limits at 4.5V V_{CC} from 0.9V (min), 2.2V (max) to 1.31V (min), 1.42V (max) 5
- Changed V_{T-} limits at 6V V_{CC} from 1.2V (min), 3.0V (max) to 1.72V (min), 1.87V (max)....5
- Changed ΔV_T limits at 2V V_{CC} from 0.2V (min), 1.0V (max) to 0.55V (min), 0.67V (max)....5
- Changed ΔV_T limits at 4.5V V_{CC} from 0.4V (min), 1.4V (max) to 1.04V (min), 1.21V (max)....5
- Changed ΔV_T limits at 6V V_{CC} from 0.6V (min), 1.6V (max) to 1.34V (min), 1.49V (max)....5

Changes from Revision B (January 2021) to Revision C (December 2021) **Page**

- Added DYY package to the *Device Information* table....1
- Added DYY package information to the *Pin Configuration and Functions* section....3
- Added DYY package to Thermal Information table....5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74HCS00BQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00BQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00DR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00DYYR	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00DYYR.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HCS00
SN74HCS00PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS00

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS00 :

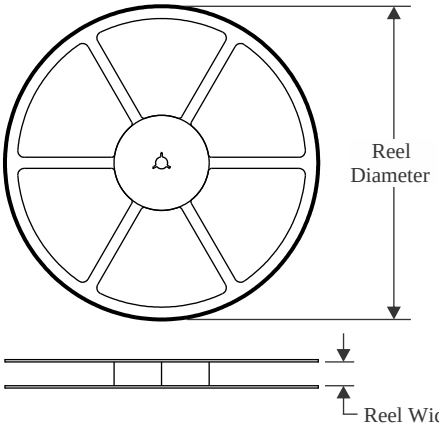
- Automotive : SN74HCS00-Q1

NOTE: Qualified Version Definitions:

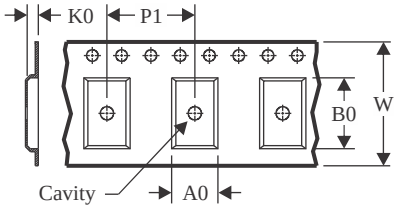
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

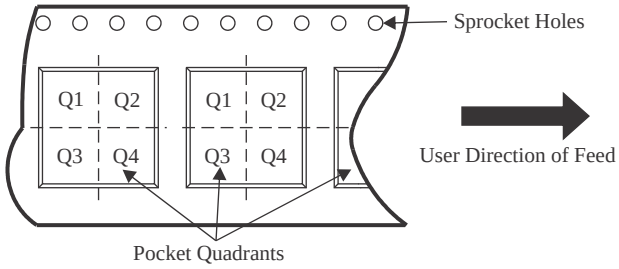


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

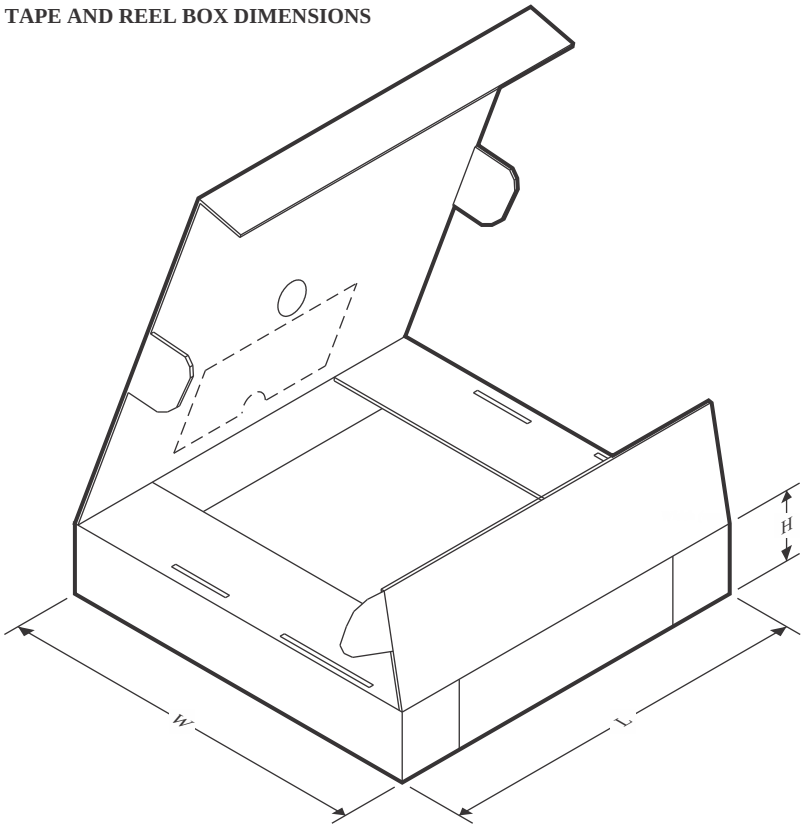
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS00BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS00BQAR	WQFN	BQA	14	3000	177.8	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS00BQAR	WQFN	BQA	14	3000	330.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS00DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS00DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74HCS00PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

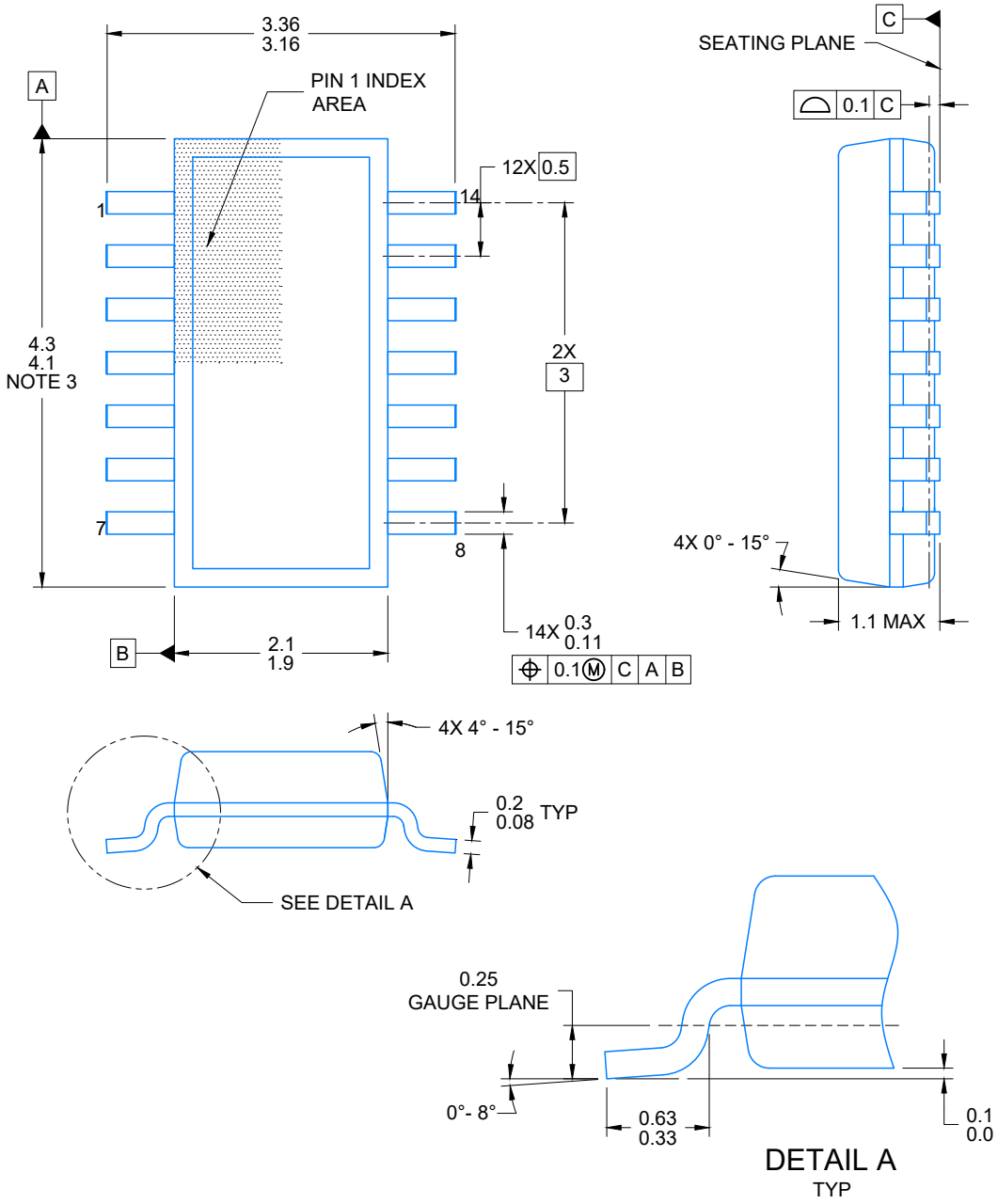
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS00BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74HCS00BQAR	WQFN	BQA	14	3000	208.0	191.0	35.0
SN74HCS00BQAR	WQFN	BQA	14	3000	346.0	346.0	33.0
SN74HCS00DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74HCS00DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCS00DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
SN74HCS00PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

PACKAGE OUTLINE

DYY0014A

SOT-23-THIN - 1.1 mm max height

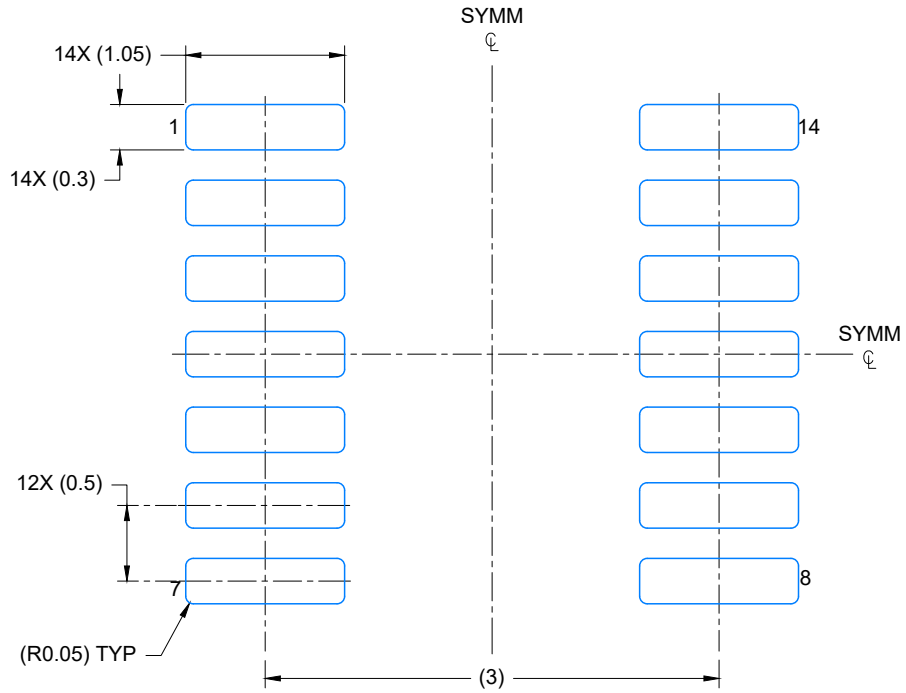
PLASTIC SMALL OUTLINE



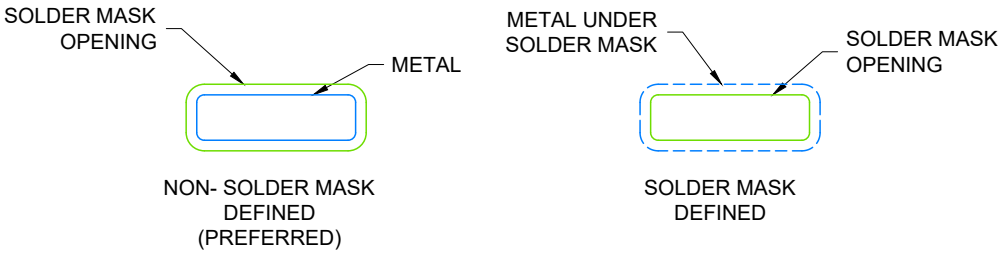
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224643/D 07/2024

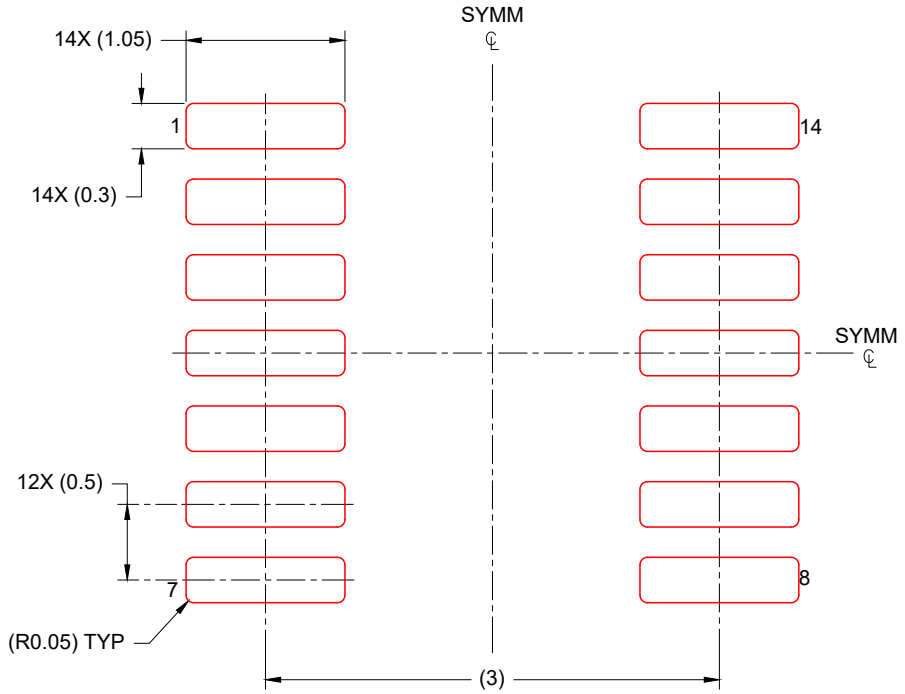
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

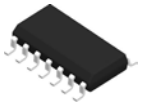


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

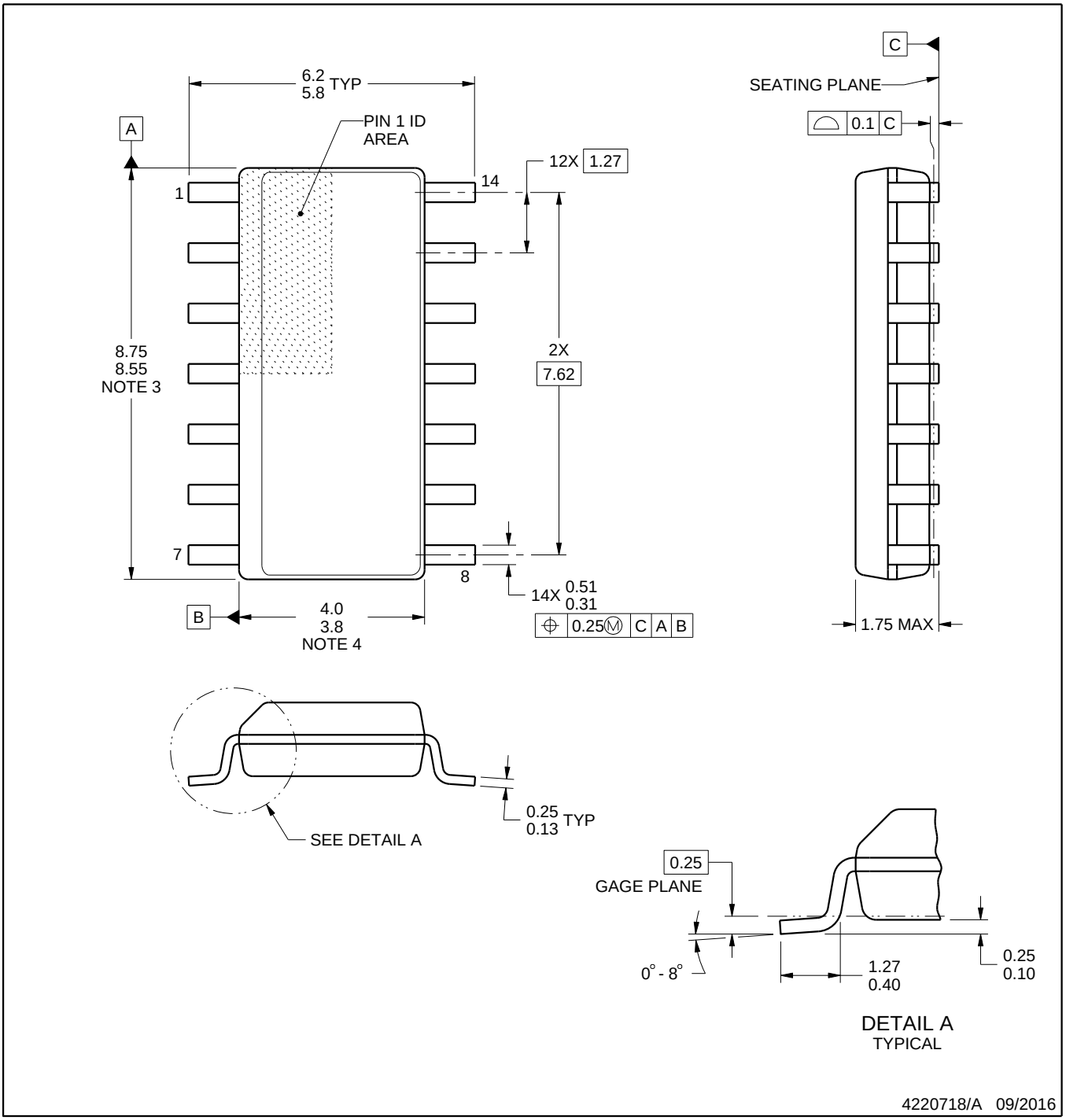


PACKAGE OUTLINE

D0014A

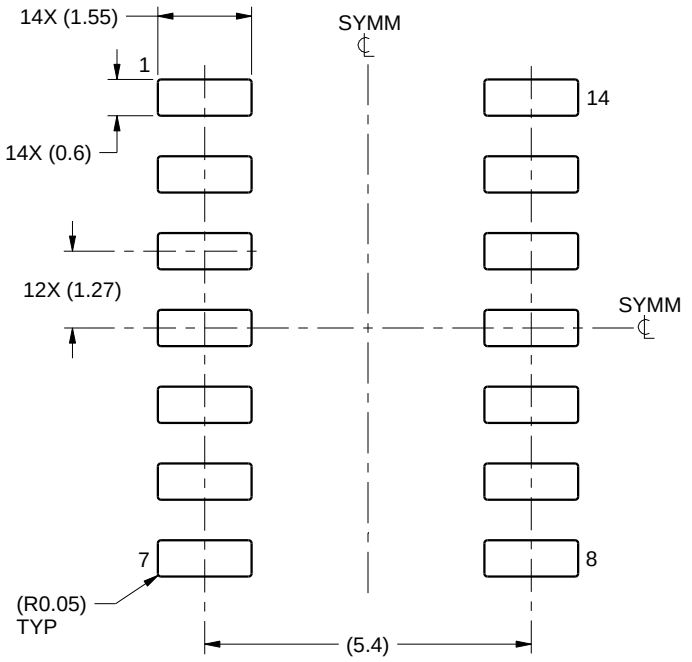
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

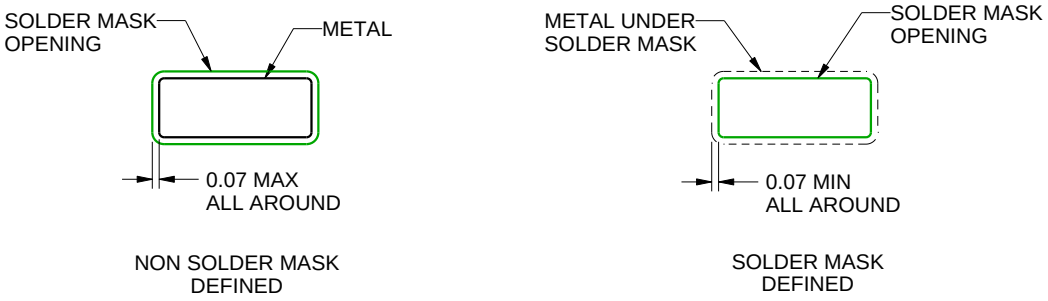


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

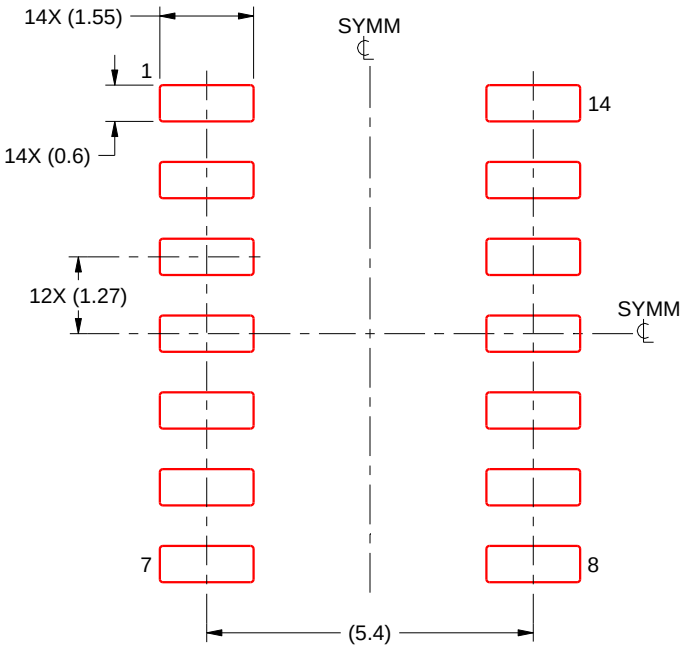
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

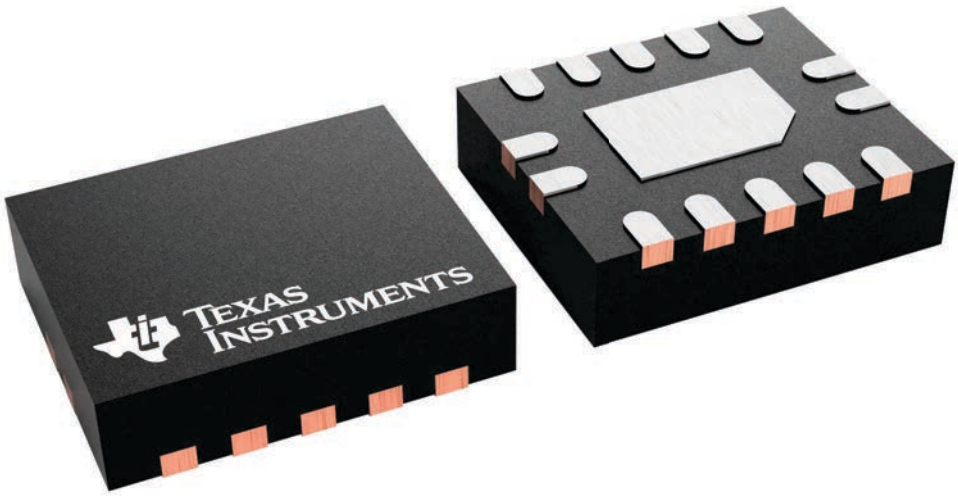
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



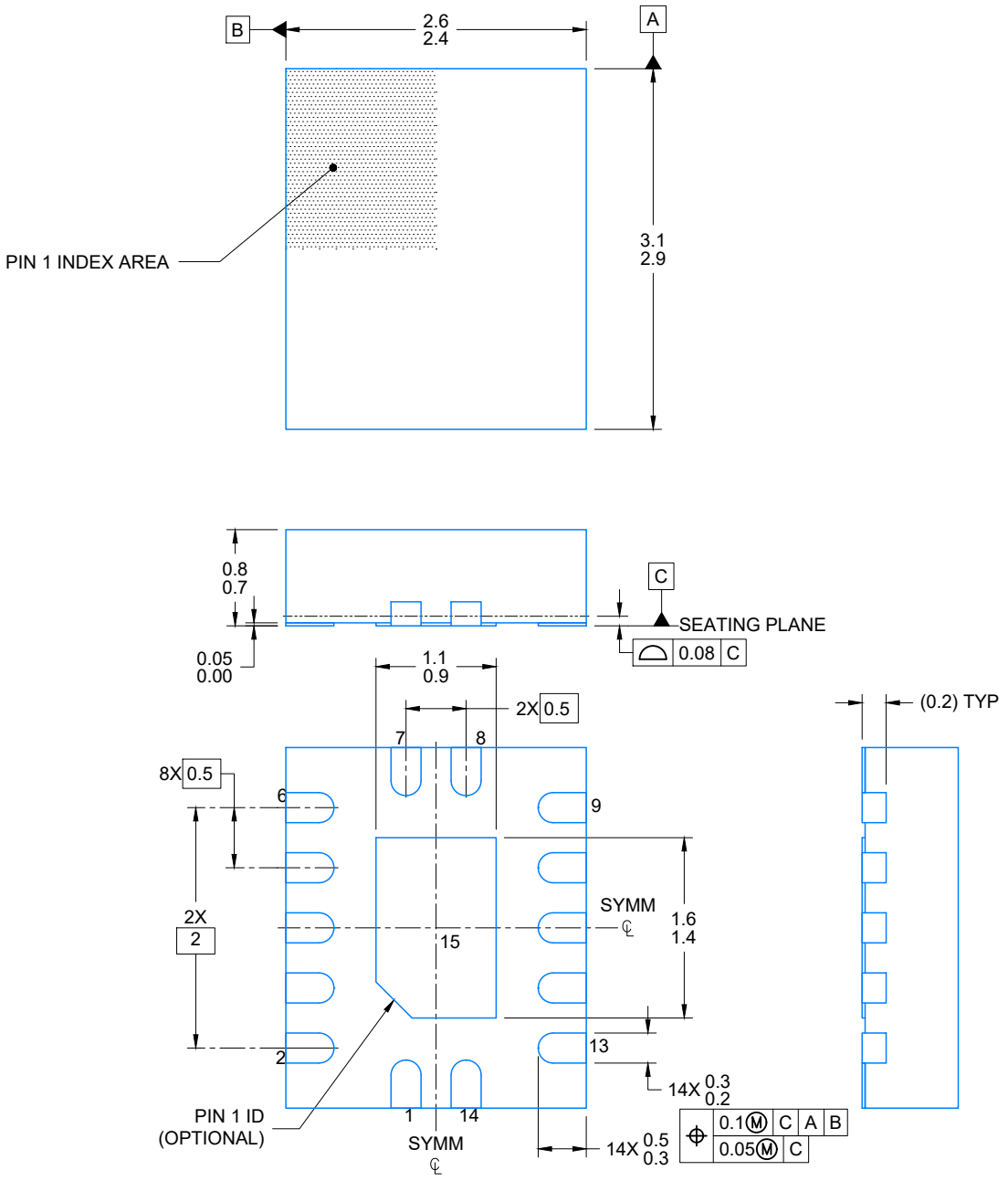
4227145/A

PACKAGE OUTLINE

BQA0014A

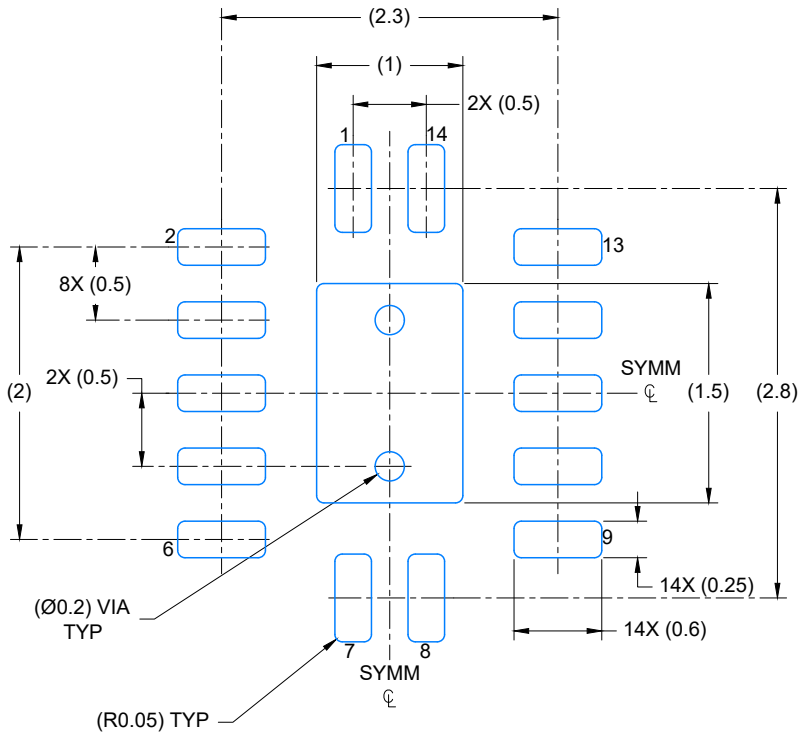
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

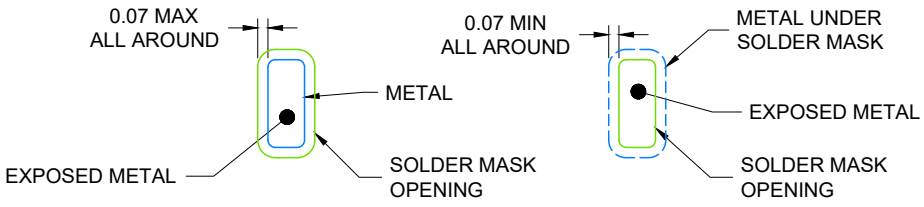


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



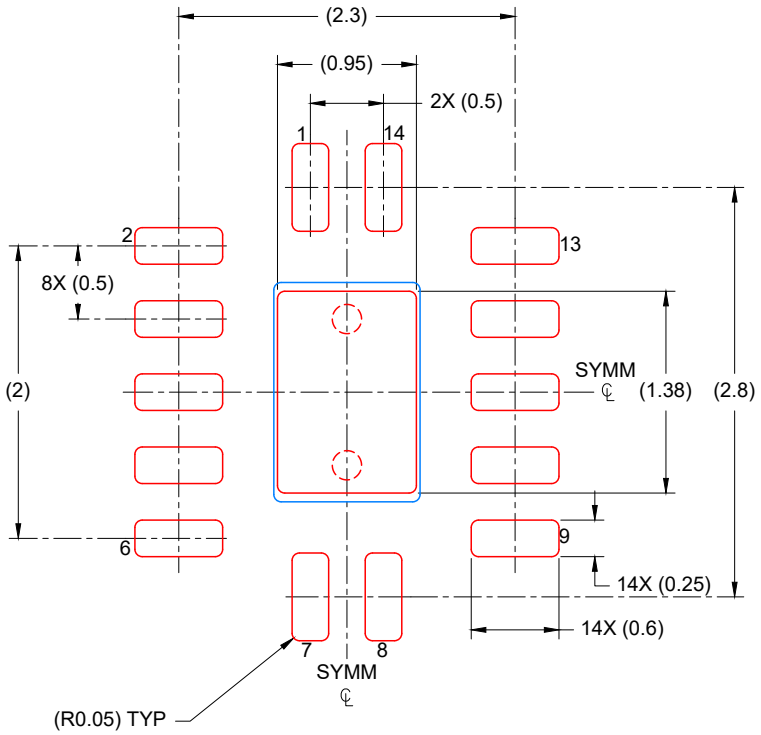
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

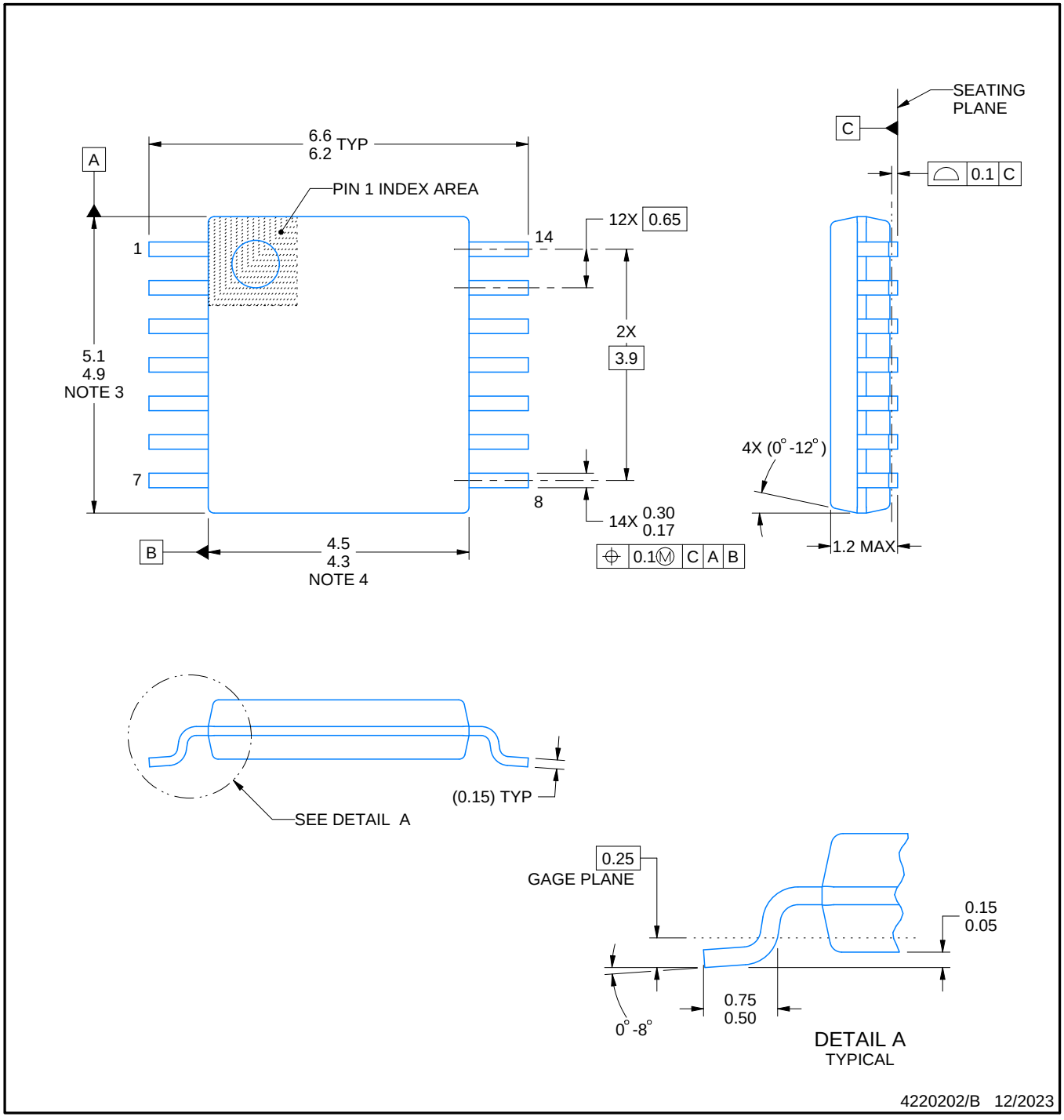
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

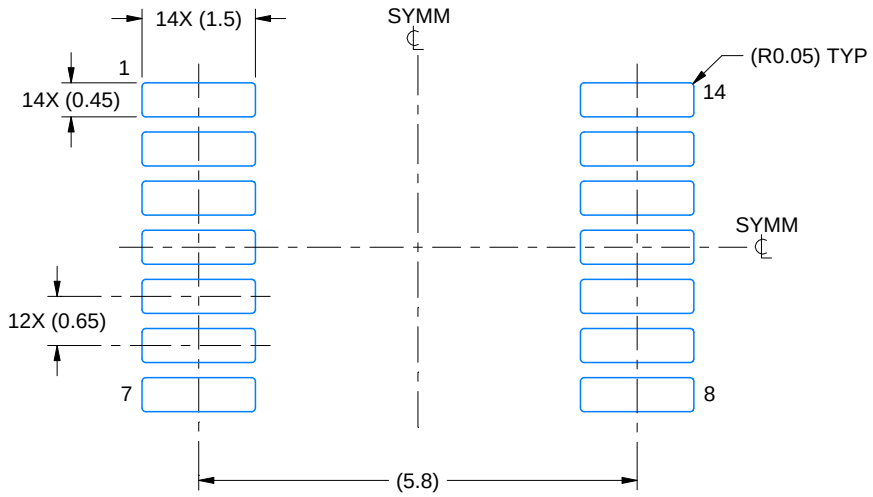
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

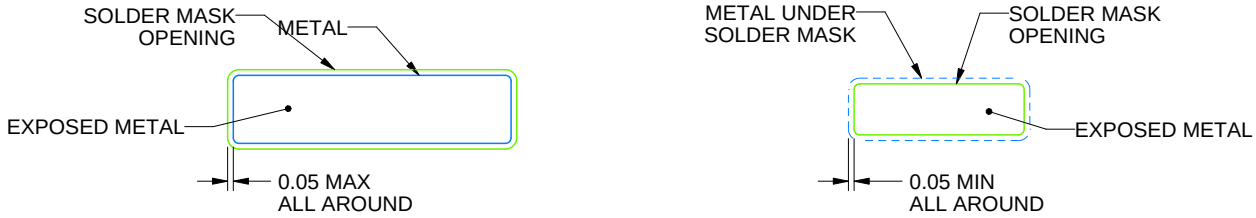


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

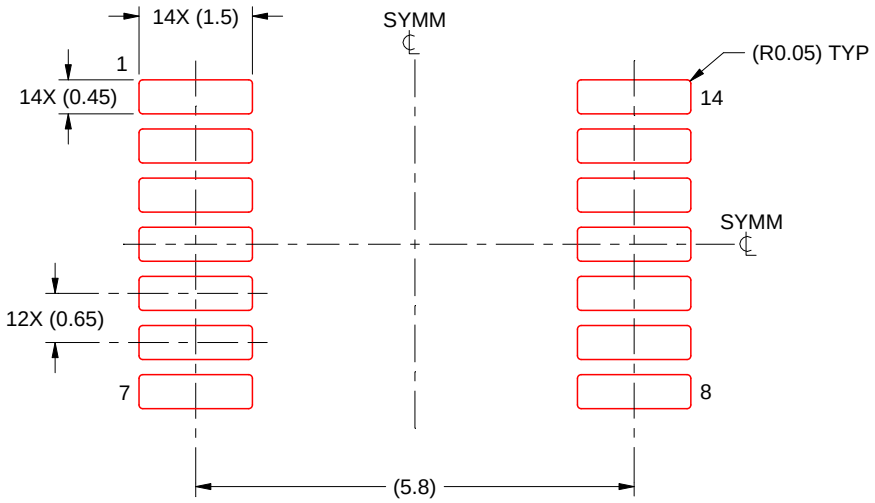


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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