

# SN54145, SN54LS145, SN74145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

SDLS051

MARCH 1974 - REVISED MARCH 1988

## FOR USE AS LAMP, RELAY, OR MOS DRIVERS

- Full Decoding of Input Logic
- SN54145, SN74145, and SN74LS145 Have 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions
- Low Power Dissipation of 'LS145 . . . 35 mW Typical

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

### description

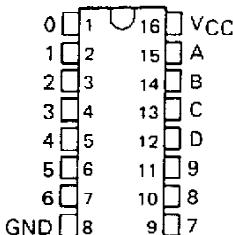
These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) of the SN54145, SN74145, or SN74LS145 will sink up to 80 milliamperes of current. Each input is one Series 54/74 or Series 54LS/74LS standard load, respectively. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts for the '145 and 35 milliwatts for the 'LS145.

SN54145, SN54LS145 . . . J OR W PACKAGE

SN74145 . . . N PACKAGE

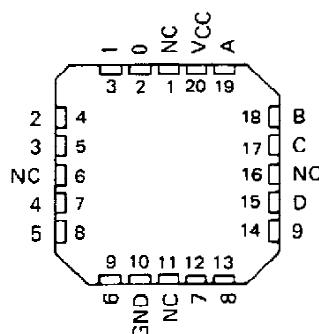
SN74LS145 . . . D OR N PACKAGE

(TOP VIEW)



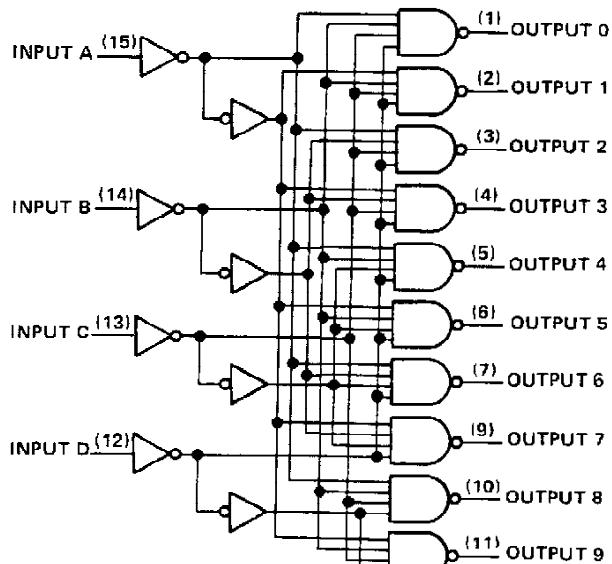
SN54LS145 . . . FK PACKAGE

(TOP VIEW)



NC = No internal connection

### logic diagram



Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN54LS145, SN74LS145 BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Maximum current into any output (off-state)	1 mA
Operating free-air temperature range: SN54145	-55°C to 125°C
SN74145	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54145			SN74145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(\text{off})}$		15			15		V
Operating free-air temperature, $T_A$	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage			0.8		V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$			-1.5	V
$I_{O(\text{off})}$ Off-state output current	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$ , $V_{O(\text{off})} = 15 \text{ V}$			250	μA
$V_{O(\text{on})}$ On-state output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$	0.5	0.9		V
		$I_{O(\text{on})} = 80 \text{ mA}$		0.4	
		$I_{O(\text{on})} = 20 \text{ mA}$			
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1		mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40	μA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$			-1.6	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ , See Note 2	SN54145	43	62	
		SN74145	43	70	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

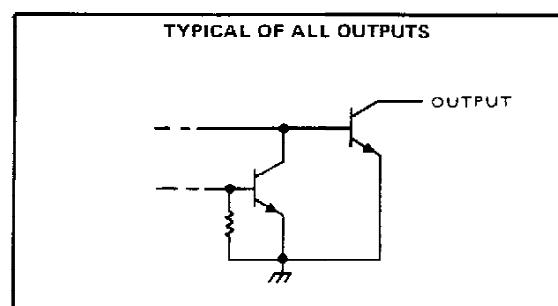
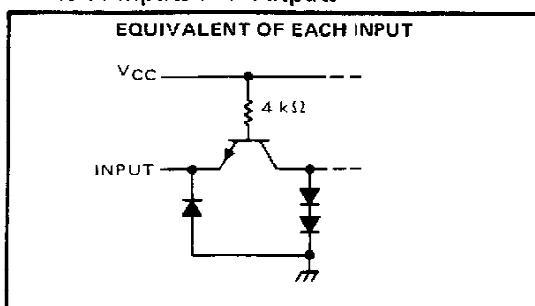
NOTE 2:  $I_{CC}$  is measured with all inputs grounded and outputs open.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF}$ , $R_L = 100 \Omega$ , See Note 3		50	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output			50	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## schematics of inputs and outputs



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## SN54145, SN74145 BCD-TO-DECIMAL DECODERS/DRIVERS

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

NOTE 1: Voltage values are with respect to network ground terminal.

### **recommended operating conditions**

	SN54LS145			SN74LS145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$			15			15	V
Operating free-air temperature, $T_A$	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>†</sup>	SN54LS145			SN74LS145			UNIT
		MIN	TYP <sup>‡</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
V <sub>IH</sub>	High-level input voltage			2		2		✓
V <sub>IL</sub>	Low-level input voltage			0.7		0.8		✓
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	✓
I <sub>O(off)</sub>	Off-state output current	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> max, V <sub>OH</sub> = 15 V		250		250		µA
V <sub>O(on)</sub>	On-state output voltage	V <sub>CC</sub> = MIN, I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4		✓
		V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 24 mA			0.35	0.5		
		V <sub>IL</sub> = V <sub>IL</sub> max, I <sub>OL</sub> = 80 mA			2.3	3		
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1		0.1		mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20		20		µA
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.4		-0.4		mA
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX, See Note 2	7	13	7	13		mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

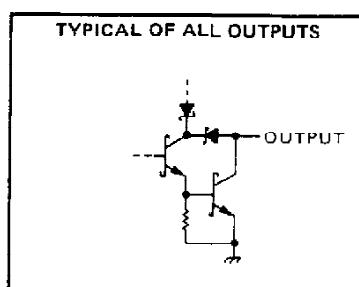
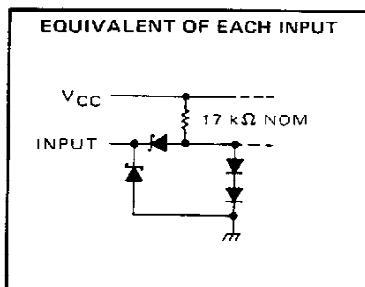
NOTE 2:  $I_{CC}$  is measured with all inputs grounded and outputs open.

switching characteristics,  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$C_L = 45 \text{ pF}$ , $R_L = 665 \Omega$ , See Note 3	50	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output		50	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

### **schematic of inputs and outputs**



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**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8508401VEA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8508401VE A SNV54LS145J
5962-8508401VEA.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8508401VE A SNV54LS145J
85084012A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85084012A SNJ54LS 145FK
8508401EA	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401EA SNJ54LS145J
8508401FA	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401FA SNJ54LS145W
SN54LS145J	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS145J
SN54LS145J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS145J
SN74145N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74145N
SN74145N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74145N
SN74LS145D	Obsolete	Production	SOIC (D)   16	-	-	Call TI	Call TI	0 to 70	LS145
SN74LS145DR	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS145
SN74LS145DR.A	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS145
SN74LS145DRE4	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS145
SN74LS145N	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS145N
SN74LS145N.A	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS145N
SN74LS145NE4	Active	Production	PDIP (N)   16	25   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS145N
SN74LS145NSR	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS145
SN74LS145NSR.A	Active	Production	SOP (NS)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS145
SNJ54145J	Active	Production	CDIP (J)   16	1   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54145J
SNJ54145J.A	Active	Production	CDIP (J)   16	1   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54145J
SNJ54LS145FK	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85084012A SNJ54LS 145FK

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS145FK.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	85084012A SNJ54LS 145FK
<a href="#">SNJ54LS145J</a>	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401EA SNJ54LS145J
SNJ54LS145J.A	Active	Production	CDIP (J)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401EA SNJ54LS145J
<a href="#">SNJ54LS145W</a>	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401FA SNJ54LS145W
SNJ54LS145W.A	Active	Production	CFP (W)   16	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8508401FA SNJ54LS145W

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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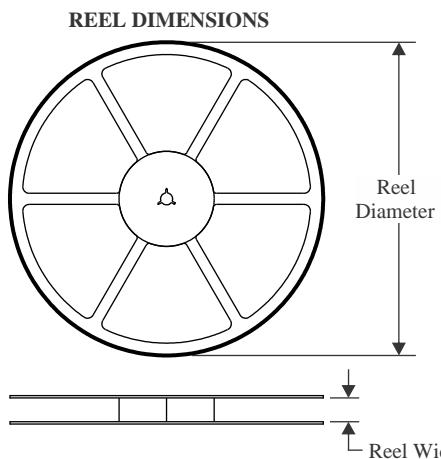
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54145, SN54LS145, SN54LS145-SP, SN74145, SN74LS145 :**

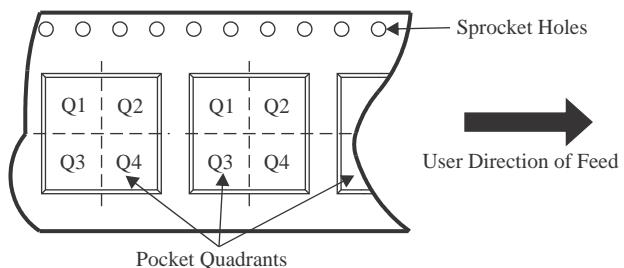
- Catalog : [SN74145](#), [SN74LS145](#), [SN54LS145](#)
- Military : [SN54145](#), [SN54LS145](#)
- Space : [SN54LS145-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

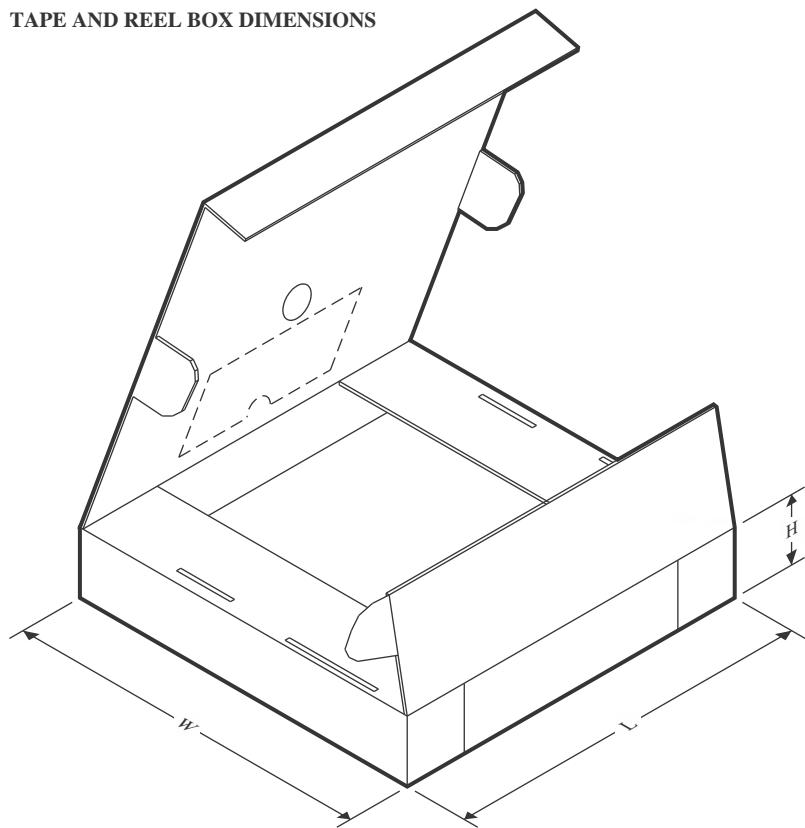
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


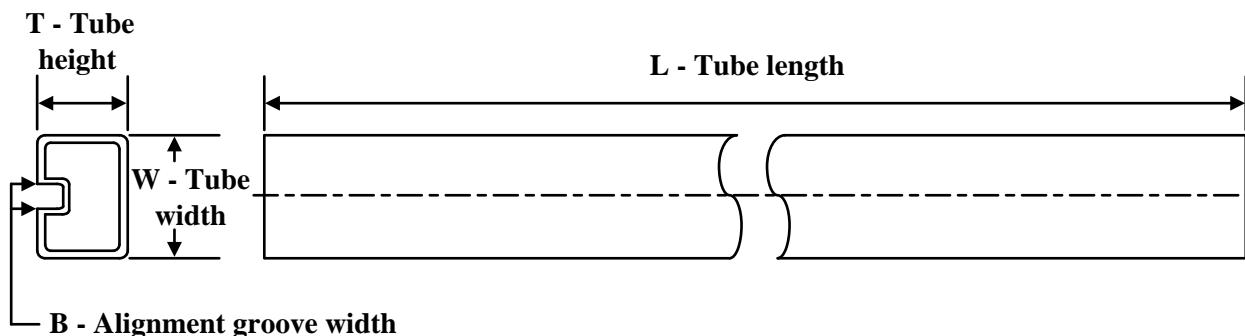
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS145DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS145NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LS145NSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS145DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LS145NSR	SOP	NS	16	2000	353.0	353.0	32.0
SN74LS145NSR	SOP	NS	16	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

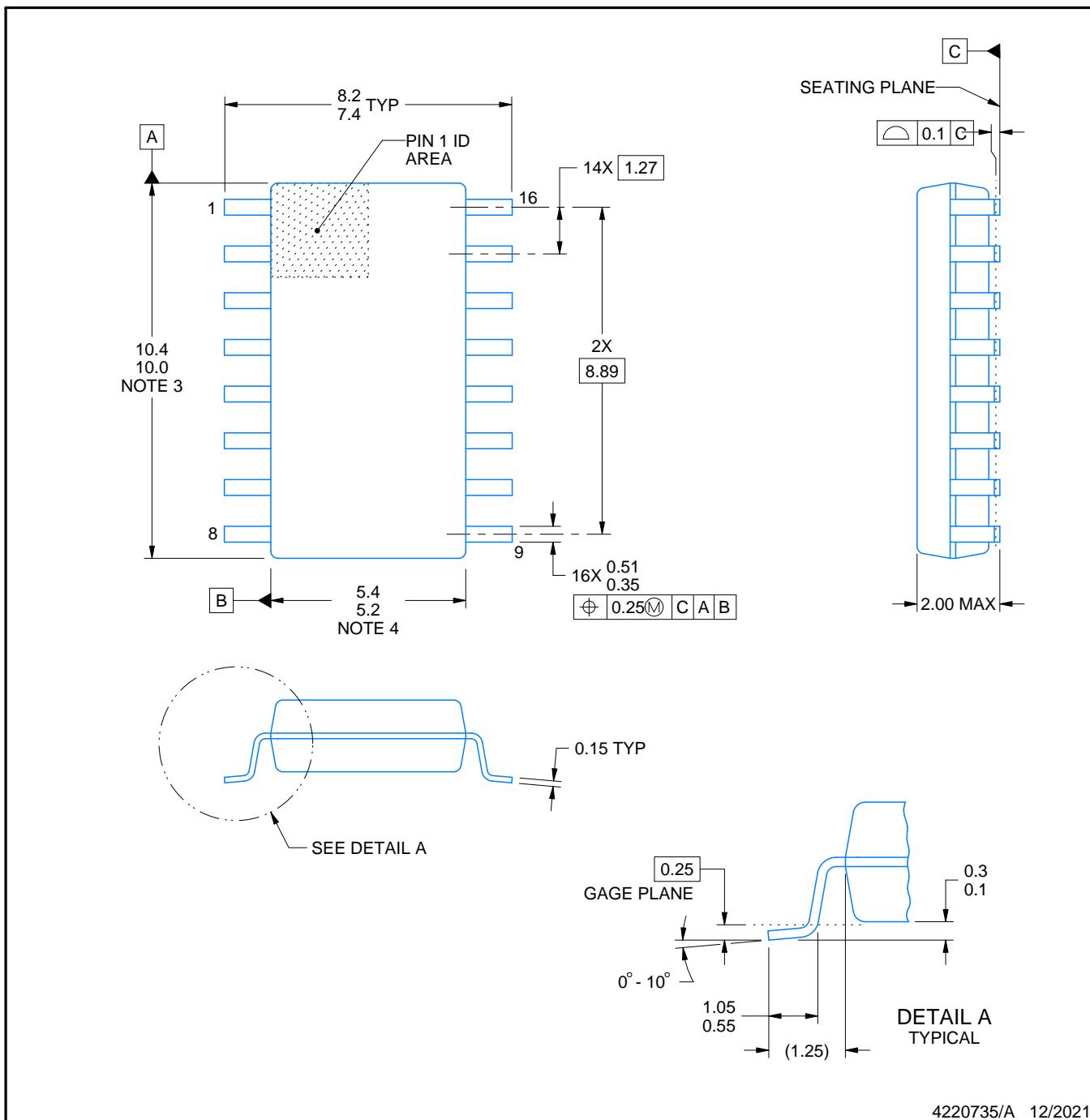
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
85084012A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74145N	N	PDIP	16	25	506	13.97	11230	4.32
SN74145N	N	PDIP	16	25	506	13.97	11230	4.32
SN74145N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74145N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145NE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS145NE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS145FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS145FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA



# PACKAGE OUTLINE

## SOP - 2.00 mm max height

SOP



### NOTES:

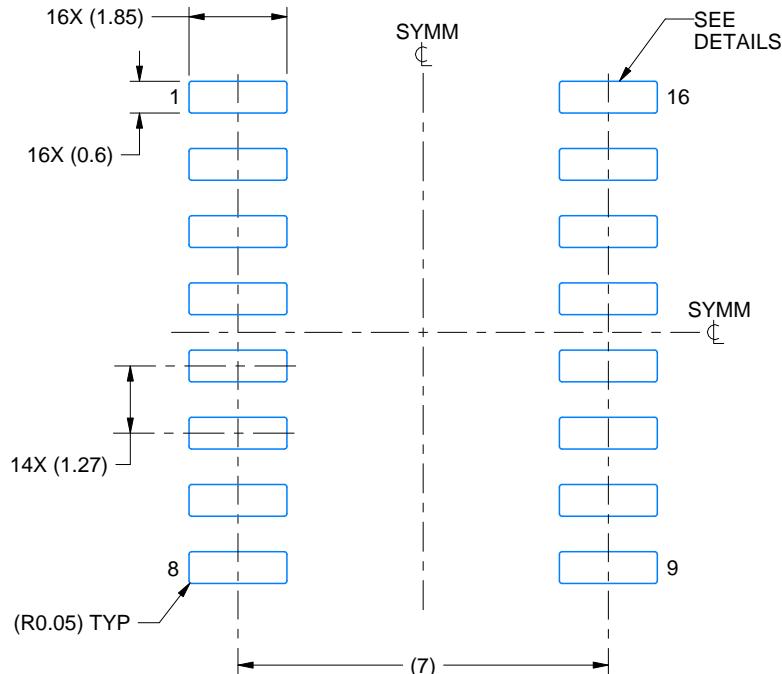
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

# EXAMPLE BOARD LAYOUT

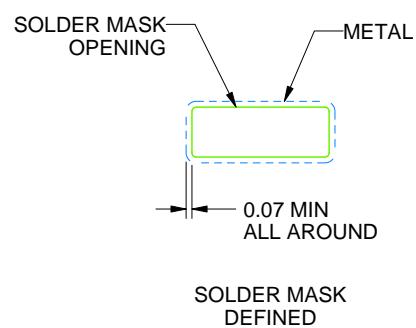
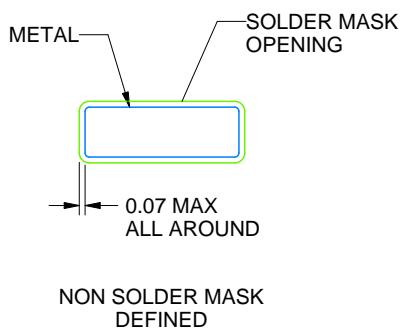
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE  
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

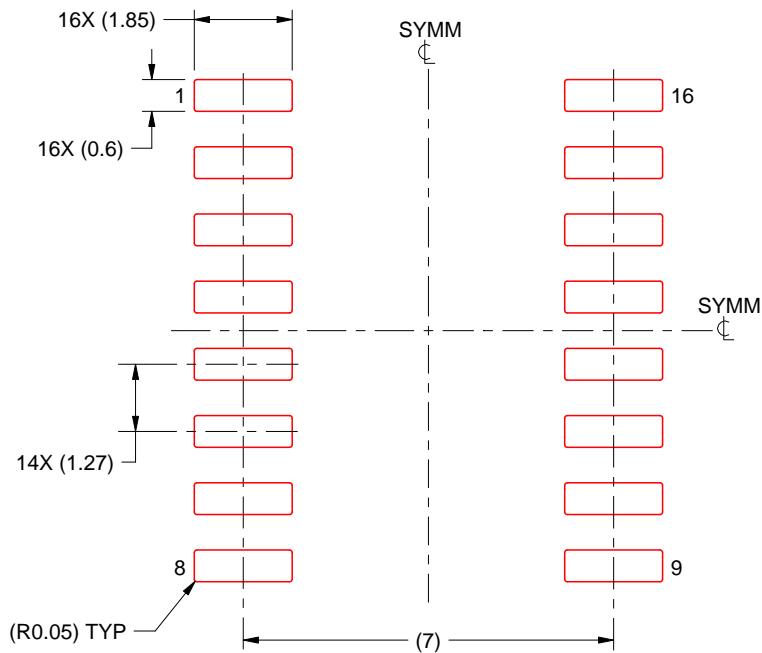
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

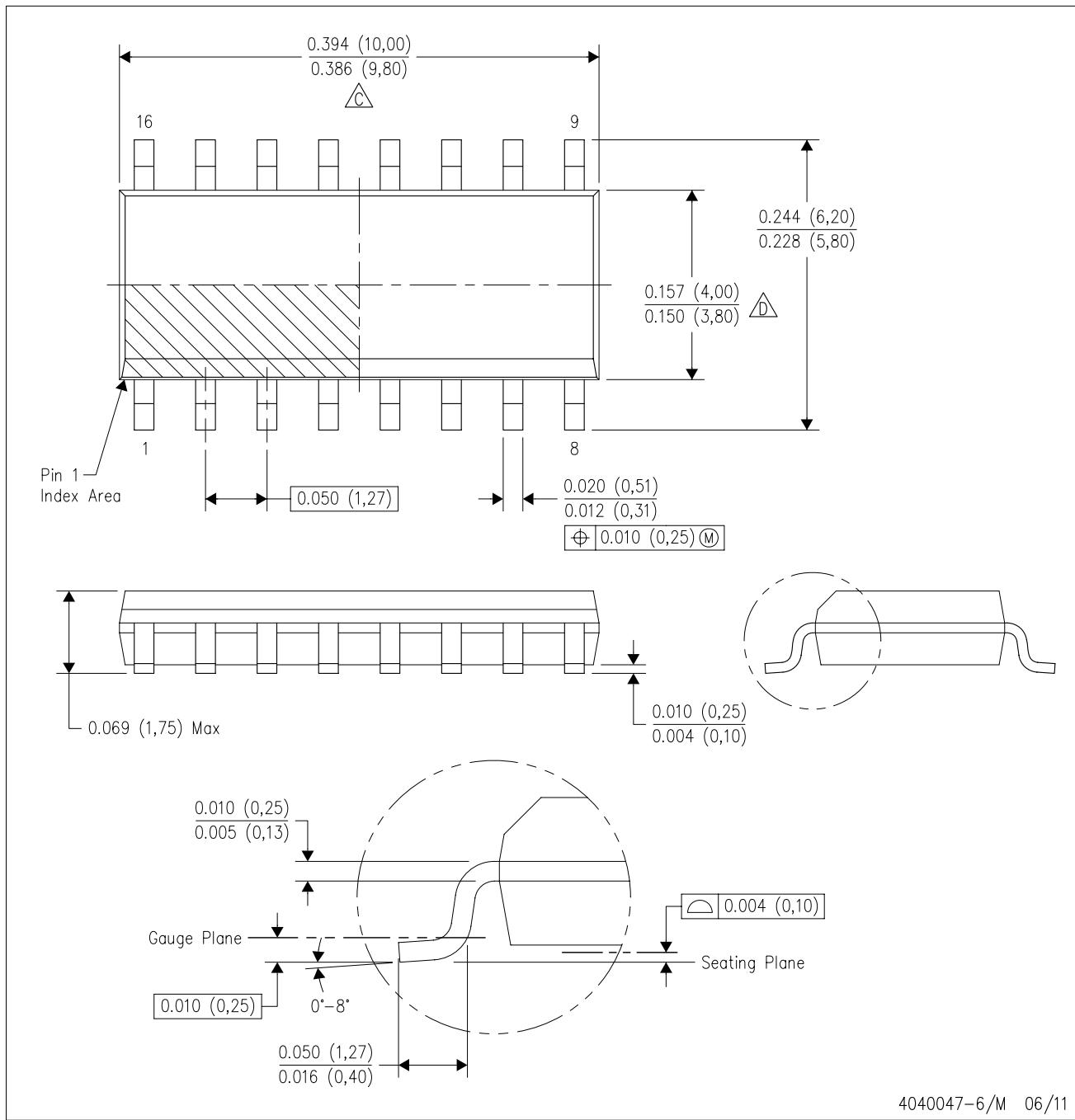
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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

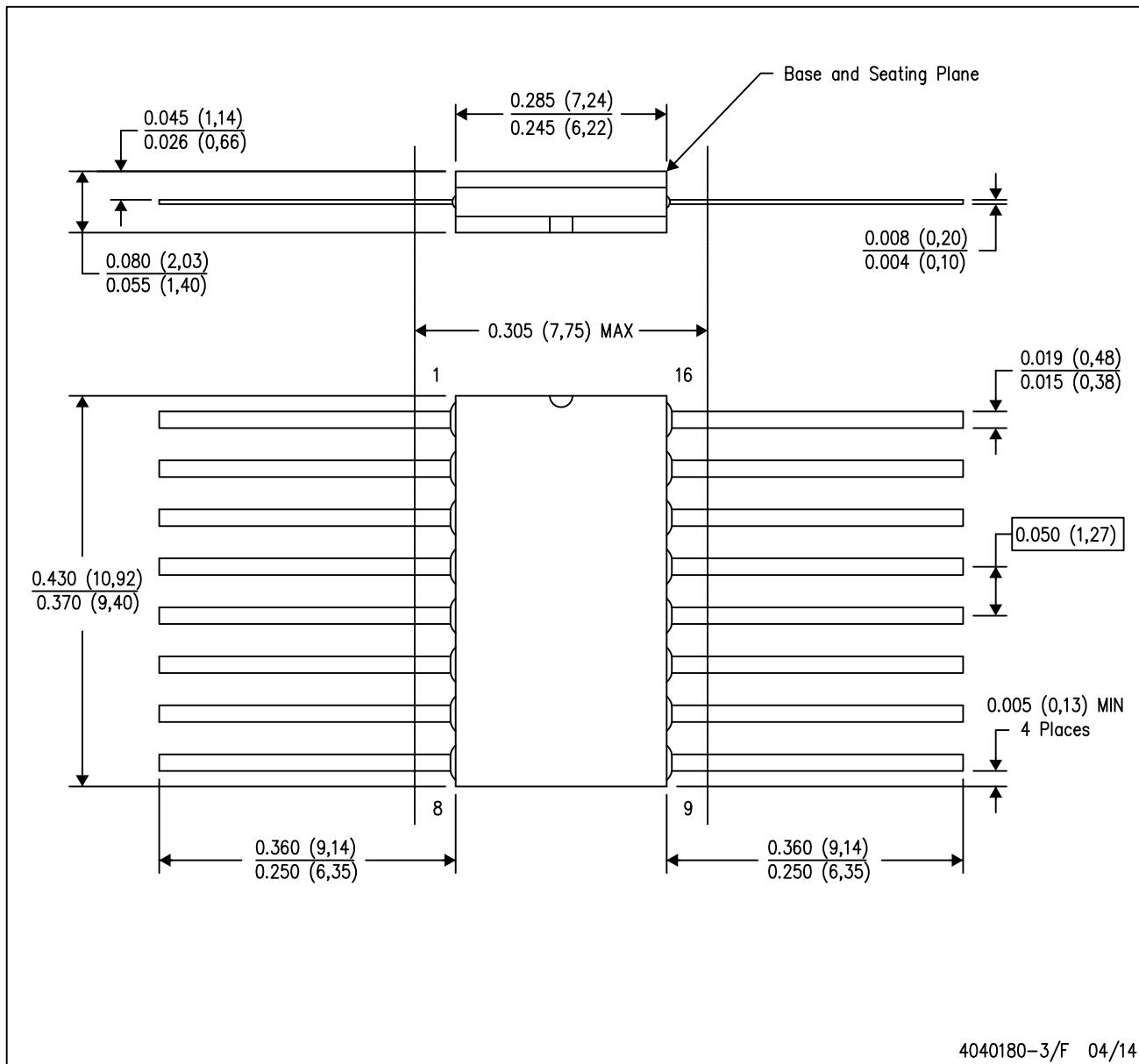
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

# GENERIC PACKAGE VIEW

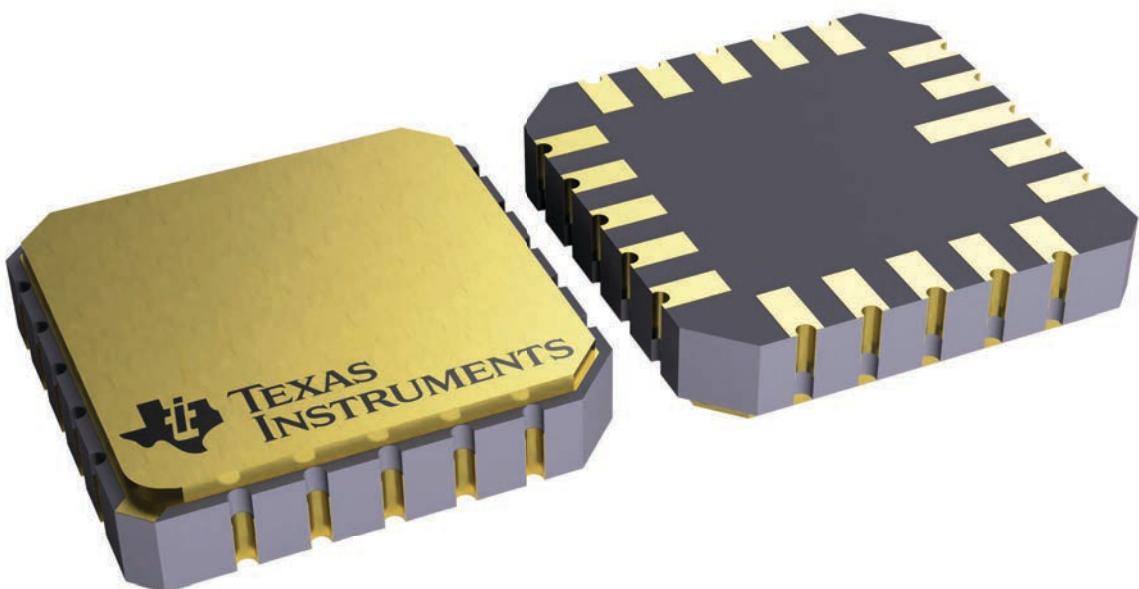
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

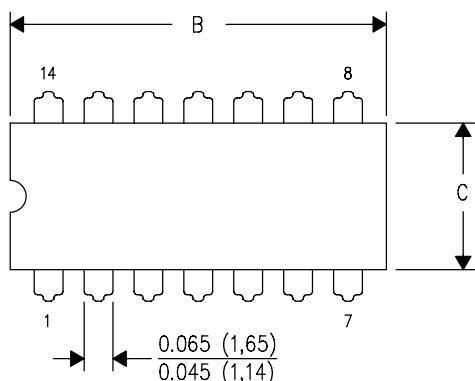


4229370VA\

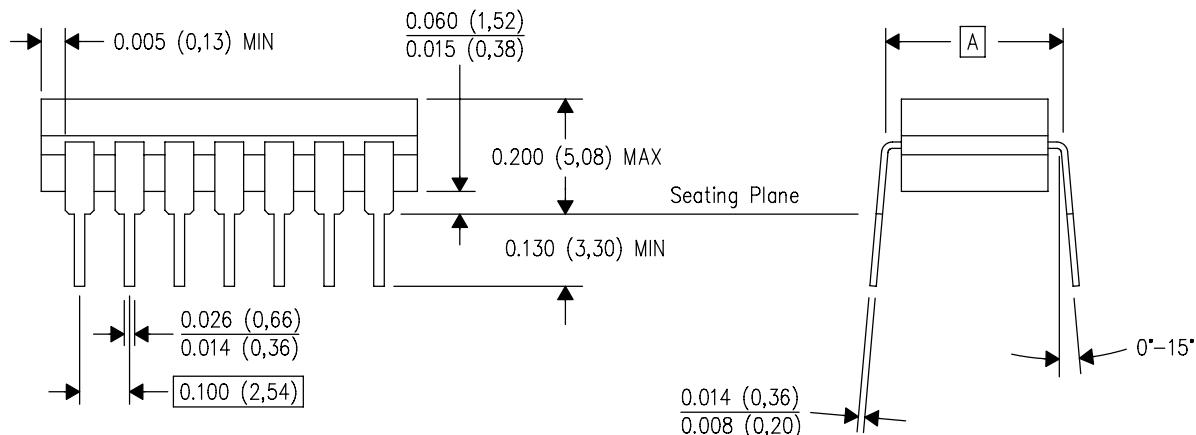
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package is hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.  
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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