

SN54173, SN54LS173A, SN74173, SN74LS173A

4-BIT D-TYPE REGISTERS

WITH 3-STATE OUTPUTS

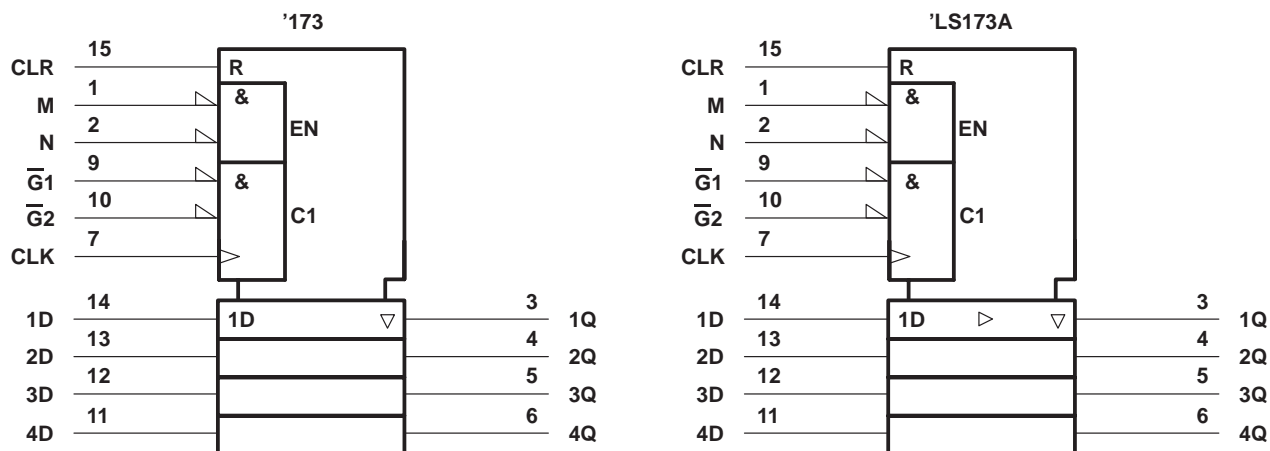
SDLS067A – OCTOBER 1976 – REVISED JUNE 1999

FUNCTION TABLE

CLR	CLK	INPUTS			OUTPUT Q
		DATA ENABLE		DATA D	
		$\overline{G1}$	$\overline{G2}$		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	\uparrow	H	X	X	Q_0
L	\uparrow	X	H	X	Q_0
L	\uparrow	L	L	L	L
L	\uparrow	L	L	H	H

When either M or N (or both) is (are) high, the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

logic symbol†

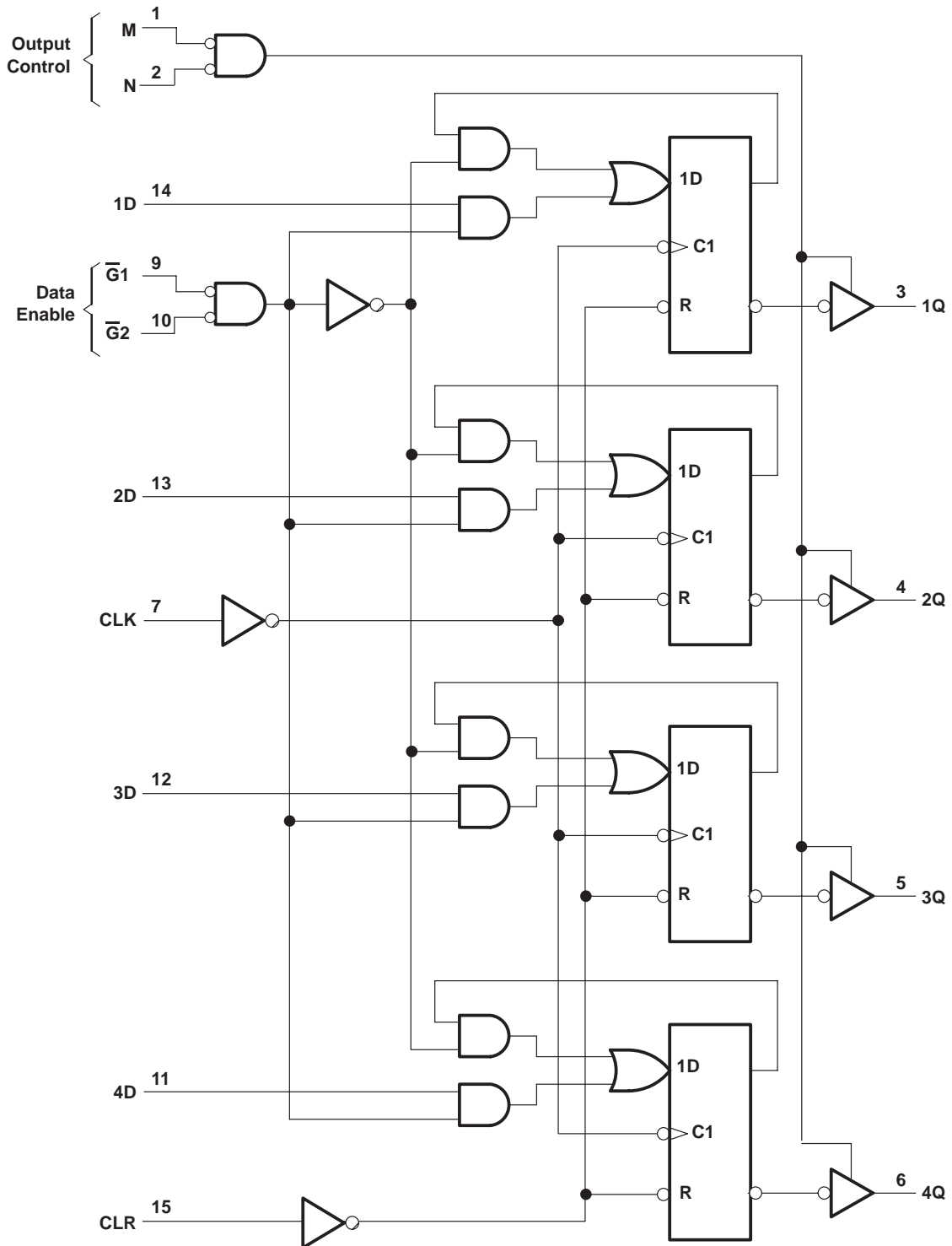


† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

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recommended operating conditions (see Note 3)

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-2			-5.2	mA
I _{OL}	Low-level output current			16			16	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54173			SN74173			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.8			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -12 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = MAX	2.4			2.4			V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OL} = 16 mA			0.4			0.4	V
I _{O(off)}	Off-state (high-impedance state) output current	V _{CC} = MAX, V _{IH} = 2 V	V _O = 2.4 V			150			40	μA
			V _O = 0.4 V			-150			-40	
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 5.5 V			1			1	mA
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.4 V			40			40	μA
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V			-1.6			-1.6	mA
I _{OS}	Short-circuit output current§	V _{CC} = MAX		-30		-70	-30		-70	mA
I _{CC}	Supply current	V _{CC} = MAX,	See Note 4	50		72	50		72	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G1}$, $\overline{G2}$, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

		SN54173		SN74173		UNIT	
		MIN	MAX	MIN	MAX		
f _{clock}	Input clock frequency		25		25	MHz	
t _w	Pulse duration		20		20	ns	
t _{su}	Setup time			Data enable ($\overline{G1}$, $\overline{G2}$)	17	17	ns
				Data	10	10	
				CLR (inactive state)	10	10	
t _h	Hold time			Data enable ($\overline{G1}$, $\overline{G2}$)	2	2	ns
				Data	10	10	



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 400\ \Omega$ (see Figure 1)

PARAMETER	TEST CONDITIONS	SN54173			SN74173			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum clock frequency	25	35		25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input		18	27		18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input		28	43		28	43	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input		19	31		19	31	
t_{PZH}	Output enable time to high level	7	16	30	7	16	30	ns
t_{PZL}	Output enable time to low level	7	21	30	7	21	30	
t_{PHZ}	Output disable time from high level	3	5	14	3	5	14	ns
t_{PLZ}	Output disable time from low level	3	11	20	3	11	20	



SN54173, SN54LS173A, SN74173, SN74LS173A 4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

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recommended operating conditions

		SN54LS173A			SN74LS173A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS173A			SN74LS173A			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT	
V _{IH}	High-level input voltage	2			2			V	
V _{IL}	Low-level input voltage	0.7			0.8			V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5			V	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax} , I _{OH} = MAX			2.4 3.4			V	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OL} = 12 mA		0.25 0.4		0.25 0.4		V	
		I _{OL} = 24 mA				0.35 0.5		V	
I _{O(off)}	Off-state (high-impedance state) output current	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V		20		20		V	
		V _O = 0.4 V		-20		-20			
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V			0.1			mA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V			20			μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-0.4			mA	
I _{OS}	Short-circuit output current§	V _{CC} = MAX			-30 -130		-30 -130		mA
I _{CC}	Supply current	V _{CC} = MAX, See Note 4			19 30		19 24		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 4: I_{CC} is measured with all outputs open; CLR grounded, following momentary connection to 4.5 V, N, $\overline{G1}$, $\overline{G2}$, and all data inputs grounded; and CLK and M at 4.5 V.

timing requirements over recommended operating conditions (unless otherwise noted)

		SN54LS173A		SN74LS173A		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Input clock frequency	30		25		MHz
t _w	Pulse duration	CLK or CLR		25		ns
t _{su}	Setup time	Data enable ($\overline{G1}$, $\overline{G2}$)		35		ns
		Data		17		
		CLR (inactive state)		10		
t _h	Hold time	Data enable ($\overline{G1}$, $\overline{G2}$)		0		ns
		Data		3		



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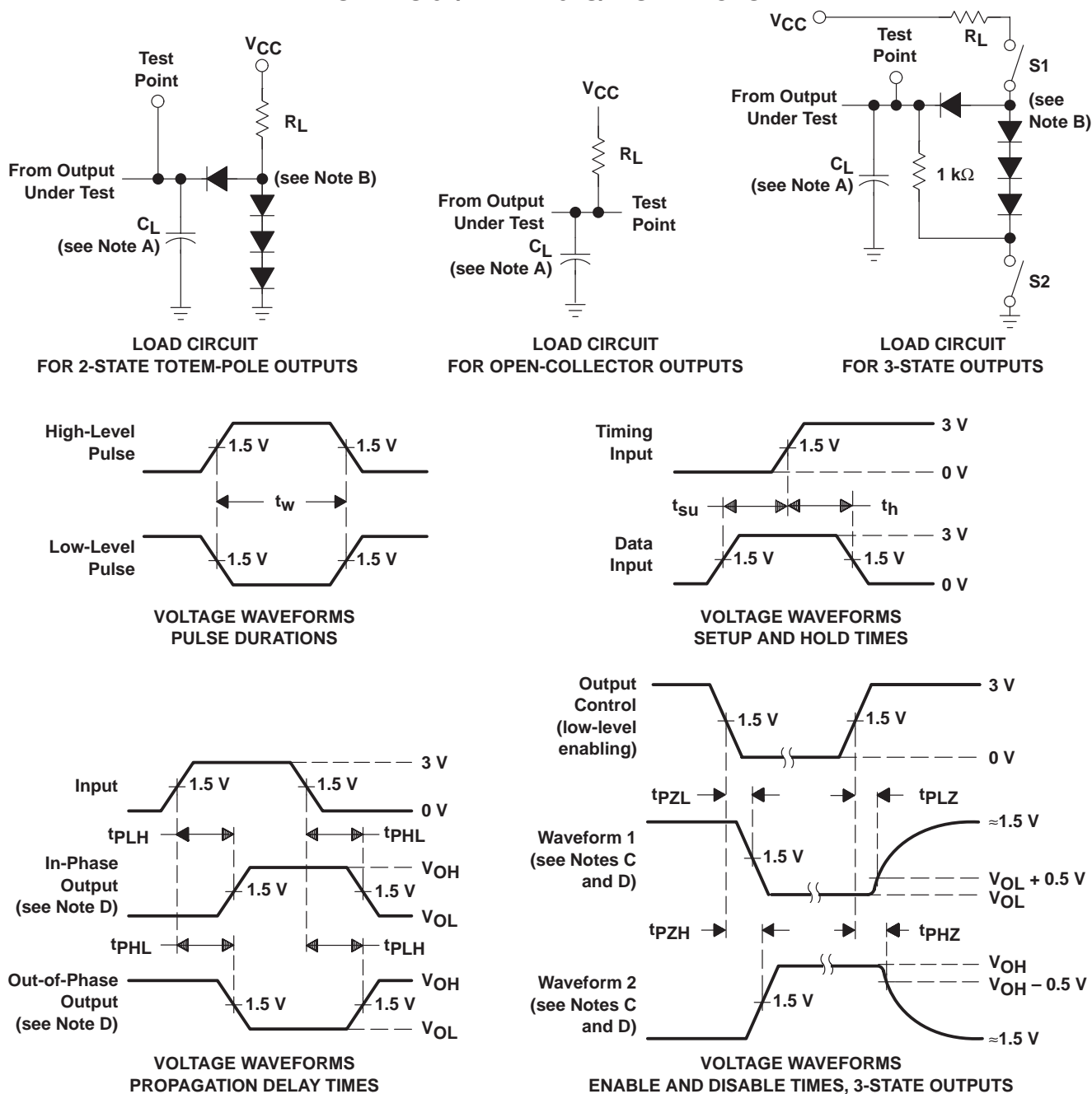
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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $R_L = 667\ \Omega$ (see Figure 2)

PARAMETER		TEST CONDITIONS	SN54LS173A			SN74LS173A			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
f_{max}	Maximum clock frequency	$C_L = 45\text{ pF}$	30	50		30	50		MHz	
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			26	35		26	35		ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			17	25		17	25		ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			22	30		22	30		
t_{PZH}	Output enable time to high level			15	23		15	23		ns
t_{PZL}	Output enable time to low level			18	27		18	27		
t_{PHZ}	Output disable time from high level	$C_L = 5\text{ pF}$		11	20		11	20	ns	
t_{PLZ}	Output disable time from low level			11	17		11	17		



PARAMETER MEASUREMENT INFORMATION
 SERIES 54/74 AND 54S/74S DEVICES



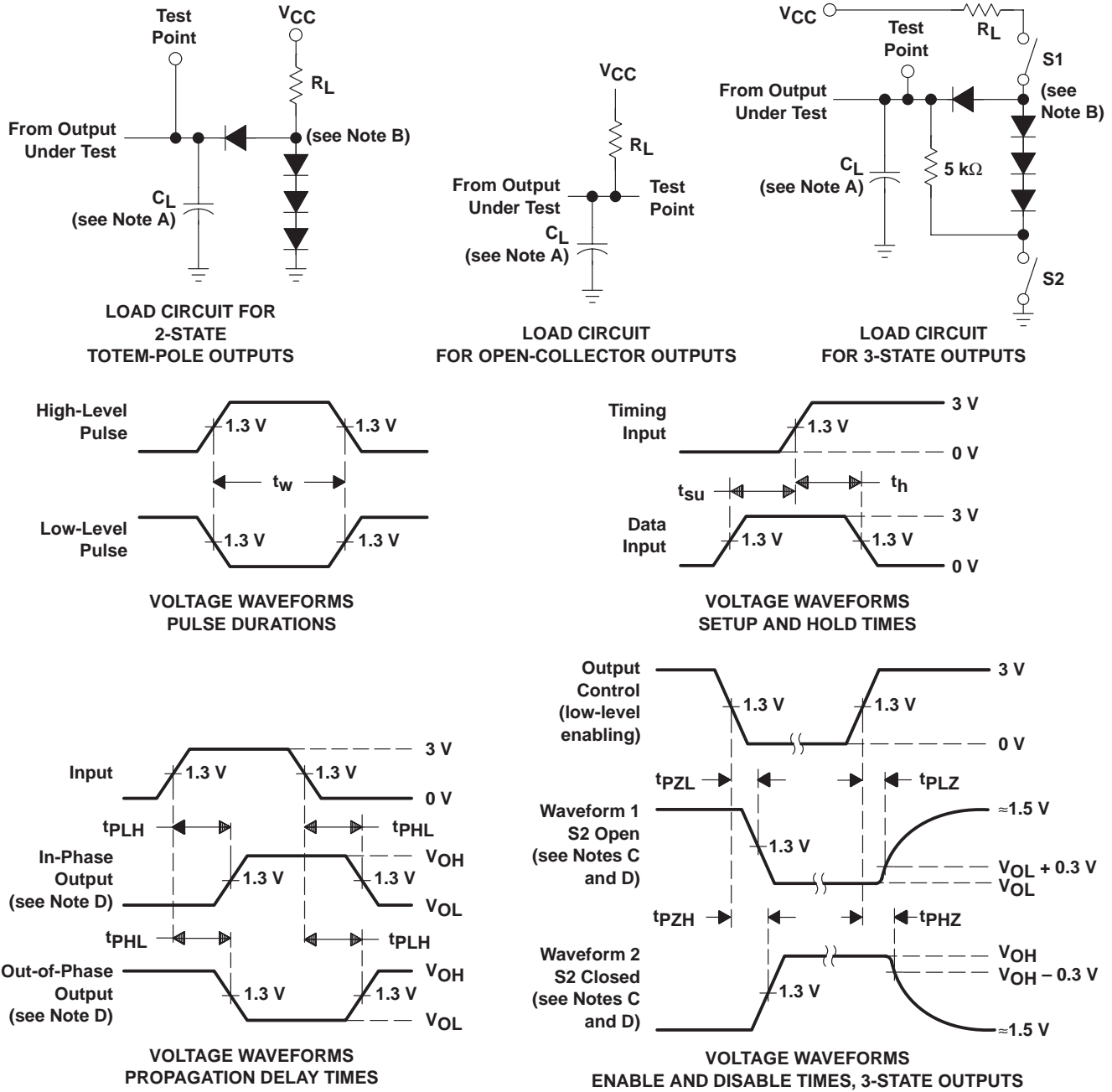
- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O \approx 50 \Omega$, t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
 F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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4-BIT D-TYPE REGISTERS
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
JM38510/36101BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
JM38510/36101BEA.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
JM38510/36101BFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
JM38510/36101BFA.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
M38510/36101BEA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BEA
M38510/36101BFA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 36101BFA
SN54173J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54173J
SN54173J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54173J
SN54LS173AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS173AJ
SN54LS173AJ.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS173AJ
SN74LS173AD	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS173A
SN74LS173AD.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS173A
SN74LS173AN	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS173AN
SN74LS173AN.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS173AN
SNJ54173J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54173J
SNJ54173J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54173J
SNJ54LS173AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 173AFK
SNJ54LS173AFK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 173AFK
SNJ54LS173AJ	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS173AJ
SNJ54LS173AJ.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS173AJ

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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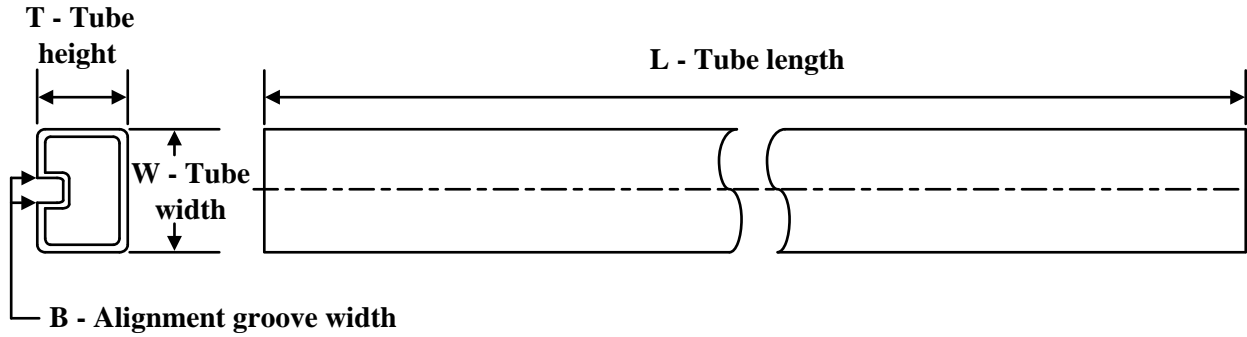
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OTHER QUALIFIED VERSIONS OF SN54LS173A, SN74LS173A :

- Catalog : [SN74LS173A](#)
- Military : [SN54LS173A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
JM38510/36101BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/36101BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/36101BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS173AD	D	SOIC	16	40	507	8	3940	4.32
SN74LS173AD.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS173AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS173AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS173AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

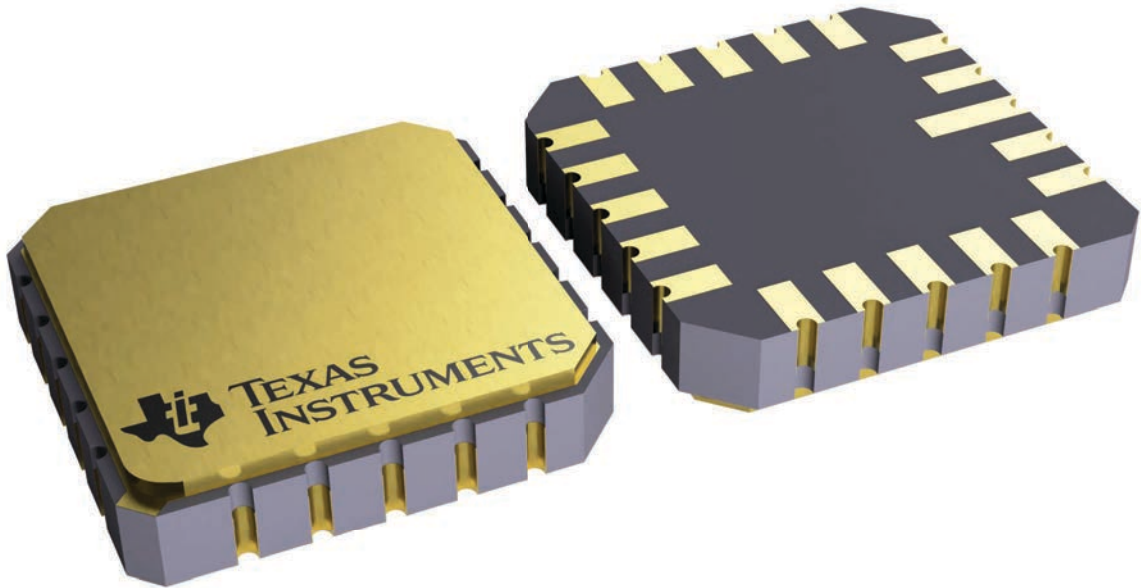
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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