

SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS175 D2536, JANUARY 1980 — REVISED MARCH 1988

- Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- 'LS422 Has Internal Timing Resistor

description

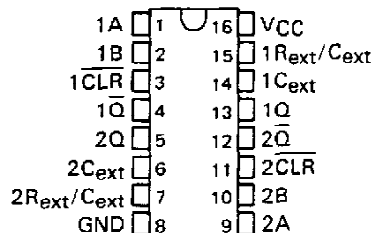
The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

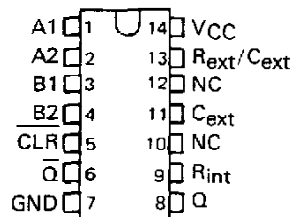
The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond. The 'LS422 R_{int} is nominally 10 k ohms.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS422 and SN74LS423 are characterized for operation from 0°C to 70°C .

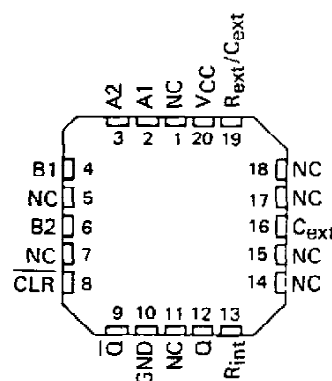
SN54LS423 . . . J OR W PACKAGE
SN74LS423 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



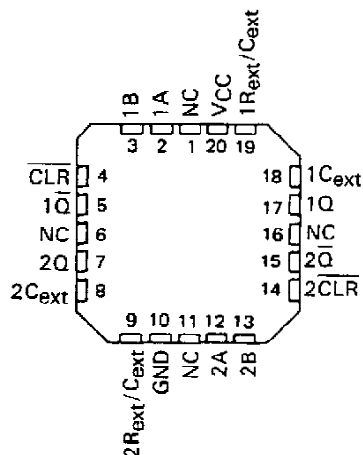
SN54LS422 . . . J OR W PACKAGE
SN74LS422 . . . D OR N PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS422 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS423 . . . FK PACKAGE
(TOP VIEW) (SEE NOTES 1 THRU 4)



- NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. To use the internal timing resistor of 'LS422, connect R_{int} to V_{CC} .
3. For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
4. To obtain variable pulse widths, connect an external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC} .

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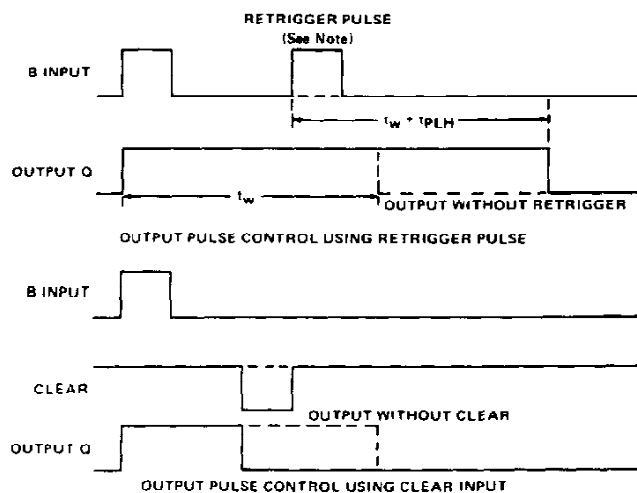
SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

description (continued)

LS422							
FUNCTION TABLE							
INPUTS				OUTPUTS			
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$	
L	X	X	X	X	L	H	
X	H	H	X	X	L†	H†	
X	X	X	L	X	L†	H†	
X	X	X	X	L	L†	H†	
H	L	X	↑	H			
H	L	X	H	↑			
H	X	L	↑	H			
H	X	L	H	↑			
X	H	↓	H	H			
X	↓	↓	H	H			
X	↓	H	H	H			

LS423					
FUNCTION TABLE					
INPUTS			OUTPUTS		
CLEAR	A	B	Q	$\bar{Q}$	
L	X	X	L	H	
X	H	X	L†	H†	
X	X	L	L†	H†	
H	L	↑			
H	X	H			

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

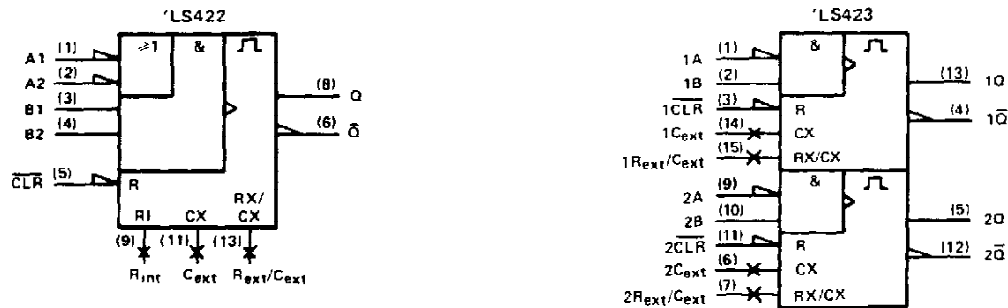


NOTE: Retrigger pulses starting before $0.22 C_{ext}$ (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

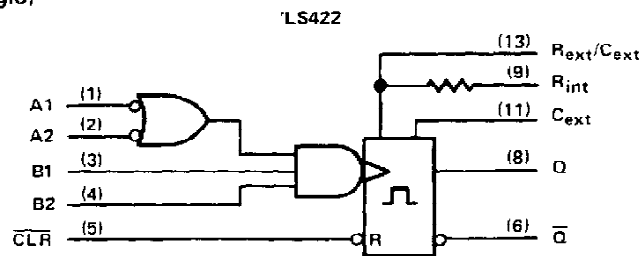
SN54LS422, SN54LS423, SN74LS422, SN74LS423 **RETRIGGERABLE MONOSTABLE MULTIVIBRATORS**

logic symbols†

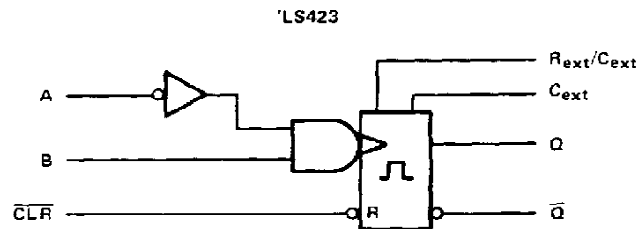


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagrams (positive logic)

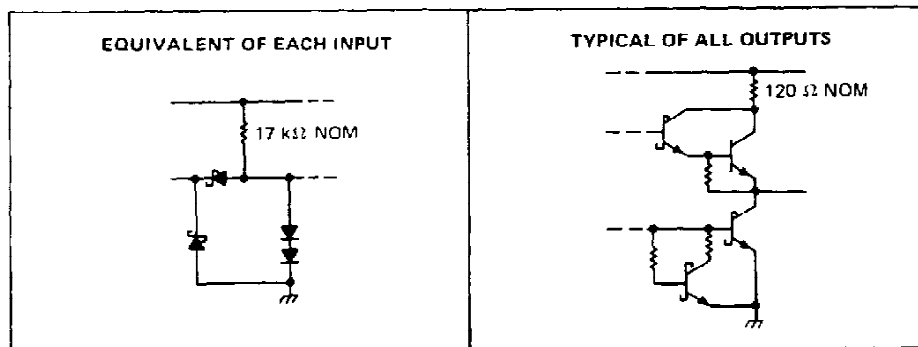


R_{int} is nominally 10 k ohms



Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs



SN54LS422, SN54LS423, SN74LS422, SN74LS423

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Pulse width, t_W	40			40			ns
External timing resistance, R_{ext}	5		180	5		260	k Ω
External capacitance, C_{ext}	No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal			50			50	pF
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS*			SN74LS*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage			2			2			V
V _{IL}	Low-level input voltage					0.7			0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN,	I _I = -18 mA			-1.5			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V, V _{IL} = V _{ILmax} I _{OH} = 400 µA	2.5	3.5		2.7	3.5		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = V _{ILmax}	V _{IH} = 2 V,	I _{OL} = 4 mA		0.25	0.4	0.25 0.4		V
				I _{OL} = 8 mA		0.35 0.5				
I _I	Input current at maximum input voltage	V _{CC} = MAX,	V _I = 7 V			0.1			0.1	mA
I _{IH}	High-level input current	V _{CC} = MAX,	V _I = 2.7 V			20			20	µA
I _{IL}	Low-level input current	V _{CC} = MAX,	V _I = 0.4 V			-0.4			-0.4	mA
I _{OS}	Short-circuit output current §	V _{CC} = MAX		-20		-100	-20		-100	mA
I _{CC}	Supply current (quiescent or triggered)	V _{CC} = MAX,	See Note 6	'LS422		6	11	6 11		mA
				'LS423		12	20	12 20		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 5. To measure V_{OH} at Q, V_{OL} at $\bar{Q}$, or I_{OS} at Q, ground R_{ext}/C_{ext} , apply 2 V to B and clear, and pulse A from 2 V to 0 V.

6. With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$, see note 7

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	A	Q	Cext = 0, Rext = 5 kΩ, CL = 15 pF, RL = 2 kΩ		23	33	ns
	B				23	44	
tPHL	A	Q̄			32	45	ns
	B				34	56	
tPHL	Clear	Q			20	27	ns
tPLH		Q̄			28	45	
tWQ (min)		Q			116	200	
tWQ	A or B	Q	Cext = 1000 pF, Rext = 10 kΩ, CL = 15 pF, RL = 2 kΩ	4	4.5	5	μs

¶ t_{wQ} = width of pulse output Q.

NOTE 7: Load circuits and voltage waveforms are shown in Section 1.

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TYPICAL APPLICATION DATA FOR 'LS422, 'LS423†

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000$ pF, use Figure 3. For C_{ext} between 0.1 nF and 1 μ F, the pulse width may be defined as:

$$t_w \approx K \cdot R_T \cdot C_{ext}$$

with K obtained from Figure 4.

When $C_{ext} \geq 1$ μ F, the output pulse width is defined as:

$$t_w \approx 0.33 \cdot R_T \cdot C_{ext}$$

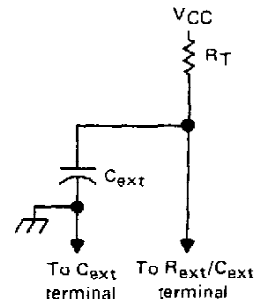
Where

R_T is in kilohms (internal or external timing resistance)

C_{ext} is in pF

t_w is in nanoseconds

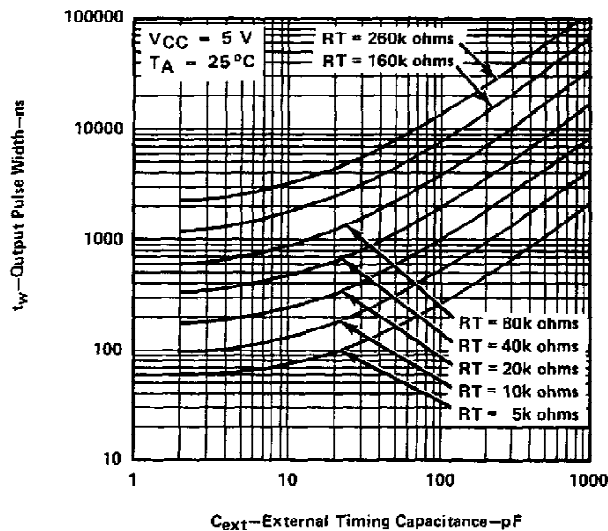
For maximum noise immunity, system ground should be applied to the C_{ext} node, even though the C_{ext} node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS422 and 'LS423, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.



TIMING COMPONENT CONNECTIONS
FIGURE 2

'LS422, 'LS423 TYPICAL OUTPUT PULSE WIDTH vs

EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3

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TYPICAL APPLICATION DATA FOR 'LS422, 'LS423 †

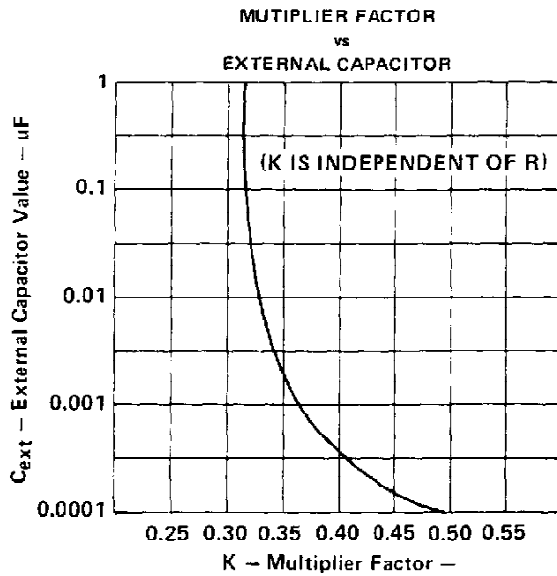


FIGURE 4

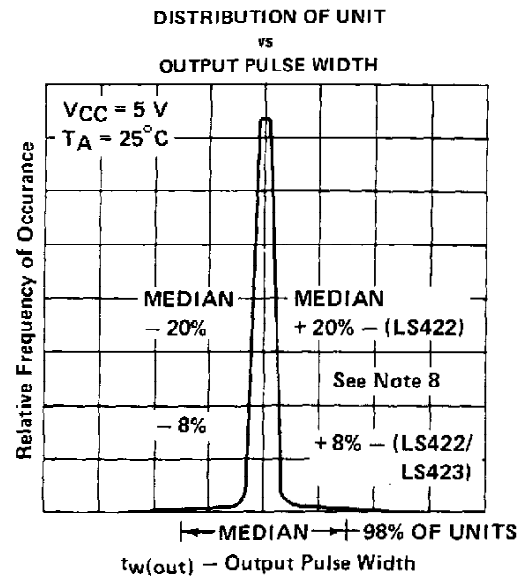


FIGURE 5

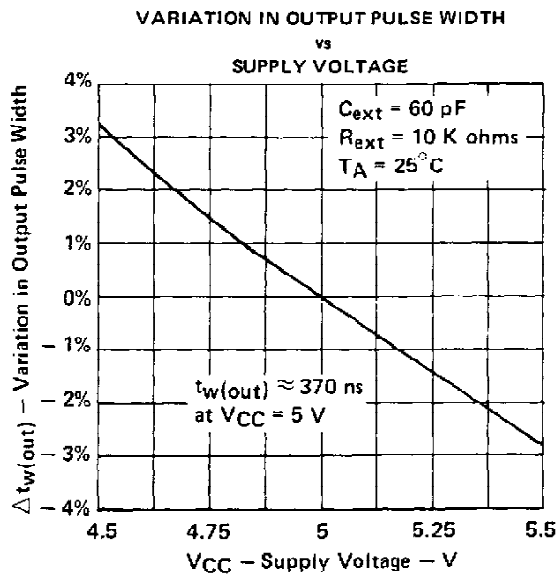


FIGURE 6

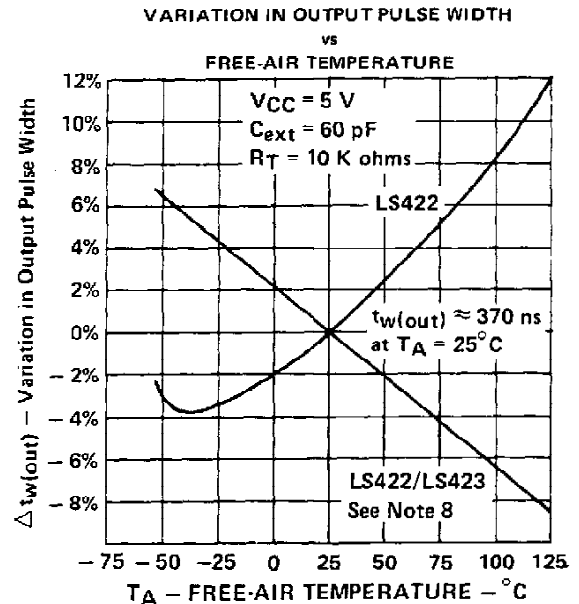


FIGURE 7

NOTE 8: For the LS422, the internal timing resistor, R_{int} , was used. For the LS422/423, an external timing resistor was used for R_T .
† Data for temperatures below $0^\circ C$ and above $70^\circ C$ and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS422 and SN54LS423 only.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS423D	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS423
SN74LS423D.A	Active	Production	SOIC (D) 16	40 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS423
SN74LS423N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS423N
SN74LS423N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS423N
SN74LS423NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS423
SN74LS423NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS423

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS423NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS423NSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS423D	D	SOIC	16	40	507	8	3940	4.32
SN74LS423D.A	D	SOIC	16	40	507	8	3940	4.32
SN74LS423N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS423N.A	N	PDIP	16	25	506	13.97	11230	4.32

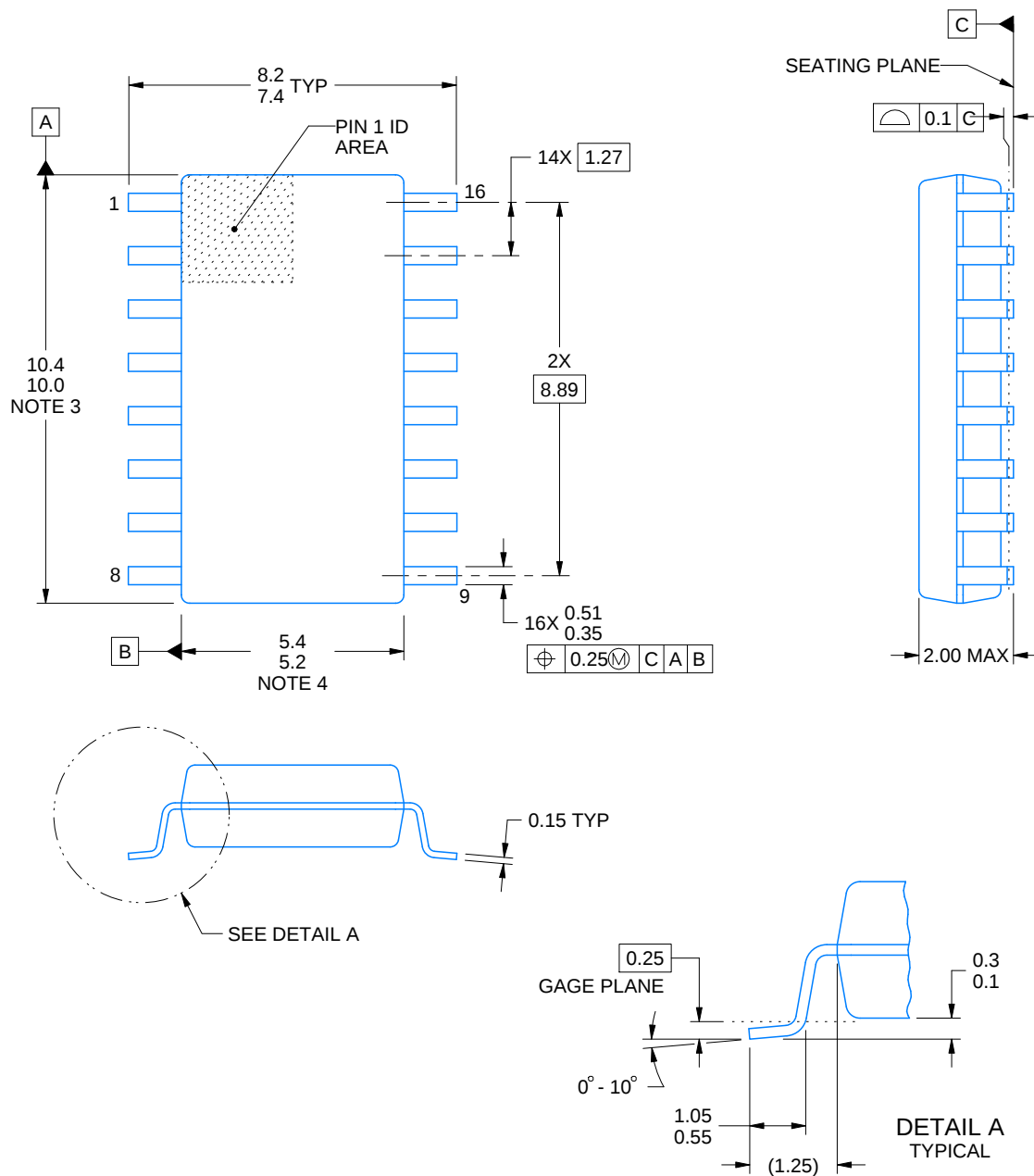


PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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