

SN54LS651 THRU SN54LS653 SN74LS651 THRU SN74LS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

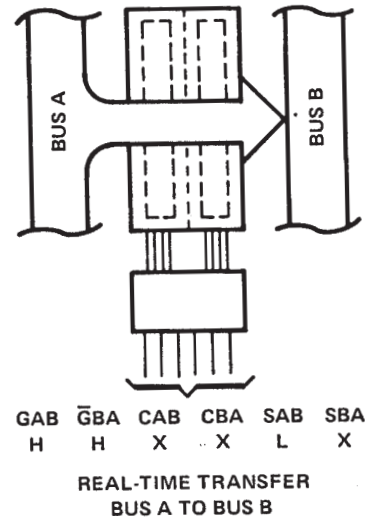
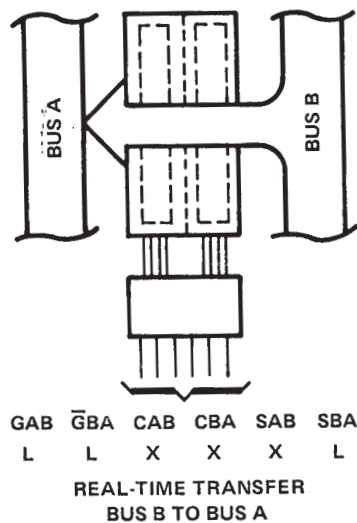
SDLS191A – JANUARY 1981 – REVISED DECEMBER 2000

- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Dependable Texas Instruments Quality and Reliability**

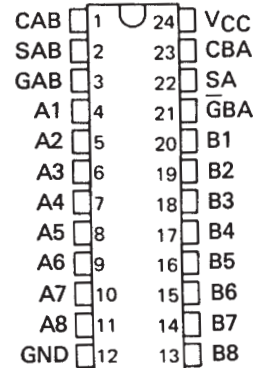
DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS651	3-State	3-State	Inverting
'LS652	3-State	3-State	True
'LS653	Open-collector	3-State	Inverting

description

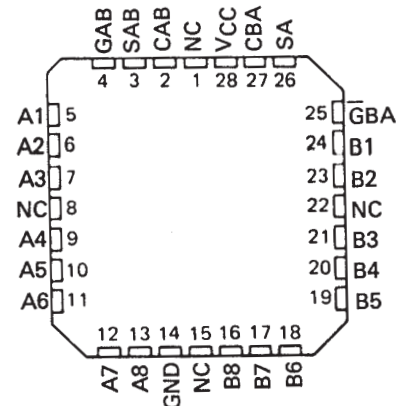
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, and 'LS653.



SN54LS' . . . JT PACKAGE
SN74LS' . . . DW OR NT PACKAGE
(TOP VIEW)



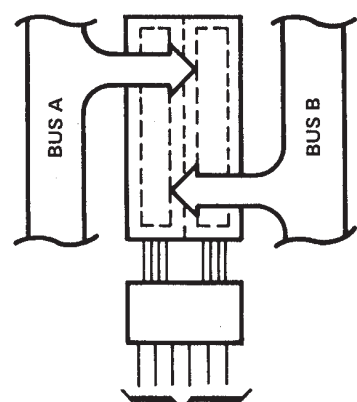
SN54LS' . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection

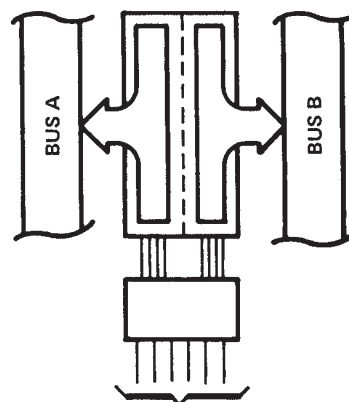
SN54LS651 THRU SN54LS653 SN74LS651 THRU SN74LS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

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GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER
STORED DATA
TO A AND/OR B

Data on the A or B data bus, or both, can be stored in the internal D flip-flop by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB or SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{GBA}}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

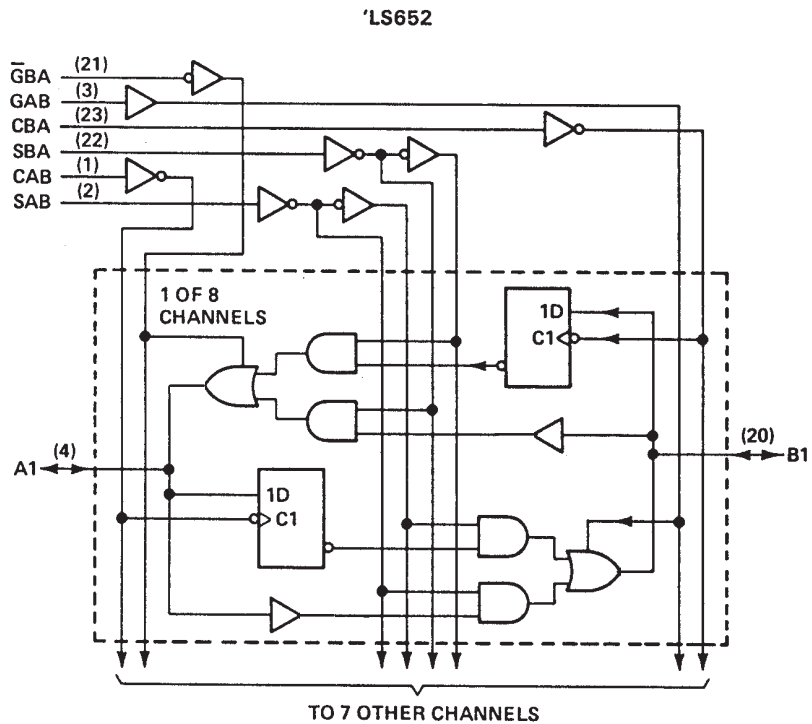
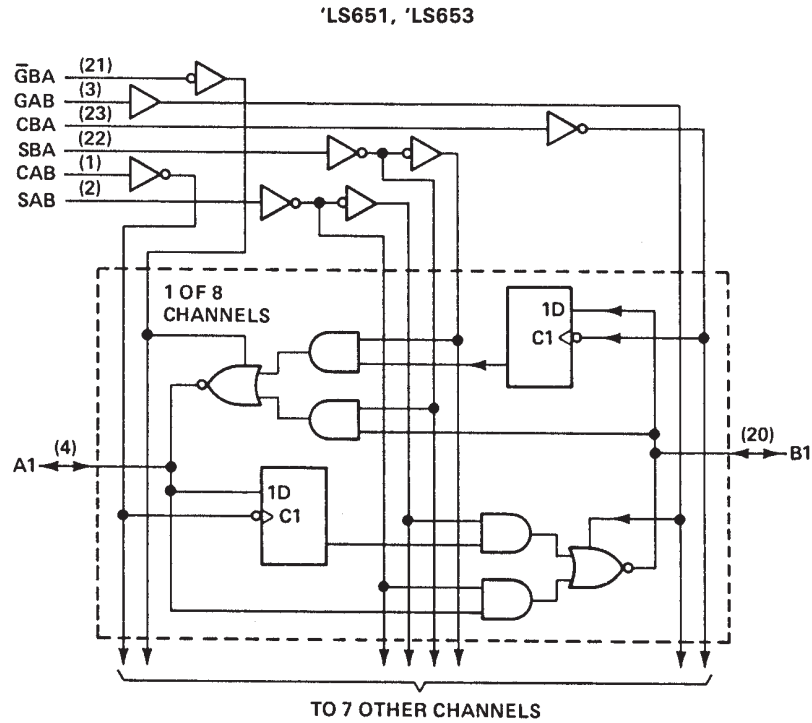
The SN54LS651 through SN54LS653 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS651 through SN74LS653 are characterized for operation from 0°C to 70°C .

FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{\text{GBA}}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651, 'LS653	'LS652, 'LS654
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{\text{B}}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{\text{B}}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{\text{A}}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{\text{A}}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{\text{A}}$ Data to B Bus and Stored $\overline{\text{B}}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and $\overline{\text{GBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

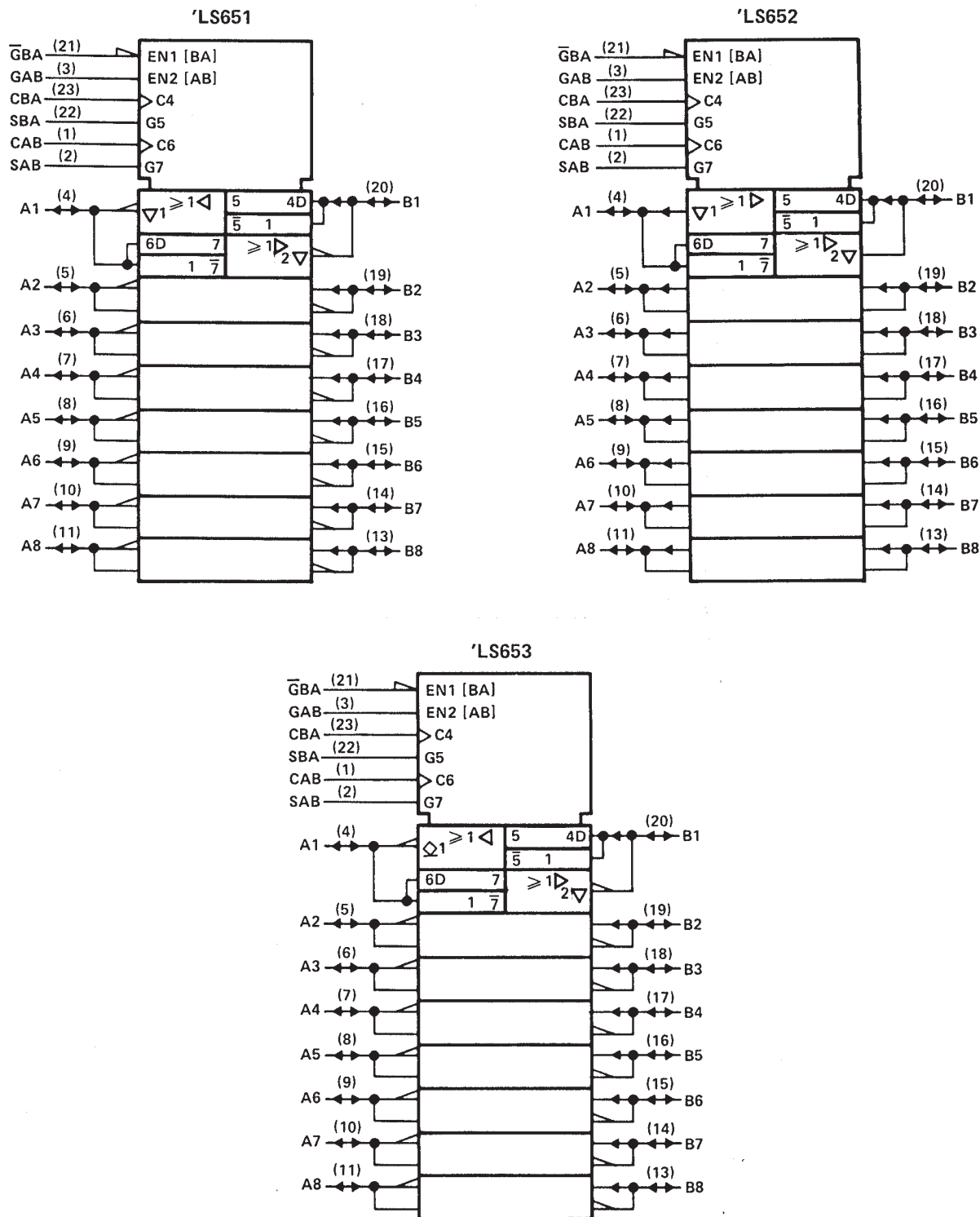


Pin numbers shown are for DW, JT or NT packages.

SN54LS651 THRU SN54LS653 SN74LS651 THRU SN74LS653 OCTAL BUS TRANSCEIVERS AND REGISTERS

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logic symbols†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, or NT packages.

SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS651, SN54LS652	– 55°C to 125°C
SN74LS651, SN74LS652	0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

			SN54LS651 SN54LS652			SN74LS651 SN74LS652			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.7			0.8	V		
I _{OH}	High-level output current				− 12			− 15	mA		
I _{OL}	Low-level output current				12			24	mA		
t _w	Pulse duration	CBA or CAB high	15			15			ns		
		CBA or CAB low	15			15					
		Data high or low	15			15					
t _{su}	Setup time before CAB ↑ or CBA ↑	A or B	15			15			ns		
t _h	Hold time after CAB ↑ or CBA ↑	A or B	0			0			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS651 SN54LS652		SN74LS651 SN74LS652		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
VIK		VCC = MIN, I1 = − 18 mA		− 1.5		− 1.5		V	
VOH		VCC = MIN, VIH = 2 V, VIL = MAX,		IOH = − 3 mA	2.4	3.4	2.4	3.4	V
				IOH = − 12 mA	2				
				IOH = − 15 mA			2		
VOL		VCC = MIN, VIH = 2 V, VIL = MAX,		IOL = 12 mA	0.25	0.4	0.25	0.4	V
				IOL = 24 mA			0.35 0.5		
II	Control inputs	VCC = MAX, VI = 7 V		0.1		0.1		mA	
	A or B ports	VCC = MAX, VI = 5.5 V		0.1		0.1			
IIH	Control inputs	VCC = MAX, VI = 2.7 V		20		20		μA	
	A or B ports¶			20		20			
IIL	Control inputs	VCC = MAX, VI = 0.4 V		− 0.4		− 0.4		mA	
	A or B ports¶			− 0.4		− 0.4			
IOS§		VCC = MAX, VO = 0 V		− 40	− 225	− 40	− 225	mA	
ICC	LS651	VCC = MAX		Outputs high	95	145	95	145	mA
				Outputs low	103	165	103	165	
				Outputs disabled	103	165	103	165	
	LS652			Outputs high	95	145	95	145	
				Outputs low	103	165	103	165	
				Outputs disabled	120	180	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

† For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS651			'LS652			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	Clock	Bus	R _L = 667 Ω, C _L = 45 pF, See Note 2		14	24		15	25	ns
t _{PHL}					23	35		24	36	ns
t _{PLH}	Bus	Bus			9	18		12	18	ns
t _{PHL}					20	30		13	20	ns
t _{PLH}	Select, with bus input high†	Bus			31	47		23	35	ns
t _{PHL}					22	33		21	32	ns
t _{PLH}	Select, with bus input low†	Bus			23	35		33	50	ns
t _{PHL}					19	30		15	23	ns
t _{PZH}	G̅BA	A Bus			29	44		30	45	ns
t _{PZL}					40	60		36	54	ns
t _{PZH}	GAB	B Bus		19	29		20	30	ns	
t _{PZL}				26	40		25	38	ns	
t _{PHZ}	G̅BA	A Bus	R _L = 667 Ω, C _L = 5 pF, See Note 2		25	38		25	38	ns
t _{PLZ}					19	30		19	30	ns
t _{PHZ}	GAB	B Bus			25	38		25	38	ns
t _{PLZ}					19	30		19	30	ns

t_{PLH} = propagation delay time, low-to-high-level output.

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

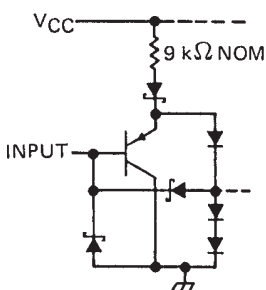
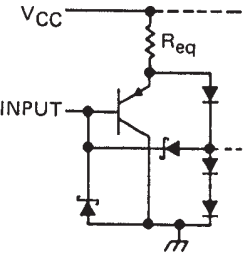
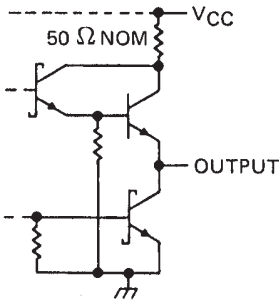
t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

EQUIVALENT OF GAB INPUTS	EQUIVALENT OF ALL OTHER INPUTS	TYPICAL OF ALL OUTPUTS
	 A and B: $R_{eq} = 15\text{ k}\Omega\text{ NOM}$ $\overline{G}BA$, CAB and CBA: $R_{eq} = 10\text{ k}\Omega\text{ NOM}$ SAB and SBA: $R_{eq} = 6\text{ k}\Omega\text{ NOM}$	

SN54LS653, SN74LS653

OCTAL BUS TRANSCEIVERS AND REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: All inputs and A I/O ports	7 V
B I/O ports	5.5 V
Operating free-air temperature range: SN54LS653	–55°C to 125°C
SN74LS653	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

			SN54LS653			SN74LS653			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.7			0.8	V		
V _{OH}	High-level output voltage	A ports			5.5			5.5	V		
I _{OH}	High-level output current	B ports			− 12			− 15	mA		
I _{OL}	Low-level output current				12			24	mA		
t _w	Pulse duration	CBA or CAB high	15			15			ns		
		CBA or CAB low	30			30					
		Data high or low	30			30					
t _{su}	Setup time before CAB ↑ or CBA ↑	A or B	15			15			ns		
t _h	Hold time after CAB ↑ or CBA ↑	A or B	0			0			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS653		SN74LS653		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IK}		V _{CC} = MIN, I _I = − 18 mA		− 1.5		− 1.5		V
V _{OH}	B ports	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = − 3 mA	2.4	3.4	2.4	3.4	V
			I _{OH} = − 12 mA	2				
			I _{OH} = − 15 mA			2		
I _{OH}	A ports	V _{CC} = MIN, V _{OH} = 5.5 V		0.1		0.1		mA
V _{OL}		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA			0.35 0.5		
I _I	Control inputs	V _{CC} = MAX, V _I = 7 V		0.1		0.1		mA
	A or B ports	V _{CC} = MAX, V _I = 5.5 V		0.1		0.1		
I _{IH}	Control inputs	V _{CC} = MAX, V _I = 2.7 V		20		20		μA
	A or B ports¶			20		20		
I _{IL}	Control inputs	V _{CC} = MAX, V _I = 0.4 V		− 0.4		− 0.4		mA
	A or B ports¶			− 0.4		− 0.4		
I _{OS} §	B ports	V _{CC} = MAX, V _O = 0 V		− 40	− 225	− 40	− 225	mA
I _{CC}	LS653	V _{CC} = MAX	Outputs high	95	145	95	145	mA
			Outputs low	103	165	103	165	
			Outputs disabled	103	165	103	165	
	LS654		Outputs high	95	145	95	145	
			Outputs low	105	170	105	170	
			Outputs disabled	120	180	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.



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SN54LS653, SN74LS653

OCTAL BUS TRANSCEIVERS AND REGISTERS

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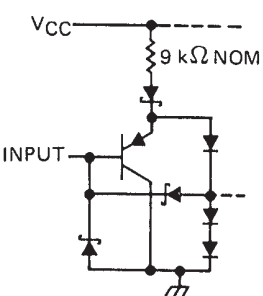
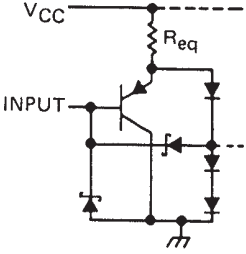
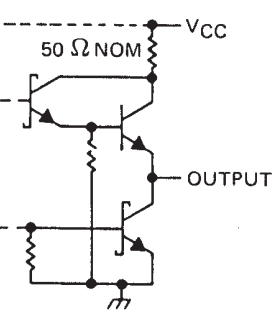
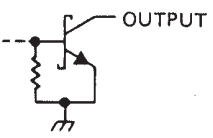
switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	CBA	A Bus	R _L = 667 Ω, C _L = 45 pF, See Note 2		25	38	ns
t _{PHL}					26	39	
t _{PLH}	CAB	B Bus			15	23	ns
t _{PHL}					24	36	
t _{PLH}	A Bus	B Bus			10	18	ns
t _{PHL}					20	30	
t _{PLH}	B Bus	A Bus			21	32	ns
t _{PHL}					16	24	
t _{PLH}	SBA [†] (with B high)	A Bus			38	57	ns
t _{PHL}					26	39	
t _{PLH}	SBA [†] (with B low)	A Bus			34	51	ns
t _{PHL}					23	35	
t _{PLH}	SAB [†] (with A high)	B Bus			32	48	ns
t _{PHL}					22	33	
t _{PLH}	SAB [†] (with A low)	B Bus			24	36	ns
t _{PHL}					20	30	
t _{PLH}	GBA	A Bus			23	35	ns
t _{PHL}					37	55	
t _{PZH}	GAB	B Bus	R _L = 667 Ω, C _L = 5 pF, See Note 2		19	29	ns
t _{PZL}					25	38	
t _{PHZ}	GAB	B Bus			26	39	ns
t _{PLZ}					19	29	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs

EQUIVALENT OF GAB INPUTS	EQUIVALENT OF ALL OTHER INPUTS	TYPICAL OF B OUTPUTS	TYPICAL OF A OUTPUTS
	 A and B: $R_{eq} = 15\text{ k}\Omega\text{ NOM}$ $\bar{G}BA$, CAB and CBA: $R_{eq} = 10\text{ k}\Omega\text{ NOM}$ SAB and SBA: $R_{eq} = 6\text{ k}\Omega\text{ NOM}$		

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LS652DW	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS652
SN74LS652DW.A	Active	Production	SOIC (DW) 24	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS652

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

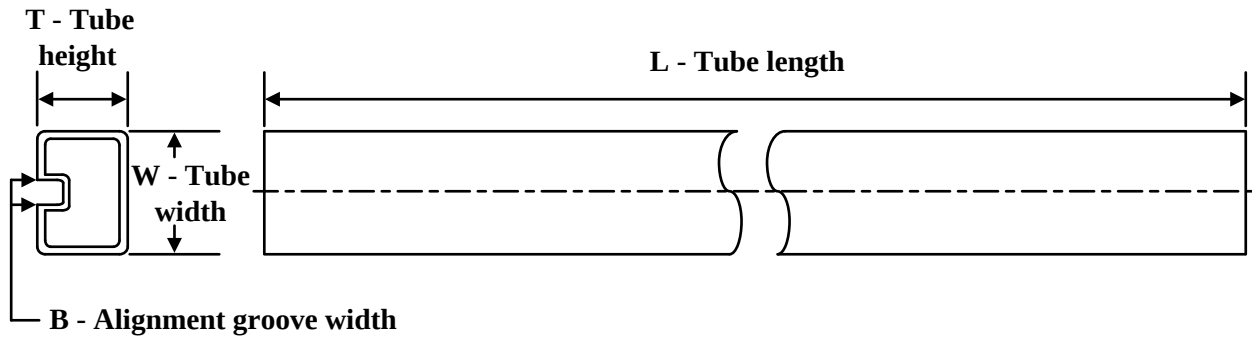
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LS652DW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LS652DW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

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