

# SN74LV126A Quadruple Bus Buffer Gates With 3-State Outputs

## 1 Features

- 2V to 5.5V  $V_{CC}$  operation
- Maximum  $t_{pd}$  of 6.5ns at 5V
- Typical  $V_{OLP}$  (output ground bounce)  $<0.8V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $>2.3V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- $I_{off}$  supports live insertion, partial power down mode, and back drive protection
- Support mixed-mode voltage operation on all ports
- Latch-up performance exceeds 250mA per JESD 17

## 2 Applications

- Servers
- Network switch
- Electronic point of sales
- TV
- Set-top-box

## 3 Description

The SN74LV126A quadruple bus buffer gates are designed for 2V to 5.5V  $V_{CC}$  operation.

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The SN74LV126A devices feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

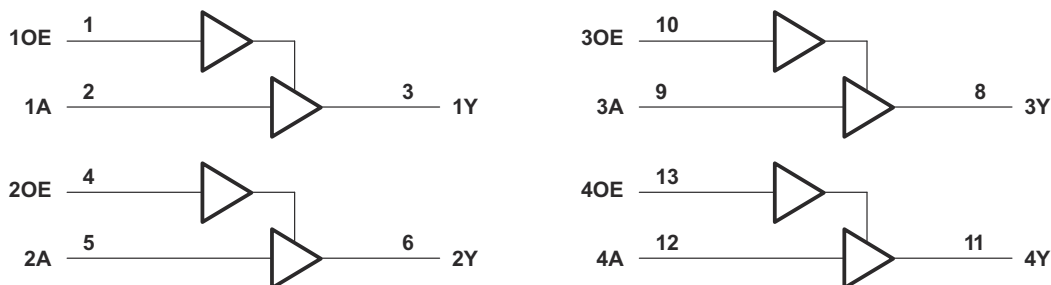
To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN74LV126A	D (SOIC, 14)	8.65mm × 6mm
	NS (SOP, 14)	10.2mm × 7.8mm
	DB (SSOP, 14)	6.2mm × 7.8mm
	PW (TSSOP, 14)	5mm × 6.4mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



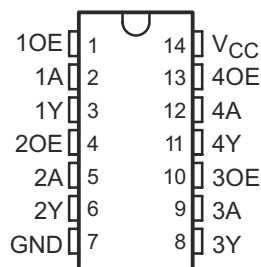
Logic Diagram (Positive Logic)



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## 4 Pin Configuration and Functions



**Figure 4-1. SN74LV126A: D, DB, DGV, NS, or PW Package, 14-Pin SOIC, SSOP, TVSOP, SOP, or TSSOP (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1OE	1	I	Channel 1, Output Enable
1A	2	I	Channel 1, Input A
1Y	3	O	Channel 1, Output Y
2OE	4	I	Channel 2, Output Enable
2A	5	I	Channel 2, Input A
2Y	6	O	Channel 2, Output Y
GND	7	—	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3OE	10	I	Channel 3, Output Enable
4Y	11	O	Channel 4, Output Y
4A	12	I	Channel 4, Input A
4OE	13	I	Channel 4, Output Enable
V <sub>CC</sub>	14	—	Positive Supply

(1) I = input, O = output, P = power, G = ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	–0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	–0.5	7	V
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	7	V
V <sub>O</sub>	Output voltage <sup>(2)</sup> <sup>(3)</sup>	–0.5	V <sub>CC</sub> + 0.5V	V
I <sub>IK</sub>	Input clamp current, V <sub>I</sub> < 0		–20	mA
I <sub>OK</sub>	Output clamp current, V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current, V <sub>O</sub> = 0 to V <sub>CC</sub>		±35	mA
	Continuous current through V <sub>CC</sub> or GND		±70	mA
T <sub>stg</sub>	Storage temperature	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5V maximum.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

see <sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2V	1.5		V
		V <sub>CC</sub> = 2.3 to 2.7V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 to 3.6V	V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 to 5.5V	V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2V		0.5	V
		V <sub>CC</sub> = 2.3 to 2.7V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 to 3.6V		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 to 5.5V		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2V		–50	μA
		V <sub>CC</sub> = 2.3 to 2.7V		–2	mA
		V <sub>CC</sub> = 3 to 3.6V		–8	
		V <sub>CC</sub> = 4.5 to 5.5V		–16	

### 5.3 Recommended Operating Conditions (continued)

see (1)

		MIN	MAX	UNIT
$I_{OL}$	Low-level output current	$V_{CC} = 2V$	50	$\mu A$
		$V_{CC} = 2.3$ to $2.7V$	2	mA
		$V_{CC} = 3$ to $3.6V$	8	
		$V_{CC} = 4.5$ to $5.5V$	16	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ to $2.7V$	200	ns/V
		$V_{CC} = 3$ to $3.6V$	100	
		$V_{CC} = 4.5$ to $5.5V$	20	
$T_A$	Operating free-air temperature	-40	125	$^{\circ}C$

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		D	DB	DGV	NS	PW	UNIT
		14 PINS					
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(2)</sup>	92.7	105.0	127.6	89.6	119.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54.1	57.5	50.7	47.2	48.6	
R <sub>θJB</sub>	Junction-to-board thermal resistance	47.0	52.3	60.5	48.4	61.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.9	19.1	6.1	14.0	5.7	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.7	51.8	59.8	48.1	61.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	MIN	TYP	MAX	UNIT
$V_{OH}$	$I_{OH} = -50\mu A$	2 to 5.5V	$V_{CC} - 0.1$			V
	$I_{OH} = -2mA$	2.3V	2			
	$I_{OH} = -8mA$	3V	2.48			
	$I_{OH} = -16mA$	4.5V	3.8			
$V_{OL}$	$I_{OL} = 50\mu A$	2 to 5.5V			0.1	V
	$I_{OL} = 2mA$	2.3V			0.4	
	$I_{OL} = 8mA$	3V			0.44	
	$I_{OL} = 16mA$	4.5V			0.55	
$I_I$	$V_I = 5.5V$ or GND	0 to 5.5V			$\pm 1$	$\mu A$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.5V			$\pm 5$	$\mu A$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5V			20	$\mu A$
$I_{off}$	$V_I$ or $V_O = 0$ to 5.5V	0V			$\pm 5$	$\mu A$
$C_i$	$V_I = V_{CC}$ or GND	3.3V		1.6		pF

## 5.6 Switching Characteristics, $V_{CC} = 2.5V \pm 0.2V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A	Y	$C_L = 15pF$		7.1	13	1	15.5	ns
$t_{en}$	OE				7.4	13	1	15.5	
$t_{dis}$	OE				5.7	14.7	1	17	
$t_{pd}$	A	Y	$C_L = 50pF$		9.2	16.5	1	18.5	ns
$t_{en}$	OE				9.5	16.5	1	18.5	
$t_{dis}$	OE				8.1	18.2	15	20.5	
$t_{sk(o)}$						2		2	

## 5.7 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A	Y	$C_L = 15pF$		5	8	1	9.5	ns
$t_{en}$	OE				5.1	8	1	9.5	
$t_{dis}$	OE				4.4	9.7	1	11.5	
$t_{pd}$	A	Y	$C_L = 50pF$		6.4	11.5	1	13	ns
$t_{en}$	OE				6.6	11.5	1	13	
$t_{dis}$	OE				6.1	13.2	1	15	
$t_{sk(o)}$						1.5		1.5	

## 5.8 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ C$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{pd}$	A	Y	$C_L = 15pF$		3.5	5.5	1	6.5	ns
$t_{en}$	OE				3.6	5.1	1	6	
$t_{dis}$	OE				3.3	6.8	1	8	
$t_{pd}$	A	Y	$C_L = 50pF$		4.6	7.5	1	8.5	ns
$t_{en}$	OE				4.6	7.1	1	8	
$t_{dis}$	OE				4.3	8.8	1	10	
$t_{sk(o)}$						1		1	

## 5.9 Noise Characteristics

$V_{CC} = 3.3V$ ,  $C_L = 50pF$ ,  $T_A = 25^\circ C$  (see (1))

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.2	-0.8	
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.1		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.97	

(1) Characteristics are for surface-mount packages only.

## 5.10 Operating Characteristics

$T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enable; $C_L = 50pF$ , $f = 10MHz$	3.3V	14.4	pF
			5V	15.9	

## 5.11 Typical Characteristics

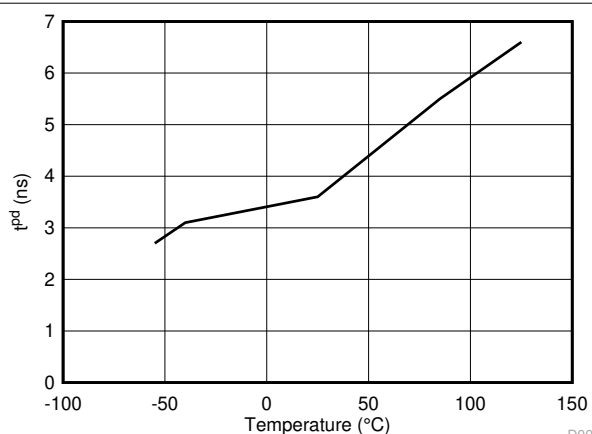


Figure 5-1. SN74LV126A  $t_{PD}$  vs Temperature at 5V

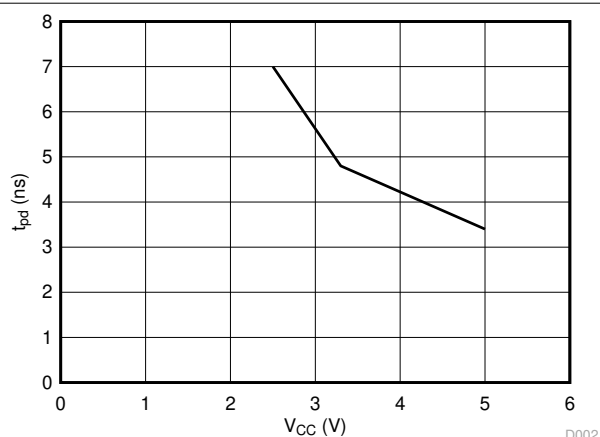
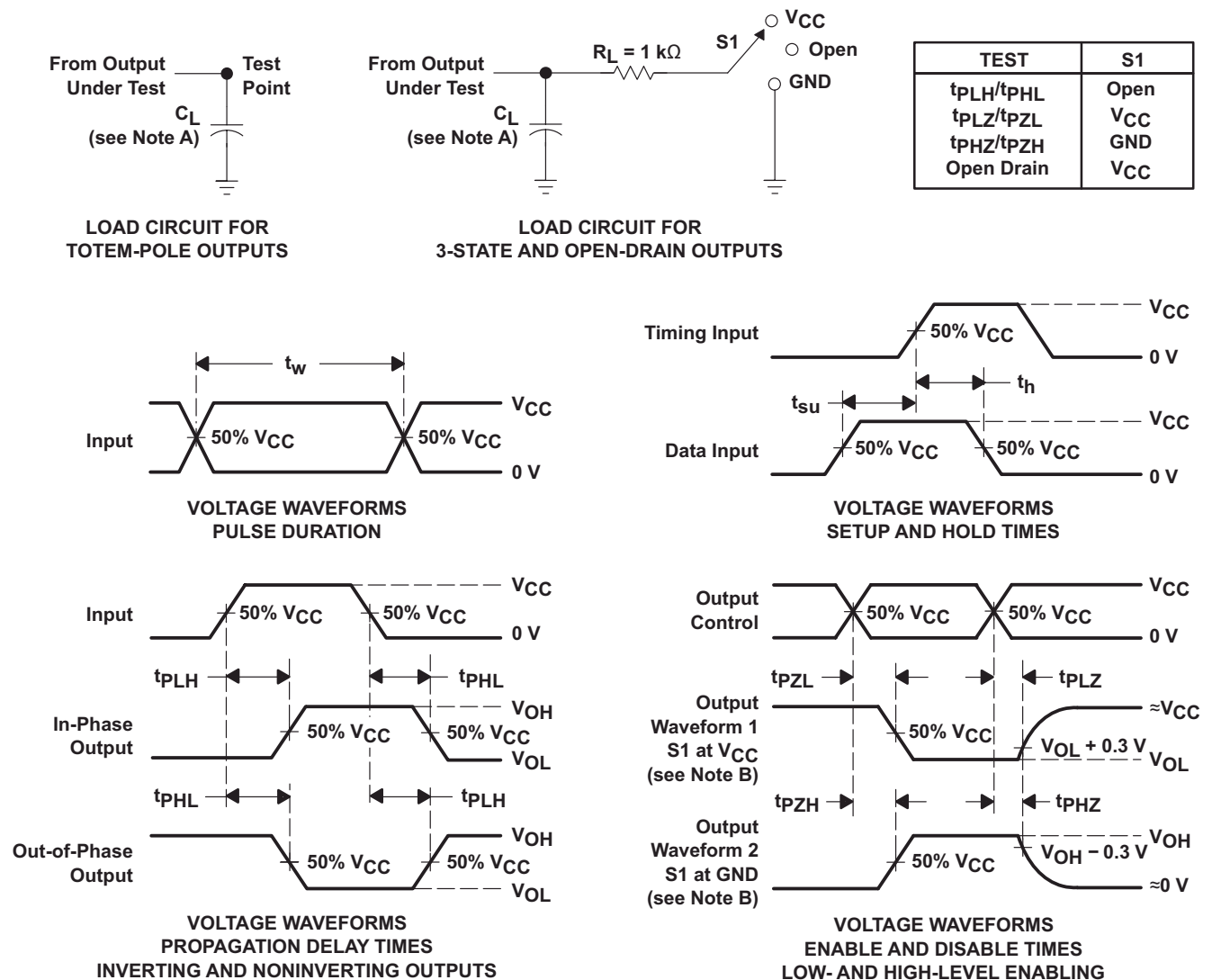


Figure 5-2. SN74LV126A  $t_{PD}$  vs  $V_{CC}$  at 25°C

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

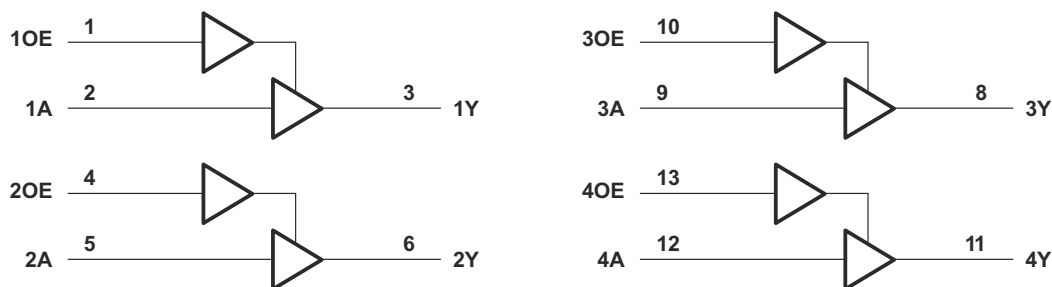
**Figure 6-1. Load Circuit and Voltage Waveforms**

## 7 Detailed Description

### 7.1 Overview

The SN74LV126A devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low. When OE is high, the respective gate passes the data from the A input to its Y output. To put the device in the high-impedance state during power up or power down, tie OE to GND through a pulldown resistor; the current-sourcing capability of the driver determines the minimum value of the resistor.

### 7.2 Functional Block Diagram



A. Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, and W packages.

**Figure 7-1. Logic Diagram (Positive Logic)**

### 7.3 Feature Description

- Wide operating voltage range, operates from 2 to 5.5V
- Allows down voltage translation, inputs accept voltages to 5.5V
- Ioff supports live insertion, partial power down mode, and back drive protection

### 7.4 Device Functional Modes

**Table 7-1. Function Table  
(Each Buffer)**

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z



## 8 Application and Implementation

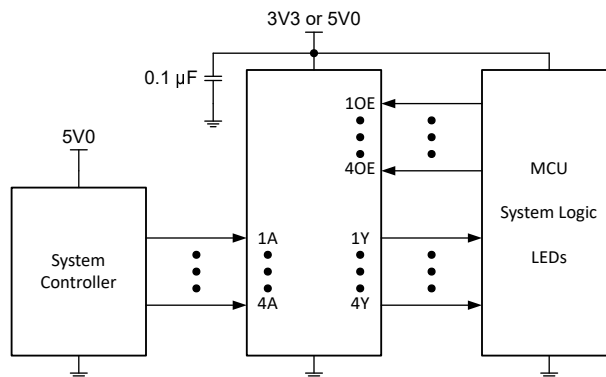
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74LV126A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs are 5.5V tolerant at any valid  $V_{CC}$  making this device an excellent choice for translating down to  $V_{CC}$ .

### 8.2 Typical Application



**Figure 8-1. Typical Application Schematic**

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended input conditions
  - Rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#).
  - Specified High and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#).
- Recommend output conditions
  - Load currents should not exceed 35mA per output and 70mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

## 8.2.3 Application Curve

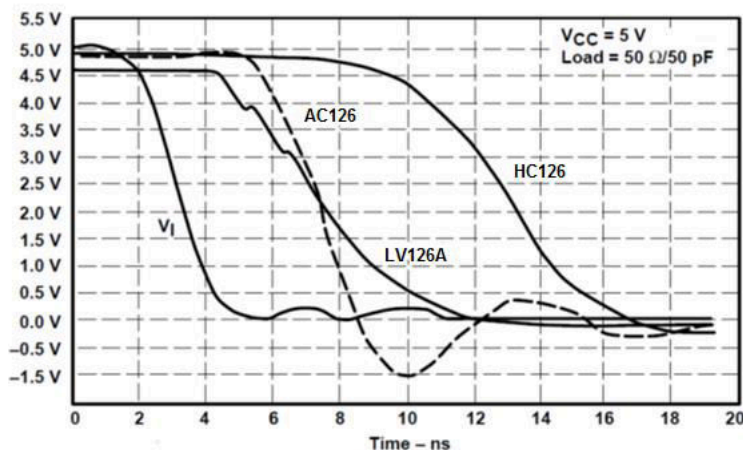


Figure 8-2. Switching Characteristics Comparison

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in [Recommended Operating Conditions](#). Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended and if there are multiple  $V_{CC}$  terminals then .01 or .022  $\mu\text{F}$  is recommended for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever makes more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

### 8.4.2 Layout Example

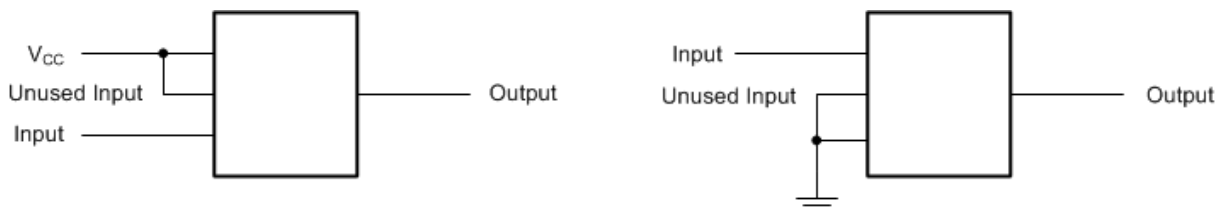


Figure 8-3. Layout Recommendation

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February 2015) to Revision J (April 2024)	Page
• Removed the <i>SN54LV126A</i> device from the data sheet.....	1
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed the 125 function table with the correct 126 function table.....	8

Changes from Revision H (April 2005) to Revision I (February 2015)	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV126A .....	3

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LV126AD</a>	Obsolete	Production	SOIC (D)   14	-	-	Call TI	Call TI	-40 to 125	LV126A
<a href="#">SN74LV126ADBR</a>	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126ADBR.A	Active	Production	SSOP (DB)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
<a href="#">SN74LV126ADGVR</a>	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126ADGVR.A	Active	Production	TVSOP (DGV)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
<a href="#">SN74LV126ADR</a>	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126ADR.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
<a href="#">SN74LV126ANSR</a>	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV126A
SN74LV126ANSR.A	Active	Production	SOP (NS)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV126A
<a href="#">SN74LV126APW</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	LV126A
<a href="#">SN74LV126APWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126APWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126APWRG4	Active	Production	TSSOP (PW)   14	2000   null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126APWRG4	Active	Production	TSSOP (PW)   14	2000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126APWRG4.A	Active	Production	TSSOP (PW)   14	2000   null	No	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
SN74LV126APWRG4.A	Active	Production	TSSOP (PW)   14	2000   null	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV126A
<a href="#">SN74LV126APWT</a>	Obsolete	Production	TSSOP (PW)   14	-	-	Call TI	Call TI	-40 to 125	LV126A

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV126ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV126ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV126ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV126ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LV126APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV126ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LV126ADGVR	TVSOP	DGV	14	2000	353.0	353.0	32.0
SN74LV126ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LV126ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LV126APWR	TSSOP	PW	14	2000	353.0	353.0	32.0

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194





4220762/A 05/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

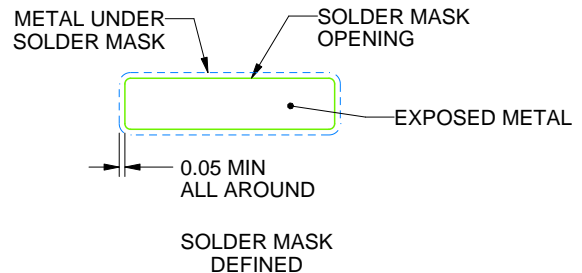
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**PW0014A**

## PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

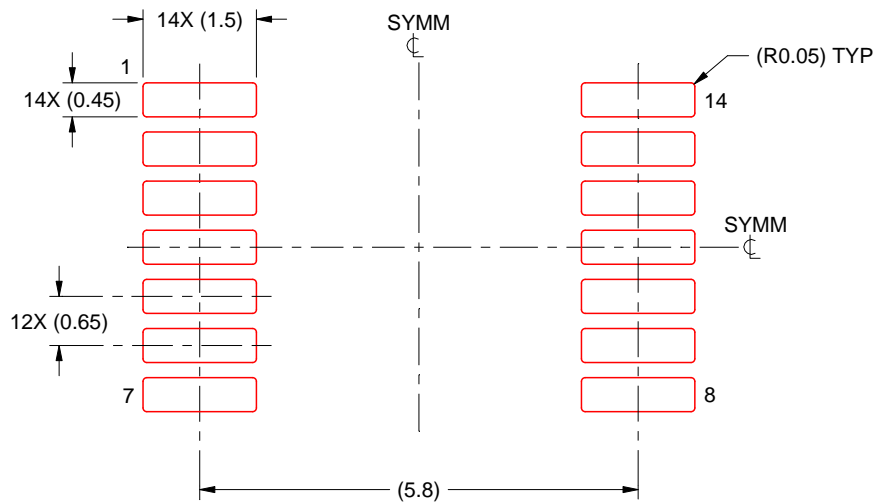
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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