# SN74LV1T32 Single Power Supply 2-Input Positive OR Gate CMOS Logic Level Shifter

## 1 Features

- Single-supply voltage translator at 5.0V, 3.3V, 2.5V, and 1.8V $V_{CC}$
- Operating range of 1.8V to 5.5V
- Up translation:
  - 1.2V(1) to 1.8V at 1.8V $V_{CC}$
  - 1.5V(1) to 2.5V at 2.5V $V_{CC}$
  - 1.8V(1) to 3.3V at 3.3V $V_{CC}$
  - 3.3V to 5.0V at 5.0V $V_{CC}$
- Down translation:
  - 3.3V to 1.8V at 1.8V $V_{CC}$
  - 3.3V to 2.5V at 2.5V $V_{CC}$
  - 5.0V to 3.3V at 3.3V $V_{CC}$
- Logic output is referenced to $V_{CC}$
- Output drive:
  - 8mA output drive at 5V
  - 7mA output drive at 3.3V
  - 3mA output drive at 1.8V
- Characterized up to 50MHz at 3.3V $V_{CC}$
- 5V Tolerance on input pins
- –40°C to 125°C operating temperature range
- Pb-free packages available: SC-70 (DCK)
  - 2 × 2.1 × 0.65mm (height 1.1mm)
- Latch-up performance exceeds 250mA per JESD 17
- Supports standard logic pinouts
- CMOS output B compatible with AUP1G and LVC1G families [1]

## 2 Applications

- Telecom
- Portable applications
- Servers
- PC and notebooks

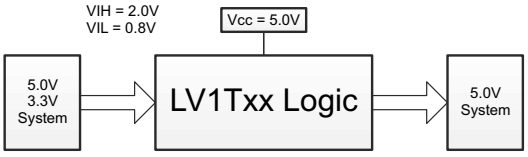
## 3 Description

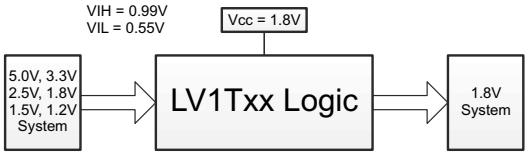
The SN74LV1T32 is a single 2-input OR gate with reduced input thresholds to support voltage translation applications.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LV1T32 | DBV (SOT-23, 5) | 2.9mm × 2.8mm | 2.9mm x 1.6mm |
| | DCK (SC70, 5) | 2.0mm × 2.1mm | 2.0mm × 1.25mm |

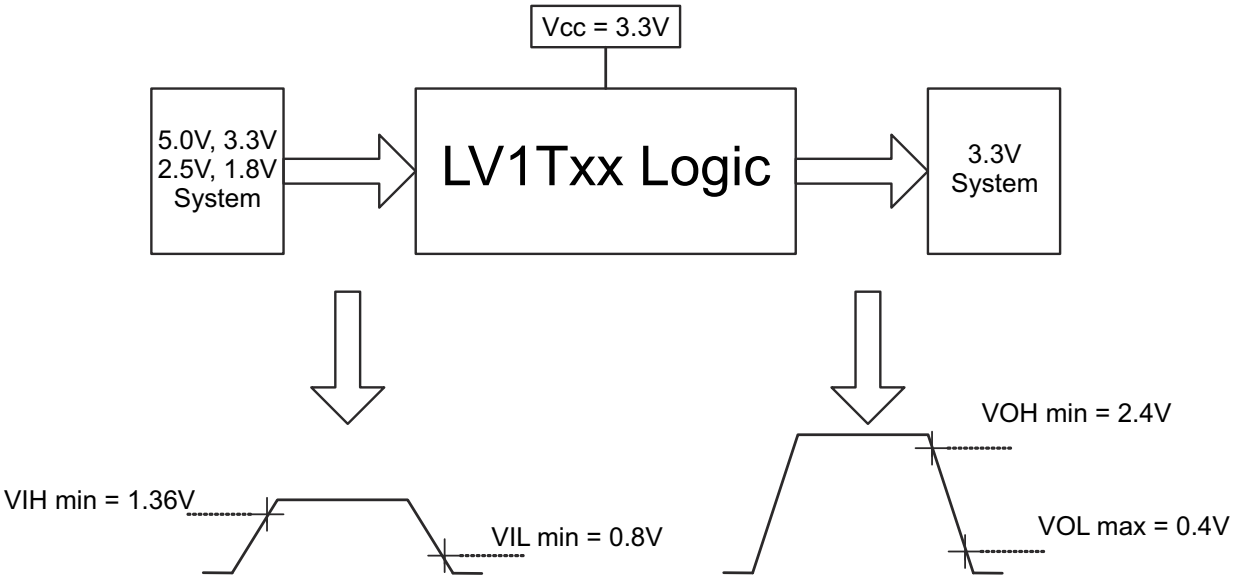
(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length x width) is a nominal value and does not include pins.




[1] Refer to the $V_{IH}/V_{IL}$ and output drive for lower $V_{CC}$ condition.

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**Switching Thresholds for 1.8-V to 3.3-V Translation**


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## 4 Related Products

| DEVICE | PACKAGE | DESCRIPTION |
|---|---|---|
| SN74LV1T00 | DCK, DBV | 2-Input Positive-NAND Gate |
| SN74LV1T02 | DCK, DBV | 2-Input Positive-NOR Gate |
| SN74LV1T04 | DCK, DBV | Inverter Gate |
| SN74LV1T08 | DCK, DBV | 2-Input Positive-AND Gate |
| SN74LV1T17 | DCK, DBV | Single Schmitt-Trigger Buffer Gate |
| SN74LV1T14 | DCK, DBV | Single Schmitt-Trigger Inverter Gate |
| SN74LV1T32 | DCK, DBV | 2-Input Positive-OR Gate |
| SN74LV1T34 | DCK, DBV | Single Buffer Gate |
| SN74LV1T86 | DCK, DBV | Single 2-Input Exclusive-Or Gate |
| SN74LV1T125 | DCK, DBV | Single Buffer Gate with 3-state Output |
| SN74LV1T126 | DCK, DBV | Single Buffer Gate with 3-state Output |
| SN74LV4T125 | RGY, PW | Quadruple Bus Buffer Gate With 3-State Outputs |


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## 5 Pin Configuration and Functions

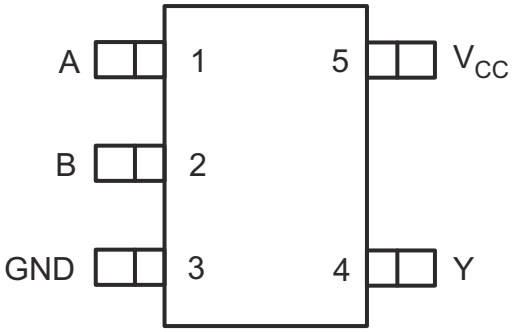



**Figure 5-1. DCK or DBV Package, 5-Pin SC70 or SOT-23 (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A | 1 | I | Input A |
| B | 2 | I | Input B |
| GND | 3 | G | Ground |
| Y | 4 | O | Output Y |
| $V_{CC}$ | 5 | P | Positive supply |

(1) I = input, O = output

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7.0 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7.0 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 4.6 | V |
| | Voltage range applied to any output in the high or low state(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.6 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.8 V | | –3 | mA |
| | | $V_{CC}$ = 2.5 V | | –5 | |
| | | $V_{CC}$ = 3.3 V | | –7 | |
| | | $V_{CC}$ = 5.0 V | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.8 V | | 3 | mA |
| | | $V_{CC}$ = 2.5 V | | 5 | |
| | | $V_{CC}$ = 3.3 V | | 7 | |
| | | $V_{CC}$ = 5.0 V | | 8 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.8 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V or 2.5 V | | 20 | |
| | | $V_{CC}$ = 5.0 V | | 20 | |
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.


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## 6.4 Thermal Information

| THERMAL METRIC[1] | | DBV | DCK | UNIT |
|---|---|---|---|---|
| | | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 289.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $V_{IH}$ | High-level input voltage | | 1.65 V to 1.8 V | 0.94 | | | 1.0 | | V |
| | | | 2.0 V | 0.99 | | | 1.03 | | |
| | | | 2.25 V to 2.5 V | 1.135 | | | 1.18 | | |
| | | | 2.75 V | 1.21 | | | 1.23 | | |
| | | | 3 V to 3.3 V | 1.35 | | | 1.37 | | |
| | | | 3.6 V | 1.47 | | | 1.48 | | |
| | | | 4.5 V to 5.0 V | 2.02 | | | 2.03 | | |
| | | | 5.5 V | 2.1 | | | 2.11 | | |
| $V_{IL}$ | Low-level input voltage | | 1.65 V to 2.0 V | | | 0.58 | | 0.55 | V |
| | | | 2.25 V to 2.75 V | | | 0.75 | | 0.71 | |
| | | | 3 V to 3.6 V | | | 0.8 | | 0.65 | |
| | | | 4.5 V to 5.5 V | | | 0.8 | | 0.8 | |
| $V_{OH}$ | | $I_{OH}$ = –20 µA | 1.65 V to 5.5 V | $V_{CC}$ – 0.1 | | | $V_{CC}$ – 0.1 | | V |
| | | $I_{OH}$ = –2.0 mA | 1.65 V | 1.28 | | | 1.21 | | V |
| | | | 1.8 V | 1.5 | | | 1.45 | | |
| | | $I_{OH}$ = –3 mA | 2.3 V | 2.0 | | | 1.93 | | V |
| | | $I_{OH}$ = –3 mA | 2.5 V | 2.25 | | | 2.15 | | V |
| | | $I_{OH}$ = –3.0 mA | 3.0 V | 2.78 | | | 2.7 | | V |
| | | $I_{OH}$ = –5.5 mA | | 2.6 | | | 2.49 | | |
| | | $I_{OH}$ = –5.5 mA | 3.3 V | 2.9 | | | 2.8 | | |
| | | $I_{OH}$ = –4 mA | 4.5 V | 4.2 | | | 4.1 | | V |
| | | $I_{OH}$ = –8 mA | | 4.1 | | | 3.95 | | |
| | | $I_{OH}$ = –8 mA | 5.0 V | 4.6 | | | 4.5 | | |
| $V_{OL}$ | | $I_{OL}$ = 20 µA | 1.65 V to 5.5 V | | | 0.1 | | 0.1 | V |
| | | $I_{OL}$ = 2.0 mA | 1.65 V | | | 0.2 | | 0.25 | |
| | | $I_{OH}$ = 3 mA | 2.3 V | | | 0.15 | | 0.2 | |
| | | $I_{OL}$ = 3 mA | 3.0 V | | | 0.1 | | 0.15 | |
| | | $I_{OL}$ = 5.5 mA | | | | 0.2 | | 0.252 | |
| | | $I_{OL}$ = 4 mA | 4.5 V | | | 0.15 | | 0.2 | |
| | | $I_{OL}$ = 8 mA | | | | 0.3 | | 0.35 | |
| $I_I$ | A input | $V_I$ = 0 V or $V_{CC}$ | 0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V | | | 0.1 | | ±1 | µA |
| $I_{CC}$ | | $V_I$ = 0 V or $V_{CC}$, $I_O$ = 0; open on loading | 5.0 V | | | 1 | | 10 | µA |
| | | | 3.3 V | | | 1 | | 10 | |
| | | | 2.5 V | | | 1 | | 10 | |
| | | | 1.8 V | | | 1 | | 10 | |
| $\Delta I_{CC}$ | | One input at 0.3 V or 3.4 V, Other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 5.5 V | | | 1.35 | | 1.5 | mA |
| | | One input at 0.3 V or 1.1 V Other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 1.8 V | | | 10 | | 10 | µA |

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## 6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | $T_A$ = –40°C to 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 2 | 10 | 2 | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 3.3 V | | 2.5 | | 2.5 | | pF |

## 6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | FREQUENCY (TYP) | $V_{CC}$ | $C_L$ | $T_A$ = 25°C | | | $T_A$ = –65°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{pd}$ | Any In | Y | DC to 50 MHz | 5.0 V | 15 pF | | 4 | 5 | | 4 | 5 | ns |
| | | | | | 30 pF | | 5.5 | 7.0 | | 5.5 | 7.0 | |
| | | | | 3.3 V | 15 pF | | 4.8 | 5 | | 5 | 5.5 | ns |
| | | | | | 30 pF | | 5 | 5.5 | | 5.5 | 6.5 | |
| | | | DC to 25 MHz | 2.5 V | 15 pF | | 6 | 6.5 | | 7 | 7.5 | ns |
| | | | | | 30 pF | | 6.5 | 7.5 | | 7.5 | 8.5 | |
| | | | DC to 15 MHz | 1.8 V | 15 pF | | 10.5 | 11 | | 11 | 12 | ns |
| | | | | | 30 pF | | 12 | 13 | | 12 | 14 | |

## 6.7 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | f = 1 MHz and 10 MHz | 1.8 V ± 0.15 V | 14 | pF |
| | | | 2.5 V ± 0.2 V | 14 | |
| | | | 3.3 V ± 0.3 V | 14 | |
| | | | 5.5 V ± 0.5 V | 14 | |


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## 6.8 Typical Characteristics

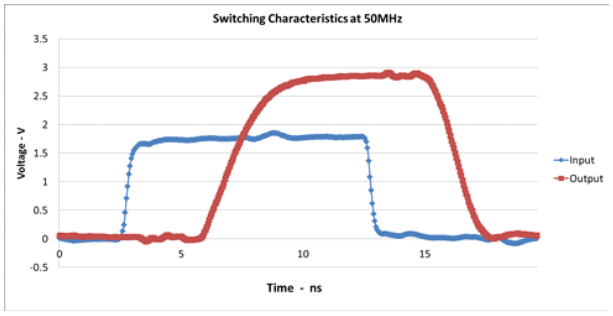



**Figure 6-1. Excellent Signal Integrity (1.8 V to 3.3 V at 3.3-V $V_{CC}$)**

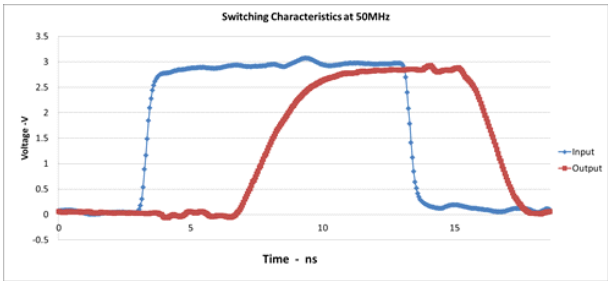



**Figure 6-2. Excellent Signal Integrity (3.3 V to 3.3 V at 3.3-V $V_{CC}$)**

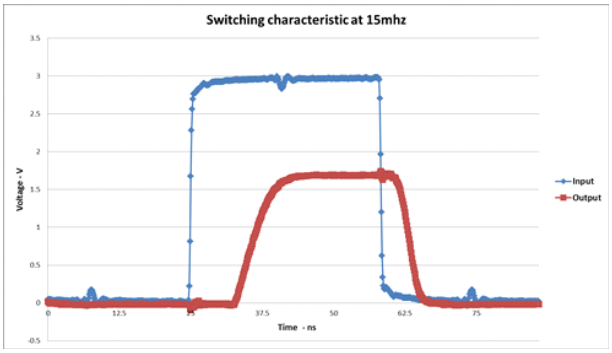
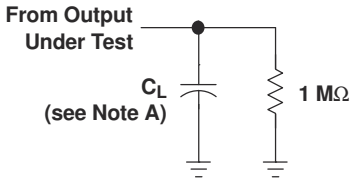



**Figure 6-3. Excellent Signal Integrity (3.3 V to 1.8 V at 1.8-V $V_{CC}$)**

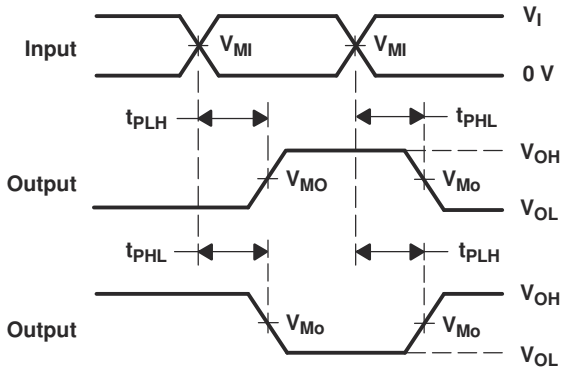
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# 7 Parameter Measurement Information




LOAD CIRCUIT

| | $V_{CC}$ = 2.5 V ± 0.2 V | $V_{CC}$ = 3.3 V ± 0.3 V |
|---|---|---|
| $C_L$ | 5, 10, 15, 30 pF | 5, 10, 15, 30 pF |
| $V_{MI}$ | $V_I/2$ | $V_I/2$ |
| $V_{MO}$ | $V_{CC}/2$ | $V_{CC}/2$ |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 7-1. Load Circuit and Voltage Waveforms**

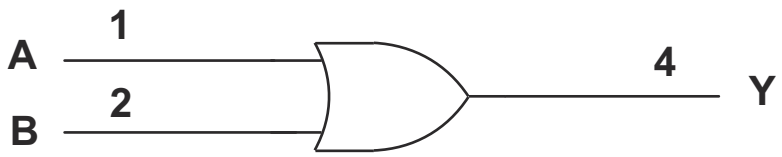

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# 8 Detailed Description

## 8.1 Overview

The SN74LV1T32 device is a low-voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels. The input is designed with a lower threshold circuit to match 1.8 V input logic at $V_{CC}$ = 3.3 V and can be used in 1.8 V to 3.3 V level-up translation. In addition, the 5 V tolerant input pins enable down translation (that is, 3.3 V to 2.5 V output at $V_{CC}$ = 2.5 V). The wide $V_{CC}$ range of 1.8 V to 5.5 V allows generation of desired output levels to connect to controllers or processors. The SN74LV1T32 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 8-1.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

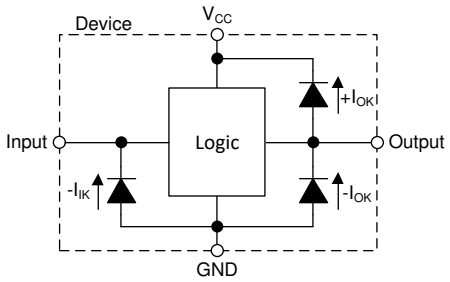



**Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output**

### 8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

### 8.3.3 LVxT Enhanced Input Voltage

The SN74LV1T32 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always

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be referenced to the supply voltage ($V_{CC}$), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 8-2 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at $V_{CC}$ or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

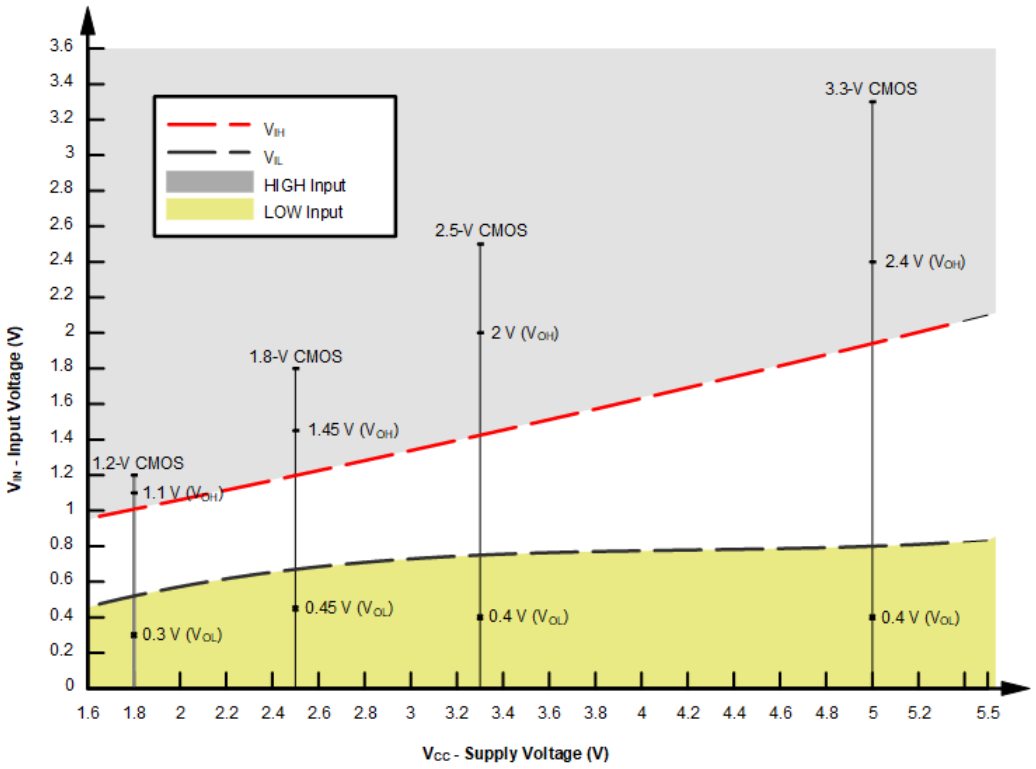



**Figure 8-2. LVxT Input Voltage Levels**

### *8.3.4 Down Translation*

Signals can be translated down using the SN74LV1T32. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state. As shown in Figure 8-2, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.


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As shown in Figure 8-3 for example, the standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V $V_{CC}$.

*Down Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5-V $V_{CC}$ – Inputs from 3.3 V and 5.0 V
- 3.3-V $V_{CC}$ – Inputs from 5.0 V

### *8.3.5 Up Translation*

Input signals can be up translated using the SN74LV1T32. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV1T32, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in #none#, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

*Up Translation Combinations* are as follows:

- 1.8-V $V_{CC}$ – Inputs from 1.2 V
- 2.5-V $V_{CC}$ – Inputs from 1.8 V
- 3.3-V $V_{CC}$ – Inputs from 1.8 V and 2.5 V
- 5.0-V $V_{CC}$ – Inputs from 2.5 V and 3.3 V

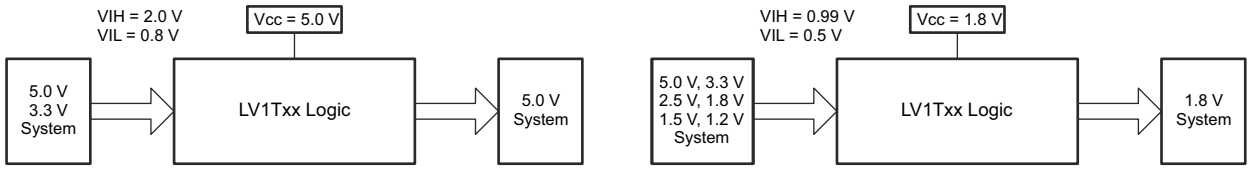



**Figure 8-3. LVxT Up and Down Translation Example**

## 8.4 Device Functional Modes

**Function Table**

| INPUT (LOWER LEVEL INPUT) | | OUTPUT ($V_{CC}$ CMOS) |
|---|---|---|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |
| **SUPPLY $V_{CC}$ = 3.3 V** | | |
| A | B | Y |
| $V_{IH}$(min) = 1.35 V<br>$V_{IL}$(max) = 0.08 V | | $V_{OH}$(min) = 2.9 V<br>$V_{OL}$(max) = 0.2 V |

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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

## 9.2 Layout

### *9.2.1 Layout Guidelines*

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or $V_{CC}$, whichever makes more sense for the logic function or is more convenient.

### *9.2.2 Layout Example*

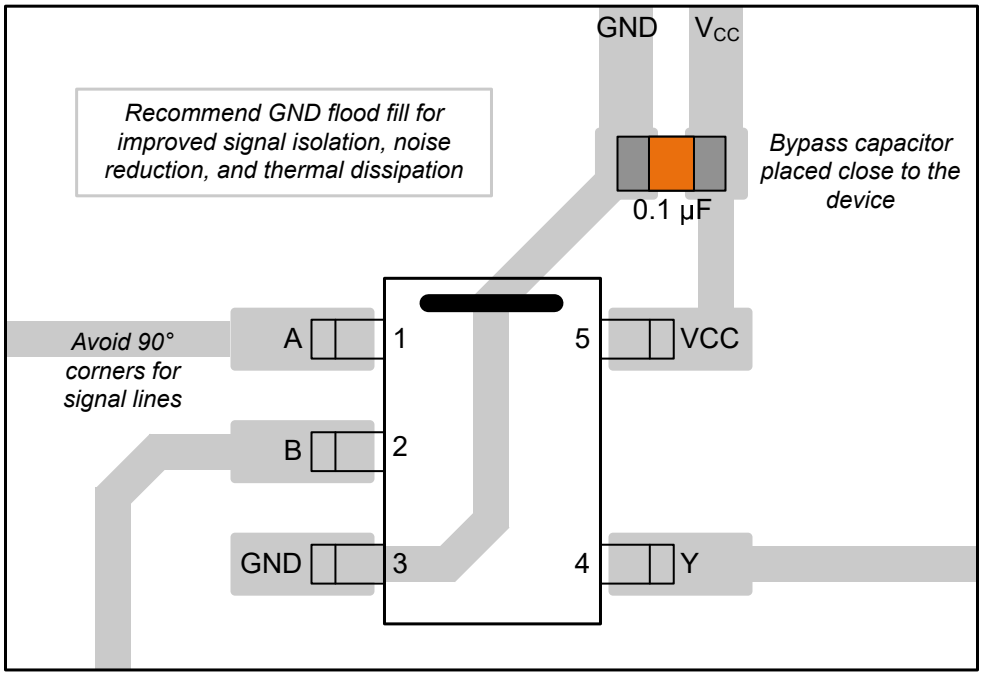



**Figure 9-1. Example Layout for the SN74LV1T32**


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# 10 Device and Documentation Support

## 10.1 Documentation Support (Analog)

### *10.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (October 2023) to Revision D (May 2024) | Page |
|---|---|
| • Updated RθJA values: DBV = 206 to 278, all values in °C/W | 7 |
| • Added *Feature Description* topics | 11 |

| Changes from Revision B (June 2022) to Revision C (October 2023) | Page |
|---|---|
| • Added package size to *Package Information* table | 1 |
| • Added Thermal Information table | 7 |
| • Added *Application and Implementation* section | 14 |

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## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV1T32DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (37XH, 3CIF, NEG3, NEGJ, NEGS) |
| SN74LV1T32DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (37XH, 3CIF, NEG3, NEGJ, NEGS) |
| SN74LV1T32DBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NEG3 |
| SN74LV1T32DBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NEG3 |
| SN74LV1T32DCKR | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1R2, WG3, WGJ, WGS) |
| SN74LV1T32DCKR.A | Active | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (1R2, WG3, WGJ, WGS) |
| SN74LV1T32DCKRG4 | Last Time Buy | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | - | WG3 |
| SN74LV1T32DCKRG4.A | Last Time Buy | Production | SC70 (DCK) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | WG3 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74LV1T32 :**

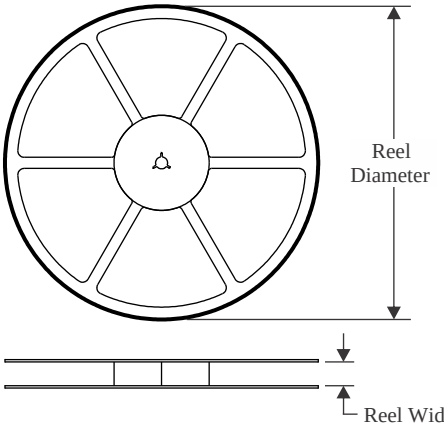
- Automotive : SN74LV1T32-Q1

NOTE: Qualified Version Definitions:

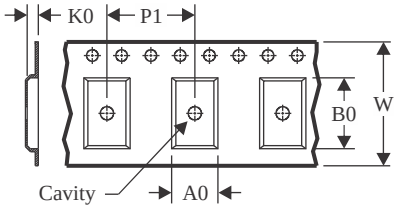
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

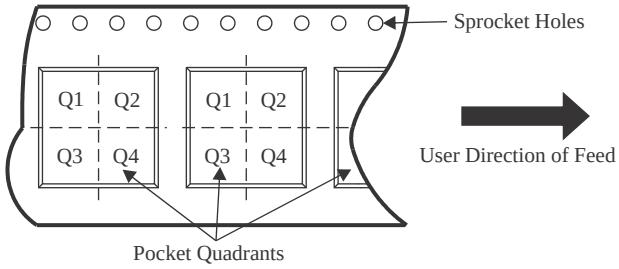



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

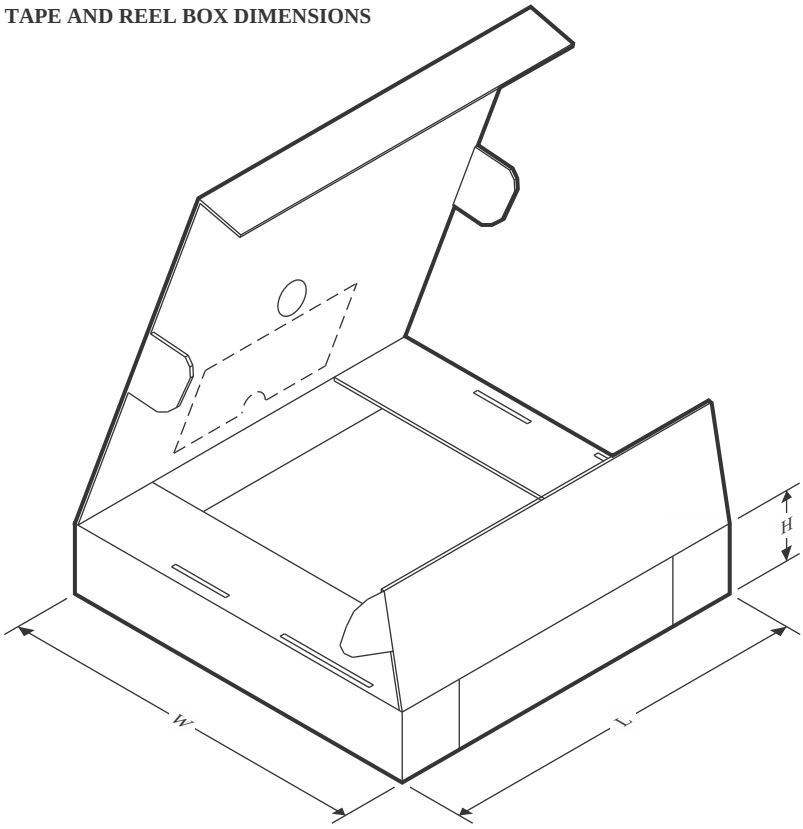
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV1T32DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LV1T32DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LV1T32DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LV1T32DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

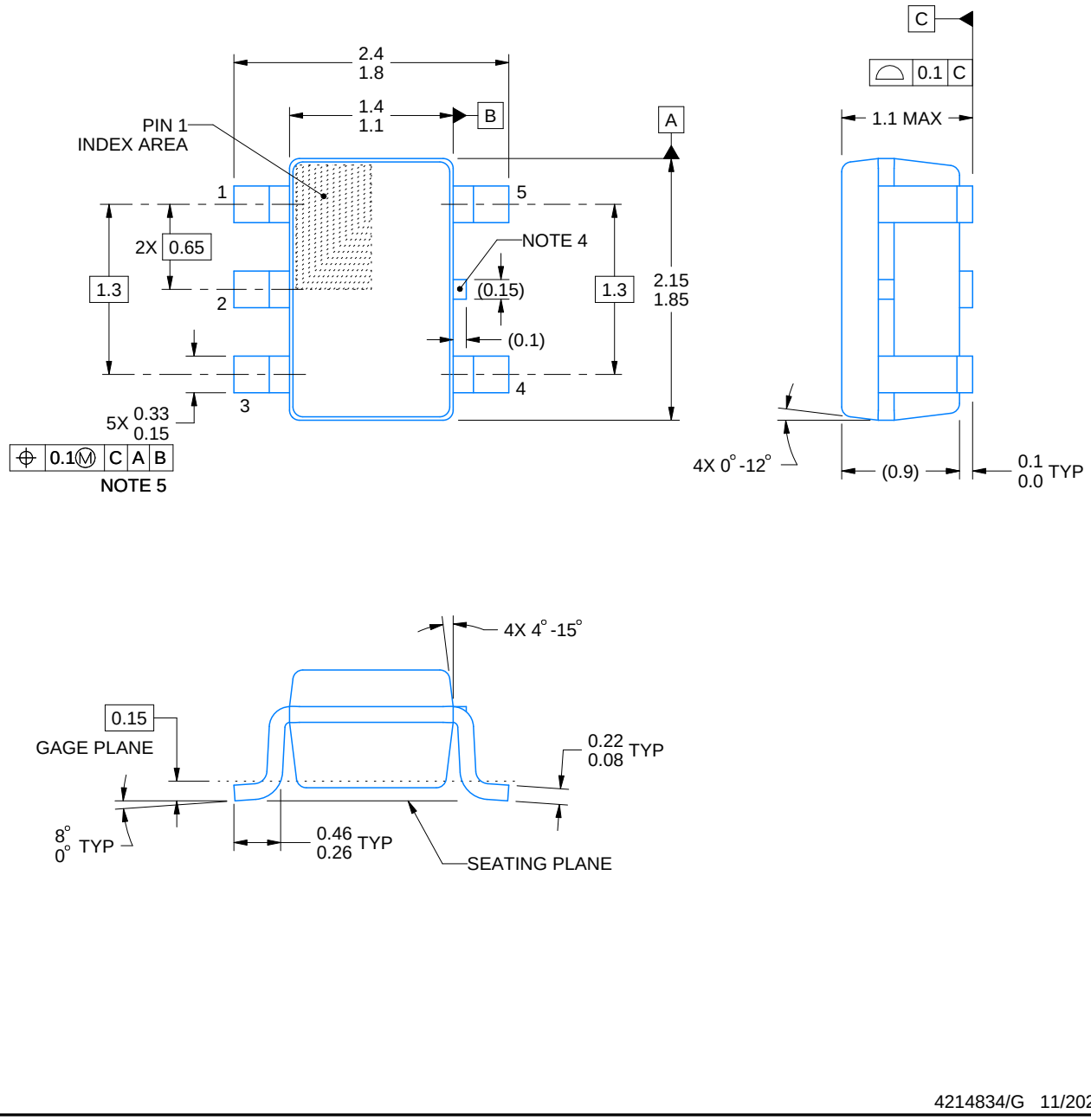
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV1T32DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LV1T32DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LV1T32DCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LV1T32DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DCK0005A

## SOT - 1.1 max height

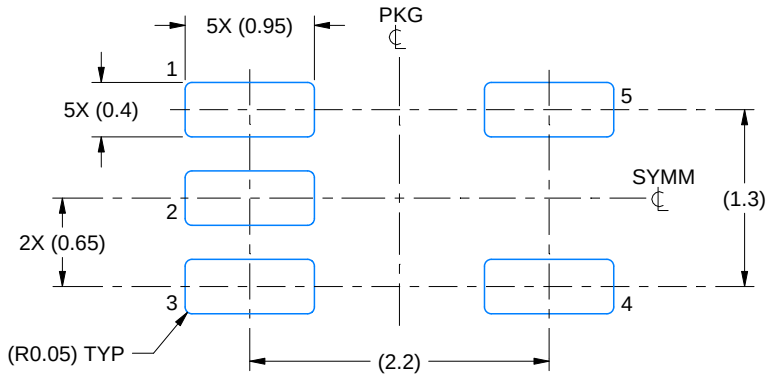
SMALL OUTLINE TRANSISTOR



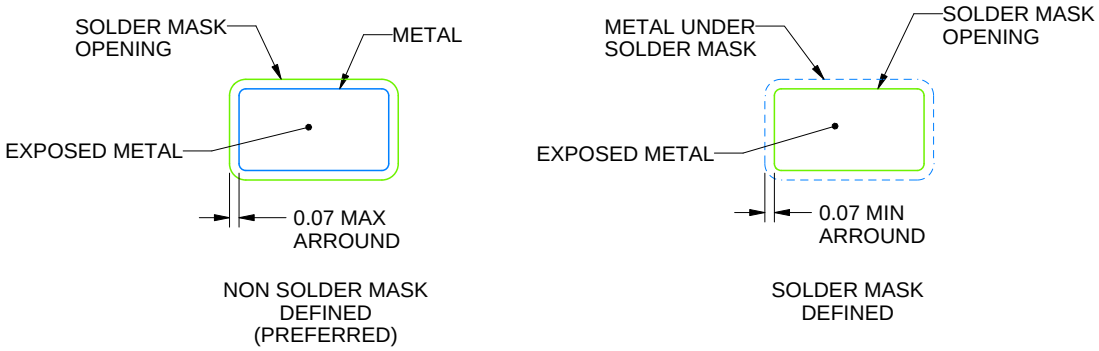

4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

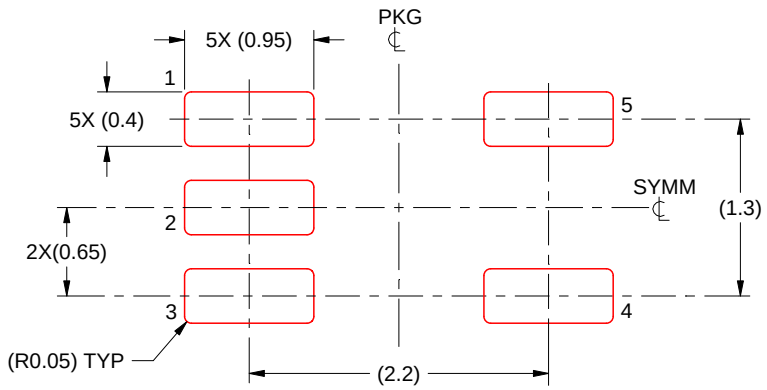



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

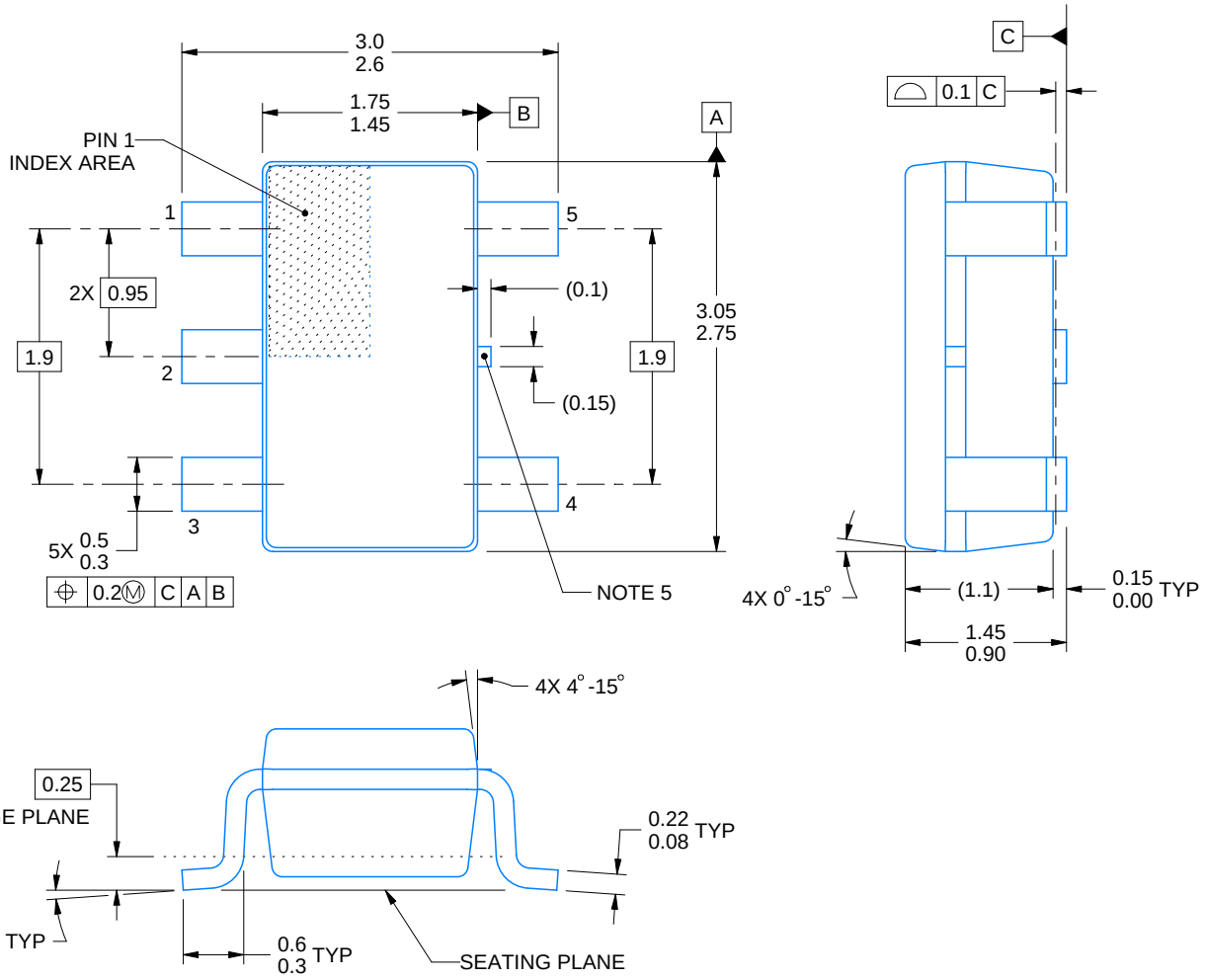
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

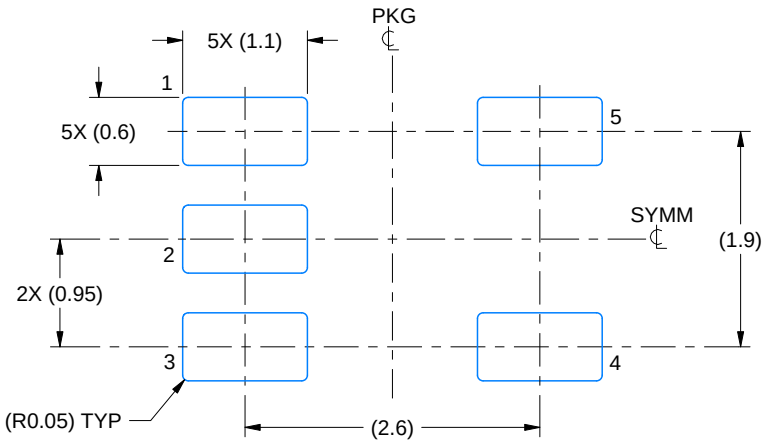
SMALL OUTLINE TRANSISTOR



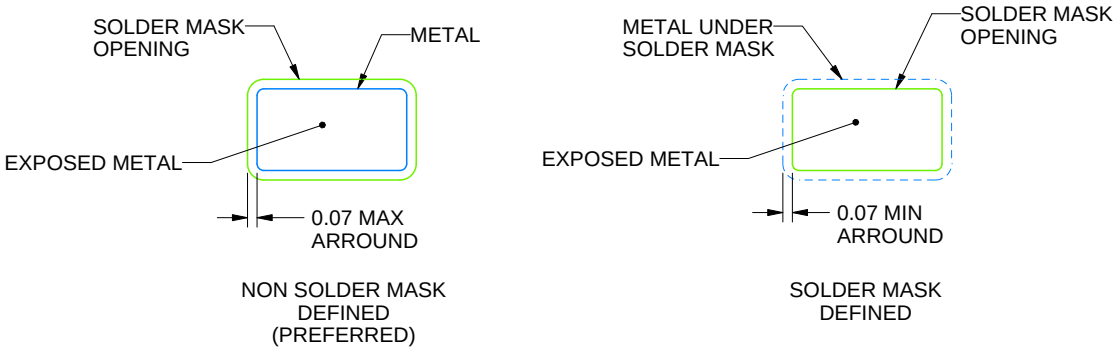

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

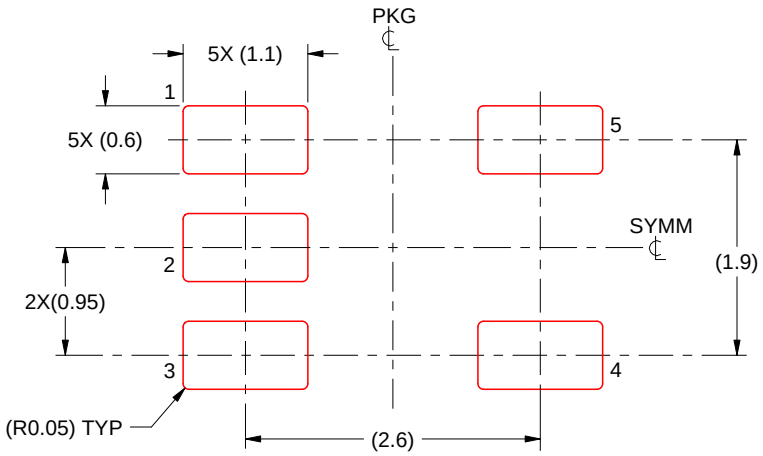



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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