# SN74LV3T99 Ultra-Configurable Multiple-Function Gates with 3-State Outputs and Logic-Level Shifter

## 1 Features

- Wide operating range of 1.65V to 5.5V
- 5.5V tolerant input pins
- Single-supply voltage translator (refer to *LVxT Enhanced Input Voltage*):
  - Up translation:
    - 1.2V to 1.8V
    - 1.5V to 2.5V
    - 1.8V to 3.3V
    - 3.3V to 5.0V
  - Down translation:
    - 5.0V, 3.3V, 2.5V to 1.8V
    - 5.0V, 3.3V to 2.5V
    - 5.0V to 3.3V
- Up to 150Mbps with 5V or 3.3V $V_{CC}$
- Supports standard function pinout
- Latch-up performance exceeds 100mA per JESD 17

## 2 Applications

- Digital signage
- Controlling an indicator LED
- Increase the number of outputs on a microcontroller

## 3 Description

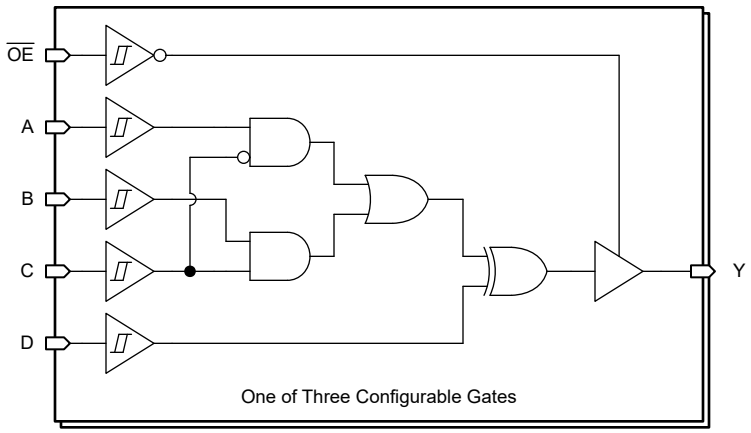
The SN74LV3T99 device contains three independent configurable logic gates with 3-state outputs. Each gate has four inputs and performs the Boolean function $Y = (A \bullet \overline{C} + B \bullet C) \oplus D$. All inputs include Schmitt-triggers, eliminating any erroneous data outputs due to slow-edged or noisy input signals. The user can choose logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer by connecting the inputs A, B, C, and D appropriately.

The input is designed with a reduced threshold circuit to support up translation when the supply voltage is larger than the input voltage. Additionally, the 5V tolerant input pins enable down translation when the input voltage is larger than the supply voltage. The output level is always referenced to the supply voltage ($V_{CC}$) and supports 1.8V, 2.5V, 3.3V, and 5V CMOS levels.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN74LV3T99 | PW (TSSOP, 20) | 6.5mm × 6.4mm | 6.5mm × 4.4mm |
| | DGS (VSSOP, 20) | 5.1mm × 4.9mm | 5.1mm × 3.0mm |
| | RKS (VQFN, 20) | 4.5mm × 2.5mm | 4.5mm × 2.5mm |

(1) For more information, see Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Functional Block Diagram**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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# 4 Pin Configuration and Functions

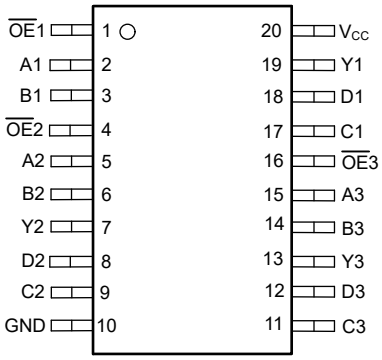



**Figure 4-1. PW or DGS Package, 20-Pin TSSOP or VSSOP (Top View)**

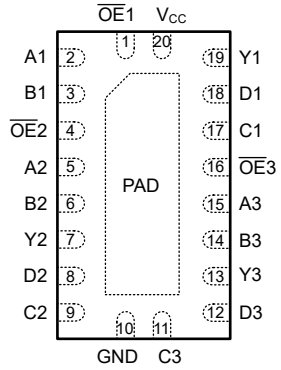



**Figure 4-2. RKS Package, 20-Pin VQFN (Transparent Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A1 | 2 | I | Channel 1, Input A |
| A2 | 5 | I | Channel 2, Input A |
| A3 | 15 | I | Channel 3, Input A |
| B1 | 3 | I | Channel 1, Input B |
| B2 | 6 | I | Channel 2, Input B |
| B3 | 14 | I | Channel 3, Input B |
| C1 | 17 | I | Channel 1, Input C |
| C2 | 9 | I | Channel 2, Input C |
| C3 | 11 | I | Channel 3, Input C |
| D1 | 18 | I | Channel 1, Input D |
| D2 | 8 | I | Channel 2, Input D |
| D3 | 12 | I | Channel 3, Input D |
| GND | 10 | G | Ground |
| $\overline{OE}$1 | 1 | I | Output enable input for Channel 1, active-low |
| $\overline{OE}$2 | 4 | I | Output enable input for Channel 2, active-low |
| $\overline{OE}$3 | 16 | I | Output enable input for Channel 3, active-low |
| Thermal Pad[2] | | — | The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply. |
| $V_{CC}$ | 20 | P | Positive supply |
| Y1 | 19 | O | Channel 1, Output Y |
| Y2 | 7 | O | Channel 2, Output Y |
| Y3 | 13 | O | Channel 3, Output Y |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power
(2) RKS package only.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 7 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 7 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < -0.5V | | -20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±25 | mA |
| | Continuous output current through $V_{CC}$ or GND | | | ±75 | mA |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| Spec | Description | Condition | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65V to 2V | 1.1 | | V |
| | | $V_{CC}$ = 2.25V to 2.75V | 1.28 | | |
| | | $V_{CC}$ = 3V to 3.6V | 1.45 | | |
| | | $V_{CC}$ = 4.5V to 5.5V | 2 | | |
| $V_{IL}$ | Low-Level input voltage | $V_{CC}$ = 1.65V to 2V | | 0.51 | V |
| | | $V_{CC}$ = 2.25V to 2.75V | | 0.65 | |
| | | $V_{CC}$ = 3V to 3.6V | | 0.75 | |
| | | $V_{CC}$ = 4.5V to 5.5V | | 0.8 | |
| $I_O$ | Output current | $V_{CC}$ = 1.6V to 2V | | ±8 | mA |
| | | $V_{CC}$ = 2.25V to 2.75V | | ±15 | |
| | | $V_{CC}$ = 3.3V to 5.0V | | ±25 | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 1.6V to 5.0V | | 20 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 125 | °C |


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## 5.4 Thermal Information

| PACKAGE | PINS | THERMAL METRIC(1) | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $R_{\theta JA}$ | $R_{\theta JC(top)}$ | $R_{\theta JB}$ | $\Psi_{JT}$ | $\Psi_{JB}$ | $R_{\theta JC(bot)}$ | |
| DGS (VSSOP) | 20 | 131.6 | 69.5 | 86.7 | 10.9 | 85.9 | N/A | °C/W |
| PW (TSSOP) | 20 | 116.8 | 58.5 | 78.7 | 12.6 | 77.9 | N/A | °C/W |
| RKS (VQFN) | 20 | 90.4 | 92.2 | 63.4 | 29 | 63.5 | 41.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{T+}$ | | 1.65V to 2V | 0.6 | | 1.2 | 0.5 | | 1.27 | V |
| | | 2.25V to 2.75V | 0.73 | | 1.39 | 0.64 | | 1.44 | V |
| | | 3V to 3.6V | 0.88 | | 1.59 | 0.80 | | 1.63 | V |
| | | 4.5V to 5.5V | 1.15 | | 2.03 | 1.1 | | 2.07 | V |
| $V_{T-}$ | | 1.65V to 2V | 0.225 | | 0.685 | 0.185 | | 0.755 | V |
| | | 2.25V to 2.75V | 0.295 | | 0.775 | 0.265 | | 0.805 | V |
| | | 3V to 3.6V | 0.385 | | 0.875 | 0.345 | | 0.895 | V |
| | | 4.5V to 5.5V | 0.535 | | 1.075 | 0.495 | | 1.085 | V |
| $\Delta V_T$ | | 1.65V to 2V | 0.35 | | 0.68 | 0.28 | | 0.8 | V |
| | | 2.25V to 2.75V | 0.4 | | 0.77 | 0.33 | | 0.87 | V |
| | | 3V to 3.6V | 0.44 | | 0.88 | 0.38 | | 0.91 | V |
| | | 4.5V to 5.5V | 0.53 | | 1.2 | 0.51 | | 1.4 | V |
| $V_{OH}$ | $I_{OH}$ = -50 uA | 1.65V to 5.5V | $V_{CC}$-0.1 | | | $V_{CC}$-0.1 | | | V |
| | $I_{OH}$ = -2mA | 1.65V to 2V | 1.28 | 1.7 (1) | | 1.21 | | | |
| | $I_{OH}$ = -3mA | 2.25V to 2.75V | 2 | 2.4(1) | | 1.93 | | | |
| | $I_{OH}$ = -5.5mA | 3V to 3.6V | 2.6 | 3.08(1) | | 2.49 | | | |
| | $I_{OH}$ = -8mA | 4.5V to 5.5V | 4.1 | 4.65(1) | | 3.95 | | | |
| $V_{OL}$ | $I_{OL}$ = 50 uA | 1.65V to 5.5V | | | 0.1 | | | 0.1 | V |
| | $I_{OL}$ = 2mA | 1.65V to 2V | | 0.1(1) | 0.2 | | | 0.25 | |
| | $I_{OL}$ = 3mA | 2.25V to 2.75V | | 0.15(1) | 0.17 | | | 0.2 | |
| | $I_{OL}$ = 5.5mA | 3V to 3.6V | | 0.2(1) | 0.23 | | | 0.25 | |
| | $I_{OL}$ = 8mA | 4.5V to 5.5V | | 0.3(1) | 0.3 | | | 0.35 | |

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## 5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_I$ | $V_I$ = 0V or $V_{CC}$ | 0V to 5.5V | | | ±0.1 | | | ±1 | µA |
| $I_{CC}$ | $V_I$ = 0V or $V_{CC}$, $I_O$ = 0; open on loading | 1.65V to 5.5V | | | 2 | | | 20 | µA |
| $\Delta I_{CC}$ | One input at 0.3V or 3.4V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 5.5V | | | 1.35 | | | 1.5 | mA |
| | One input at 0.3V or 1.1V, other inputs at 0 or $V_{CC}$, $I_O$ = 0 | 1.8V | | | 10 | | | 20 | µA |
| $I_{OZ}$ | $V_O$ = $V_{CC}$ or GND and $V_{CC}$ = 5.5V | 5.5V | | | ±0.25 | | | ±2.5 | µA |
| $C_I$ | $V_I$ = $V_{CC}$ or GND | 5V | | 4 | 10 | | | 10 | pF |
| $C_O$ | $V_O$ = $V_{CC}$ or GND | 5V | | 5 | | | | | pF |
| $C_{PD}$ | No load, F = 1MHz | 5V | | 20 | | | | | pF |

(1) Typical value at nearest nominal voltage (1.8V, 2.5V, 3.3V, and 5V)

## 5.6 Switching Characteristics

Over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 15pF | 1.8V | 6.8 | | 22.4 | 6.1 | | 25.3 | ns |
| $t_{PHL}$ | | | | 1.8V | 7 | | 23.9 | 6.2 | | 26.7 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 15pF | 1.8V | 6.7 | | 22.4 | 6 | | 25.3 | ns |
| $t_{PHL}$ | | | | 1.8V | 6.9 | | 23.9 | 6.1 | | 26.7 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 15pF | 1.8V | 6.6 | | 21.7 | 6 | | 24.4 | ns |
| $t_{PHL}$ | | | | 1.8V | 7.4 | | 23.3 | 6.5 | | 26 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 15pF | 1.8V | 6.2 | | 20.2 | 5.6 | | 22.7 | ns |
| $t_{PHL}$ | | | | 1.8V | 6.5 | | 21.8 | 5.8 | | 24.2 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 50pF | 1.8V | 8.8 | | 26.8 | 7.7 | | 30.1 | ns |
| $t_{PHL}$ | | | | 1.8V | 8.7 | | 27.7 | 7.8 | | 31 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 50pF | 1.8V | 8.7 | | 26.7 | 7.7 | | 30 | ns |
| $t_{PHL}$ | | | | 1.8V | 8.6 | | 27.7 | 7.7 | | 31 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 50pF | 1.8V | 8.6 | | 26.1 | 7.7 | | 29.3 | ns |
| $t_{PHL}$ | | | | 1.8V | 9.1 | | 27.2 | 8.1 | | 30.3 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 50pF | 1.8V | 8.2 | | 24.6 | 7.3 | | 27.5 | ns |
| $t_{PHL}$ | | | | 1.8V | 8.2 | | 25.6 | 7.4 | | 28.5 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 15pF | 2.5V | 4.9 | | 13.6 | 4.3 | | 15.8 | ns |
| $t_{PHL}$ | | | | 2.5V | 4.7 | | 14.1 | 4.1 | | 16.4 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 15pF | 2.5V | 4.8 | | 13.6 | 4.2 | | 15.8 | ns |
| $t_{PHL}$ | | | | 2.5V | 4.7 | | 14.1 | 4.1 | | 16.4 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 15pF | 2.5V | 4.8 | | 13.2 | 4.2 | | 15.4 | ns |
| $t_{PHL}$ | | | | 2.5V | 4.9 | | 13.8 | 4.3 | | 16 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 15pF | 2.5V | 4.5 | | 12.4 | 4 | | 14.4 | ns |
| $t_{PHL}$ | | | | 2.5V | 4.4 | | 13 | 3.9 | | 15.1 | ns |


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## 5.6 Switching Characteristics (continued)

Over operating free-air temperature range; typical values measured at $T_A$ = 25°C (unless otherwise noted). See *Parameter Measurement Information*.

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $V_{CC}$ | $T_A$ = 25°C | | | -40°C to 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A | Y | $C_L$ = 50pF | 2.5V | 6.2 | | 16.4 | 5.5 | | 19.1 | ns |
| $t_{PHL}$ | | | | 2.5V | 6.1 | | 16.7 | 5.4 | | 19.4 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 50pF | 2.5V | 6.2 | | 16.4 | 5.5 | | 19.1 | ns |
| $t_{PHL}$ | | | | 2.5V | 6 | | 16.7 | 5.3 | | 19.5 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 50pF | 2.5V | 6.2 | | 16.1 | 5.5 | | 18.6 | ns |
| $t_{PHL}$ | | | | 2.5V | 6.3 | | 16.4 | 5.6 | | 19 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 50pF | 2.5V | 5.9 | | 15.3 | 5.2 | | 17.7 | ns |
| $t_{PHL}$ | | | | 2.5V | 5.8 | | 15.5 | 5.2 | | 18 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 15pF | 3.3V | 4.2 | | 11.4 | 3.7 | | 13.3 | ns |
| $t_{PHL}$ | | | | 3.3V | 3.9 | | 11.6 | 3.4 | | 13.5 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 15pF | 3.3V | 4.2 | | 11.3 | 3.7 | | 13.2 | ns |
| $t_{PHL}$ | | | | 3.3V | 3.9 | | 11.4 | 3.4 | | 13.5 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 15pF | 3.3V | 4.2 | | 11.1 | 3.7 | | 13 | ns |
| $t_{PHL}$ | | | | 3.3V | 4 | | 11.2 | 3.5 | | 13.2 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 15pF | 3.3V | 4 | | 10.5 | 3.5 | | 12.2 | ns |
| $t_{PHL}$ | | | | 3.3V | 3.6 | | 10.6 | 3.2 | | 12.4 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 50pF | 3.3V | 5.4 | | 13.9 | 4.8 | | 16.1 | ns |
| $t_{PHL}$ | | | | 3.3V | 5.1 | | 13.9 | 4.6 | | 16.1 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 50pF | 3.3V | 5.4 | | 13.8 | 4.7 | | 16.1 | ns |
| $t_{PHL}$ | | | | 3.3V | 5.1 | | 13.8 | 4.6 | | 16.1 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 50pF | 3.3V | 5.4 | | 13.5 | 4.8 | | 15.7 | ns |
| $t_{PHL}$ | | | | 3.3V | 5.3 | | 13.6 | 4.7 | | 15.8 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 50pF | 3.3V | 5.1 | | 13 | 4.5 | | 15 | ns |
| $t_{PHL}$ | | | | 3.3V | 4.9 | | 13 | 4.4 | | 15.1 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 15pF | 5V | 3.8 | | 8.4 | 3.5 | | 9.7 | ns |
| $t_{PHL}$ | | | | 5V | 3.3 | | 8.1 | 3 | | 9.4 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 15pF | 5V | 3.8 | | 8.4 | 3.5 | | 9.7 | ns |
| $t_{PHL}$ | | | | 5V | 3.3 | | 8.1 | 3 | | 9.4 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 15pF | 5V | 3.8 | | 8.3 | 3.5 | | 9.6 | ns |
| $t_{PHL}$ | | | | 5V | 3.4 | | 7.9 | 3.1 | | 9.2 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 15pF | 5V | 3.6 | | 8 | 3.3 | | 9.1 | ns |
| $t_{PHL}$ | | | | 5V | 3.2 | | 7.5 | 2.8 | | 8.7 | ns |
| $t_{PLH}$ | A | Y | $C_L$ = 50pF | 5V | 4.7 | | 10.2 | 4.3 | | 11.7 | ns |
| $t_{PHL}$ | | | | 5V | 4.4 | | 9.8 | 3.9 | | 11.4 | ns |
| $t_{PLH}$ | B | Y | $C_L$ = 50pF | 5V | 4.7 | | 10.1 | 4.3 | | 11.7 | ns |
| $t_{PHL}$ | | | | 5V | 4.3 | | 9.8 | 3.9 | | 11.4 | ns |
| $t_{PLH}$ | C | Y | $C_L$ = 50pF | 5V | 4.8 | | 10 | 4.2 | | 11.6 | ns |
| $t_{PHL}$ | | | | 5V | 4.4 | | 9.7 | 4 | | 11.2 | ns |
| $t_{PLH}$ | D | Y | $C_L$ = 50pF | 5V | 4.6 | | 9.6 | 4.1 | | 11.1 | ns |
| $t_{PHL}$ | | | | 5V | 4.2 | | 9.3 | 3.8 | | 10.8 | ns |

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## 5.7 Typical Characteristics

$T_A$ = 25°C (unless otherwise noted)

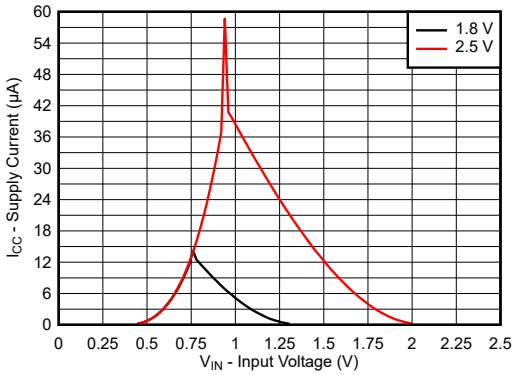



**Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply**

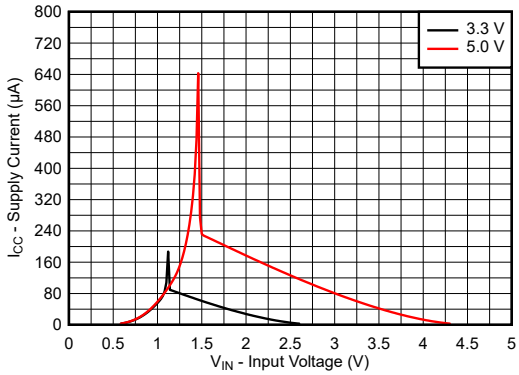



**Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply**

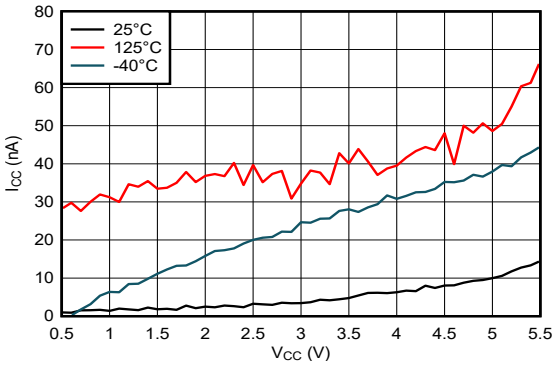



**Figure 5-3. Supply Current Across Supply Voltage**

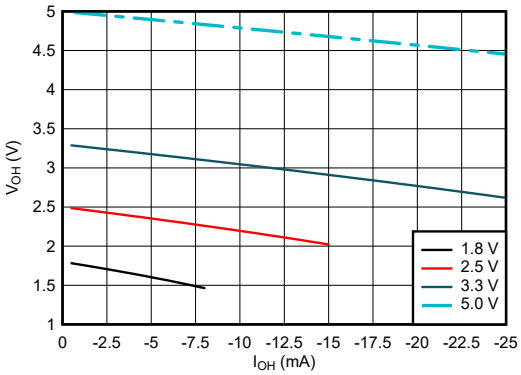



**Figure 5-4. Output Voltage vs Current in HIGH State**

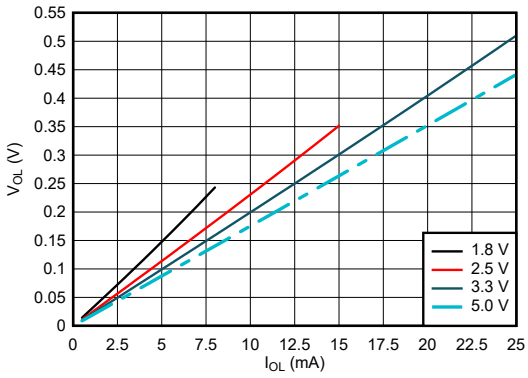



**Figure 5-5. Output Voltage vs Current in LOW State**

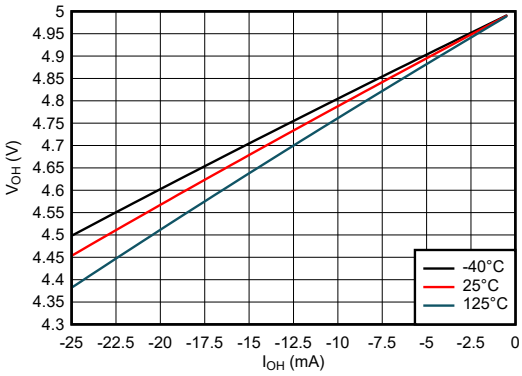



**Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply**


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## 5.7 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

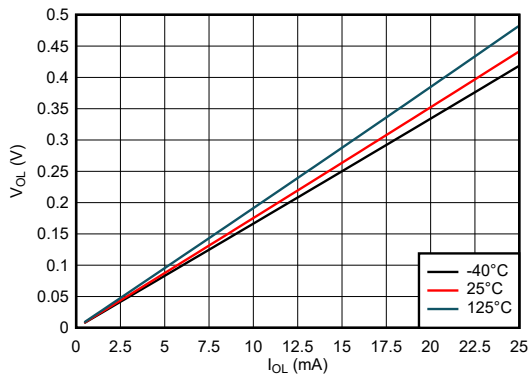



**Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply**

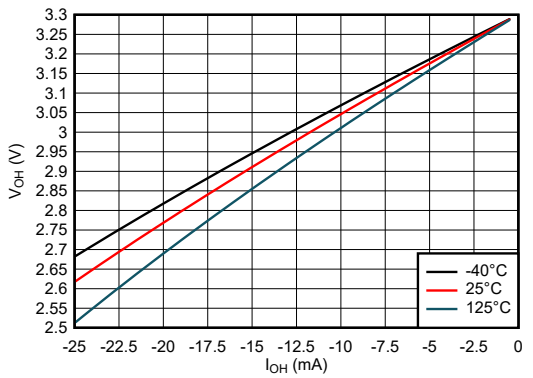



**Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply**

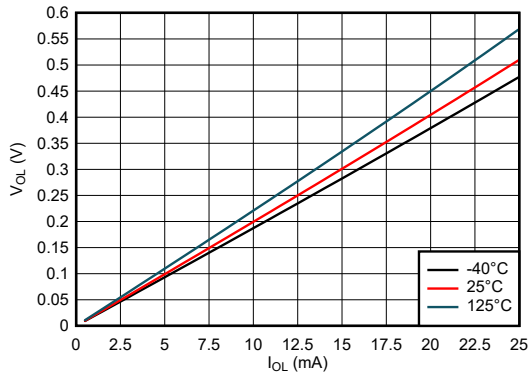



**Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply**

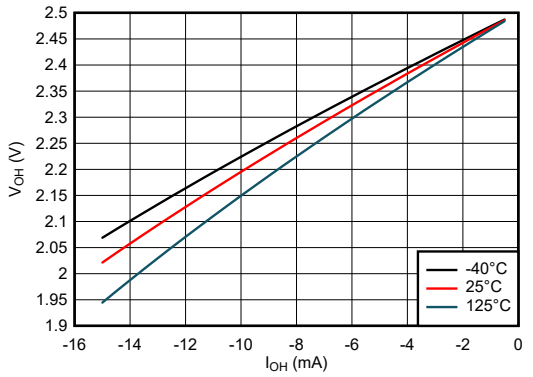



**Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply**

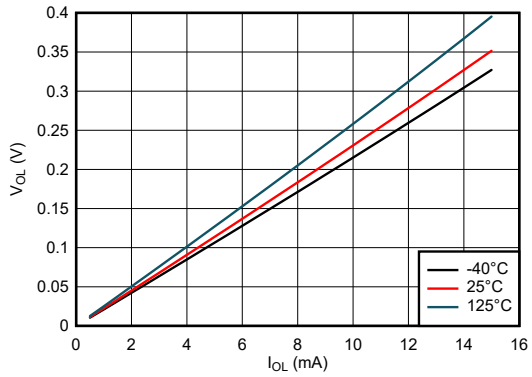



**Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply**

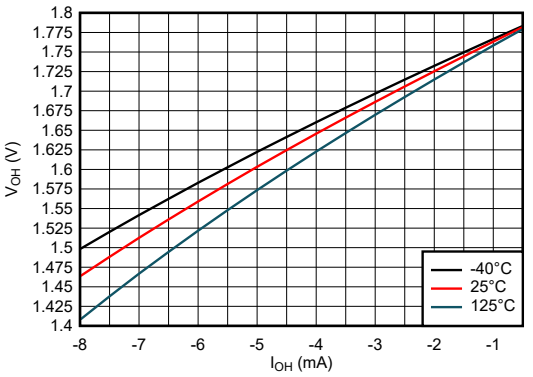



**Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply**

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## 5.7 Typical Characteristics (continued)

$T_A$ = 25°C (unless otherwise noted)

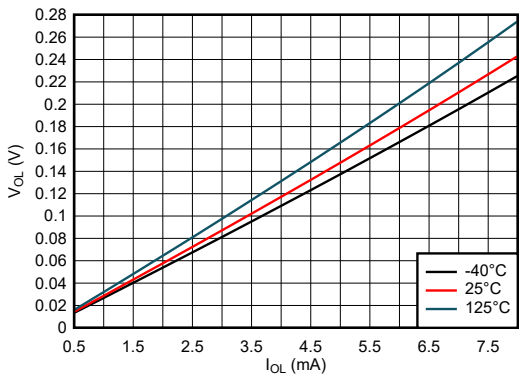



**Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply**

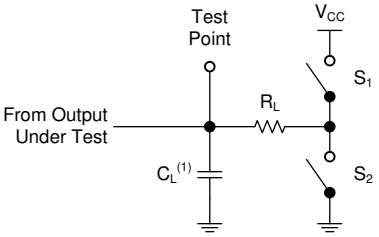

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## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, $Z_O$ = 50Ω, $t_t$ < 2.5ns.

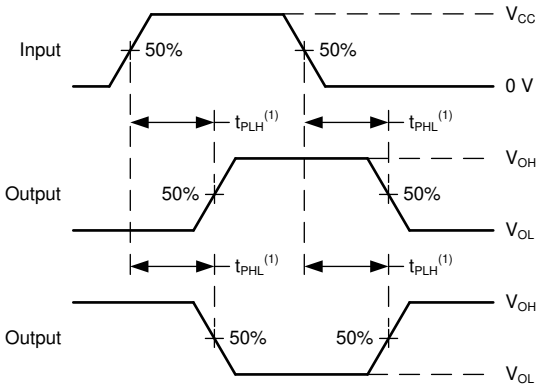
The outputs are measured individually with one input transition per measurement.

| TEST | S1 | S2 | $R_L$ | $C_L$ | ΔV | $V_{CC}$ |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | OPEN | OPEN | — | 15pF, 50pF | — | ALL |
| $t_{PLZ}$, $t_{PZL}$ | CLOSED | OPEN | 1kΩ | 15pF, 50pF | 0.15V | ≤ 2.5V |
| $t_{PHZ}$, $t_{PZH}$ | OPEN | CLOSED | 1kΩ | 15pF, 50pF | 0.15V | ≤ 2.5V |
| $t_{PLZ}$, $t_{PZL}$ | CLOSED | OPEN | 1kΩ | 15pF, 50pF | 0.3V | > 2.5V |
| $t_{PHZ}$, $t_{PZH}$ | OPEN | CLOSED | 1kΩ | 15pF, 50pF | 0.3V | > 2.5V |



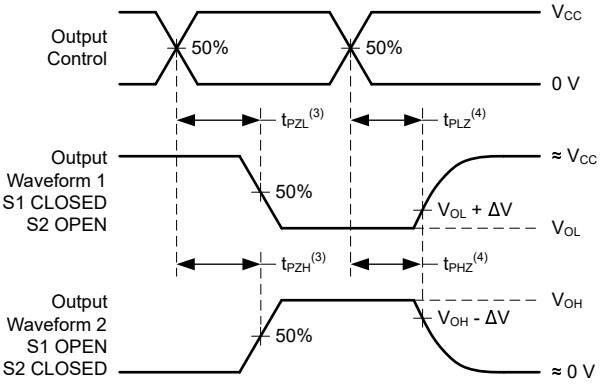

(1) $C_L$ includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**




(1) The greater between $t_{PLH}$ and $t_{PHL}$ is the same as $t_{pd}$.

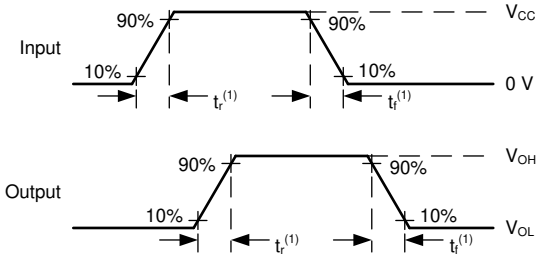
**Figure 6-2. Voltage Waveforms Propagation Delays**




(3) The greater between $t_{PZL}$ and $t_{PZH}$ is the same as $t_{en}$.

(4) The greater between $t_{PLZ}$ and $t_{PHZ}$ is the same as $t_{dis}$.

**Figure 6-3. Voltage Waveforms Propagation Delays**




(1) The greater between $t_r$ and $t_f$ is the same as $t_t$.

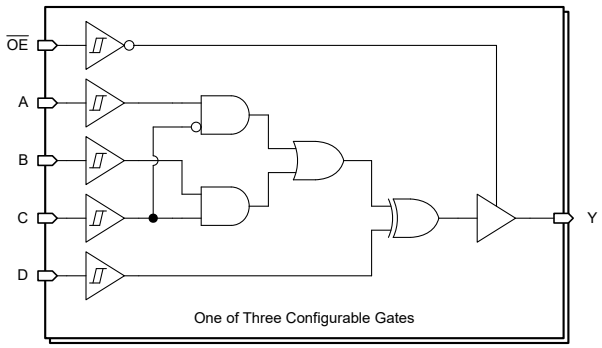
**Figure 6-4. Voltage Waveforms, Input and Output Transition Times**

# 7 Detailed Description

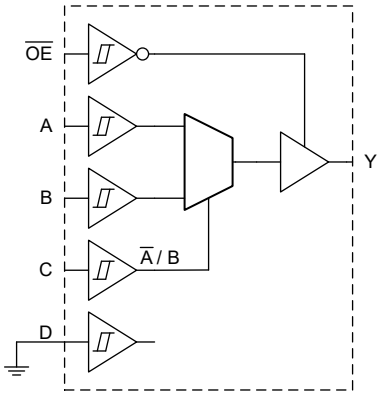
## 7.1 Overview

The SN74LV3T99 device contains three independent ultra-configurable gates with 3-state outputs. Each gate has an independent active-low output enable ($\overline{OE}$). Each channel of the device performs the boolean function $Y = (A \bullet \overline{C} + B \bullet C) \oplus D$. The user can choose logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer by connecting the inputs A, B, C, and D appropriately.

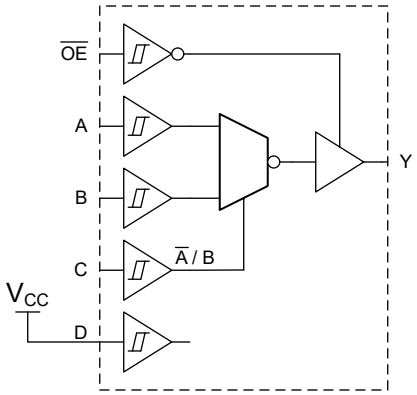
## 7.2 Functional Block Diagram



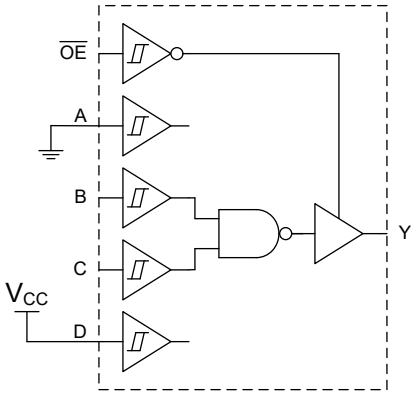

## 7.3 Combinatorial Logic Configurations



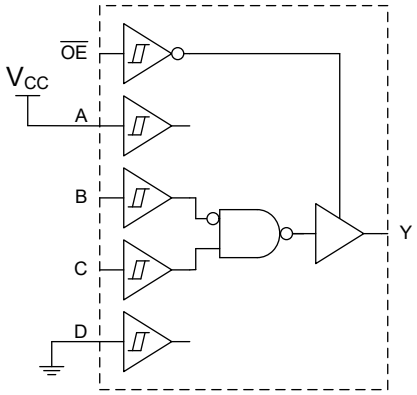

**2-to-1 data selector**




**2-to-1 data selector with inverted output**

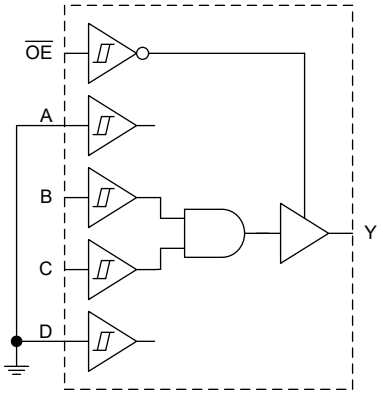



**2-Input NAND**

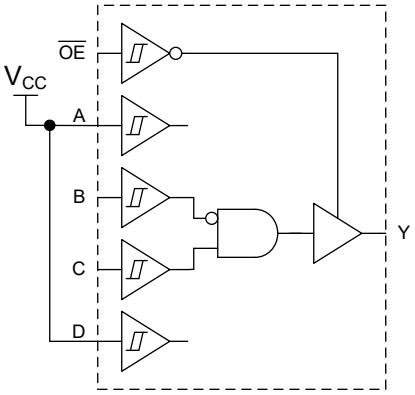



**2-Input NAND with 1 inverted input**

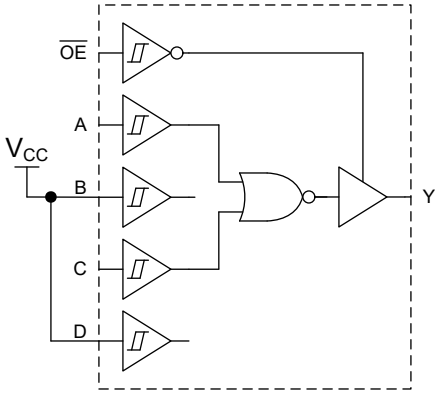

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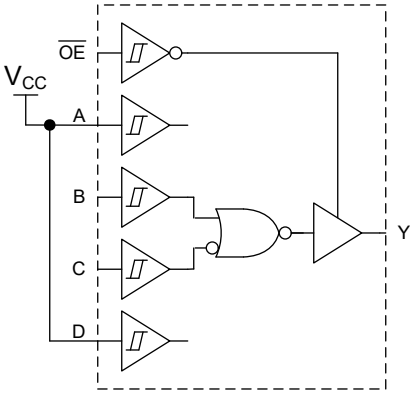

**2-Input AND**



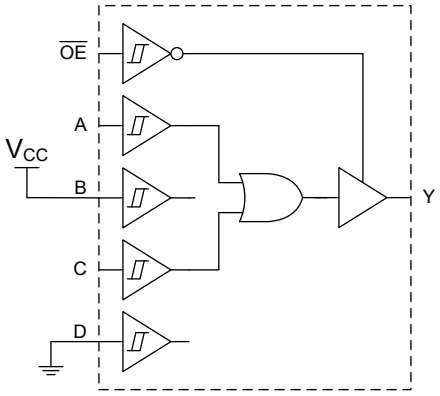

**2-Input AND with 1 inverted input**



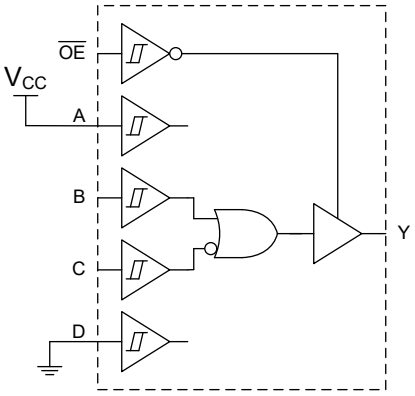

**2-Input NOR**




**2-Input NOR with 1 inverted input**

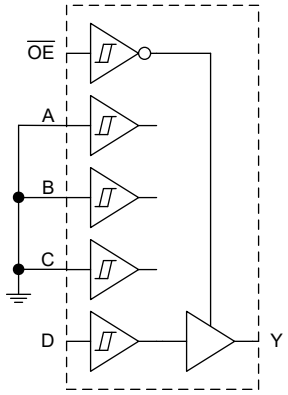



**2-Input OR**

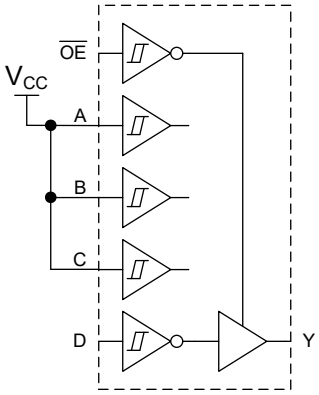



**2-Input OR with 1 inverted input**

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Schmitt-trigger buffer




Schmitt-trigger inverter

**Figure 7-1. Logic Configurations**


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## 7.4 Feature Description

### *7.4.1 Balanced CMOS 3-State Outputs*

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10kΩ resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

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### 7.4.2 LVxT Enhanced Input Voltage

The SN74LV3T99 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5V levels to support down-translation. For proper functionality, input signals must remain at or above the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. Figure 7-2 shows the typical $V_{IH}$ and $V_{IL}$ levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by $\Delta V_T$ in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see *Understanding Schmitt Triggers*.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at a valid high or low voltage level. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10kΩ resistor is recommended and will typically meet all requirements.

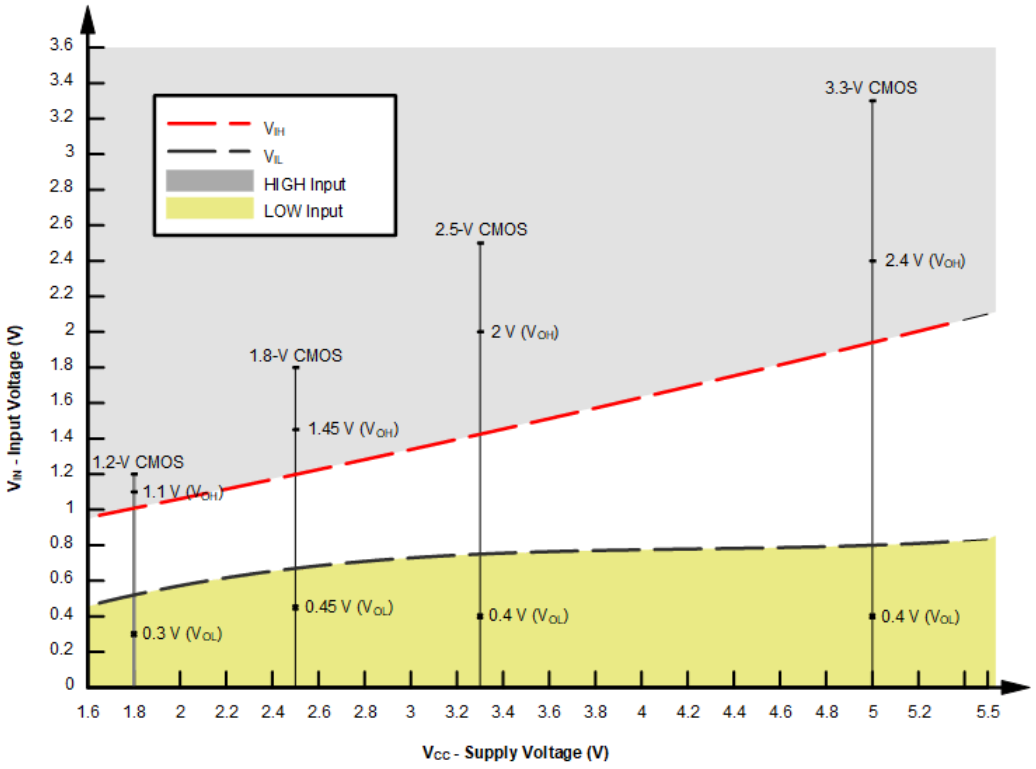



**Figure 7-2. LVxT Input Voltage Levels**


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#### 7.4.2.1 Up Translation

Input signals can be up translated using the SN74LV3T99. The voltage applied at $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5V supply will have a $V_{IH(MIN)}$ of 3.5V. For the SN74LV3T99, $V_{IH(MIN)}$ with a 5V supply is only 2V, which would allow for up-translation from a typical 2.5V to 5V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-3.

*Up Translation Combinations* are as follows:

- 1.8V $V_{CC}$ – Inputs from 1.2V
- 2.5V $V_{CC}$ – Inputs from 1.8V
- 3.3V $V_{CC}$ – Inputs from 1.8V and 2.5V
- 5.0V $V_{CC}$ – Inputs from 2.5V and 3.3V

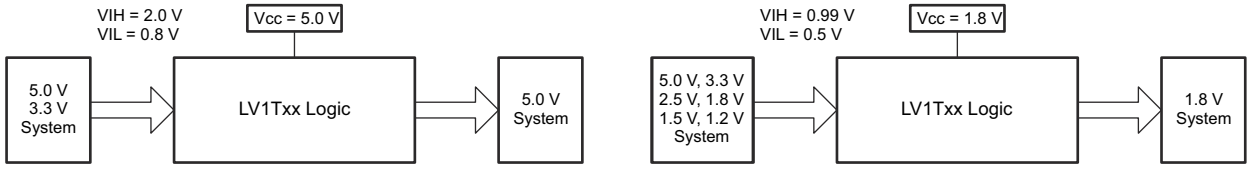



**Figure 7-3. LVxT Up and Down Translation Example**

#### 7.4.2.2 Down Translation

Signals can be translated down using the SN74LV3T99. The voltage applied at the $V_{CC}$ will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately $V_{CC}$ in the HIGH state, and 0V in the LOW state. Ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5V, and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 7-2.

For example, standard CMOS inputs for devices operating at 5.0V, 3.3V or 2.5V can be down-translated to match 1.8V CMOS signals when operating from 1.8V $V_{CC}$. See Figure 7-3.

*Down Translation Combinations* are as follows:

- 1.8V $V_{CC}$ – Inputs from 2.5V, 3.3V, and 5.0V
- 2.5V $V_{CC}$ – Inputs from 3.3V and 5.0V
- 3.3V $V_{CC}$ – Inputs from 5.0V

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### 7.4.3 Clamp Diode Structure

As Figure 7-4 shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

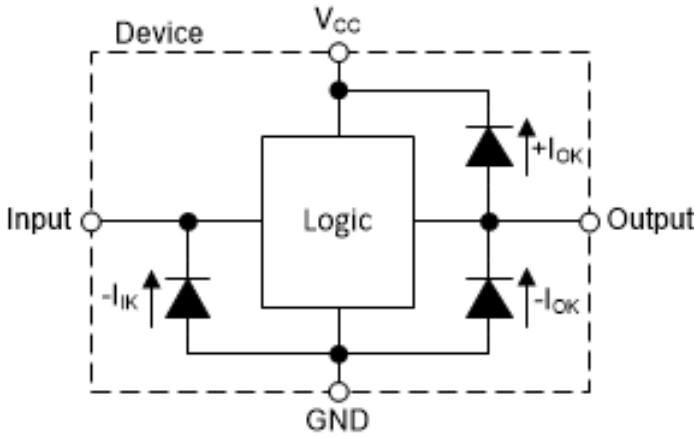



**Figure 7-4. Electrical Placement of Clamping Diodes for Each Input and Output**

## 7.5 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LV3T99.

**Table 7-1. Function Table**

| INPUTS[1] | | | | | OUTPUTS[2] |
|---|---|---|---|---|---|
| $\overline{OE}$ | D | C | B | A | Y |
| L | L | L | L | L | L |
| L | L | L | L | H | H |
| L | L | L | H | L | L |
| L | L | L | H | H | H |
| L | L | H | L | L | L |
| L | L | H | L | H | L |
| L | L | H | H | L | H |
| L | L | H | H | H | H |
| L | H | L | L | L | H |
| L | H | L | L | H | L |
| L | H | L | H | L | H |
| L | H | L | H | H | L |
| L | H | H | L | L | H |
| L | H | H | L | H | H |
| L | H | H | H | L | L |
| L | H | H | H | H | L |


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**Table 7-1. Function Table (continued)**

| INPUTS(1) | | | | | OUTPUTS(2) |
|---|---|---|---|---|---|
| $\overline{OE}$ | D | C | B | A | Y |
| H | X | X | X | X | Z |

(1) H = High Voltage level, L = Low Voltage level, X = Don't care
(2) H = Driving high state, L = Driving low state, Z = High-impedance state

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SN74LV3T99 device offers flexible configuration for many design applications. This example describes basic control of a device using the AND gate configuration. The SN74LV3T99 is used to gate the signal from the MCU based on the status of the $V_{CC}$ voltage.

## 8.2 Typical Application

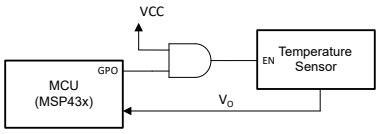



**Figure 8-1. Typical Application Schematic**


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### 8.2.1 Design Requirements

#### 8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV3T99 plus the maximum static supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through $V_{CC}$ listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV3T99 plus the maximum supply current, $I_{CC}$, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV3T99 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV3T99 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with $V_{OH}$ and $V_{OL}$. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the $V_{CC}$ pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

**CAUTION**

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

#### 8.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either $V_{CC}$ or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV3T99 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LV3T99 has no input signal transition rate requirements because it has Schmitt-Trigger inputs.

Another benefit to having Schmitt-Trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the Electrical Characteristics . This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-Trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than $V_{CC}$ or ground is plotted in the Typical Characteristics .

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Refer to the *Feature Description* for additional information regarding the inputs for this device.

#### 8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the $V_{OH}$ specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the $V_{OL}$ specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to $V_{CC}$ or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.


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### 8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from $V_{CC}$ to GND. The capacitor needs to be placed physically close to the device and electrically close to both the $V_{CC}$ and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV3T99 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than ($V_{CC}$ / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

### 8.2.3 Application Curves

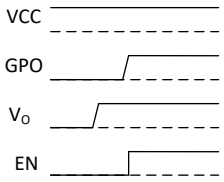



**Figure 8-2. Typical Application Timing Diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Recommended Operating Conditions*.

Verify that each $V_{CC}$ terminal has a good bypass capacitor to prevent power disturbance. For the SN74LV3T99, a 0.1µF bypass capacitor is recommended. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel.

## 8.4 Layout

### *8.4.1 Layout Guidelines*

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - Parallel traces must be separated by at least 3x dielectric thickness
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer each signal that must branch separately

### *8.4.2 Layout Example*

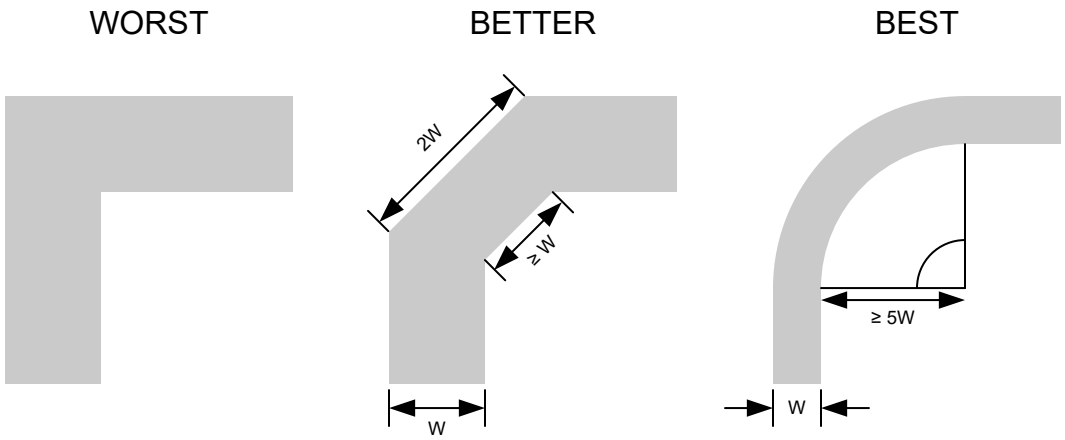



**Figure 8-3. Example Trace Corners for Improved Signal Integrity**


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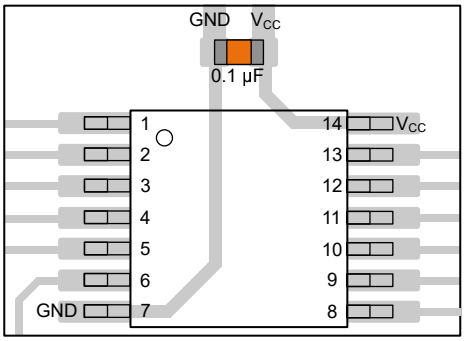



**Figure 8-4. Example Bypass Capacitor Placement for TSSOP and Similar Packages**

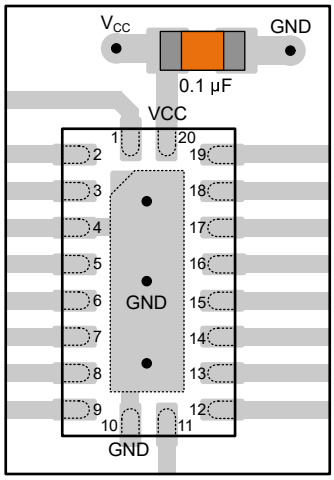



**Figure 8-5. Example Bypass Capacitor Placement for WQFN and Similar Packages**

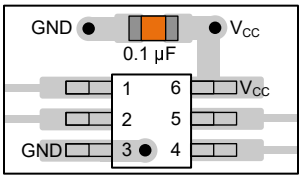



**Figure 8-6. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages**

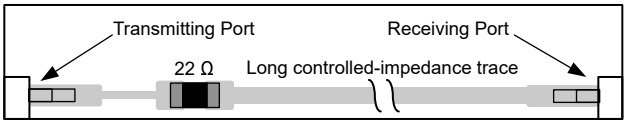



**Figure 8-7. Example Damping Resistor Placement for Improved Signal Integrity**

# 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 9.1 Documentation Support

### *9.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and $C_{pd}$ Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| November 2025 | * | Initial Release |


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LV3T99DGSR | Active | Production | VSSOP (DGS) \| 20 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | V3TG99 |
| SN74LV3T99PWR | Active | Production | TSSOP (PW) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC3G99 |
| SN74LV3T99RKSR | Active | Production | VQFN (RKS) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV3T99 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV3T99 :**

- Automotive : SN74LV3T99-Q1

NOTE: Qualified Version Definitions:

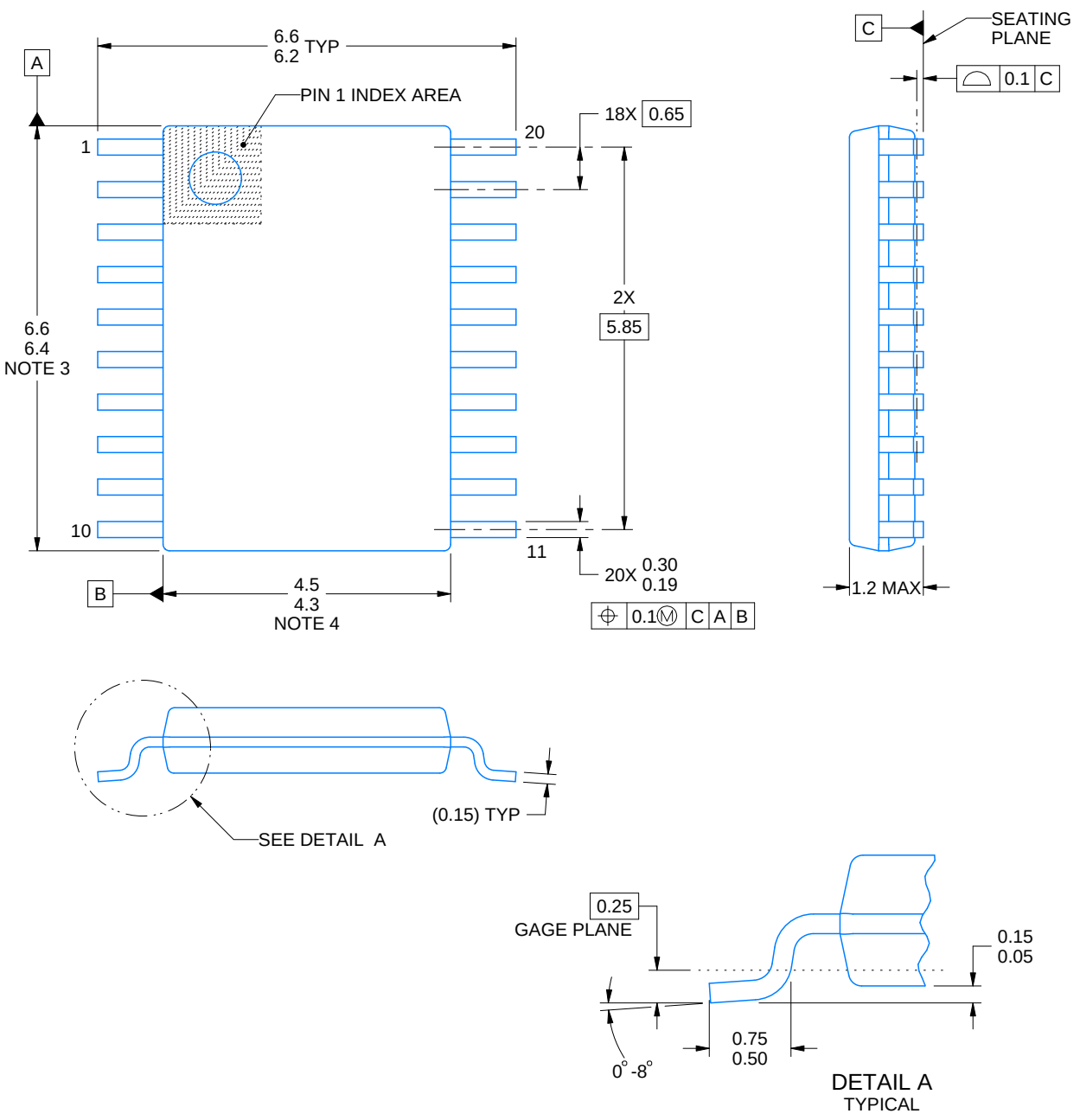
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

# PACKAGE OUTLINE

## PW0020A

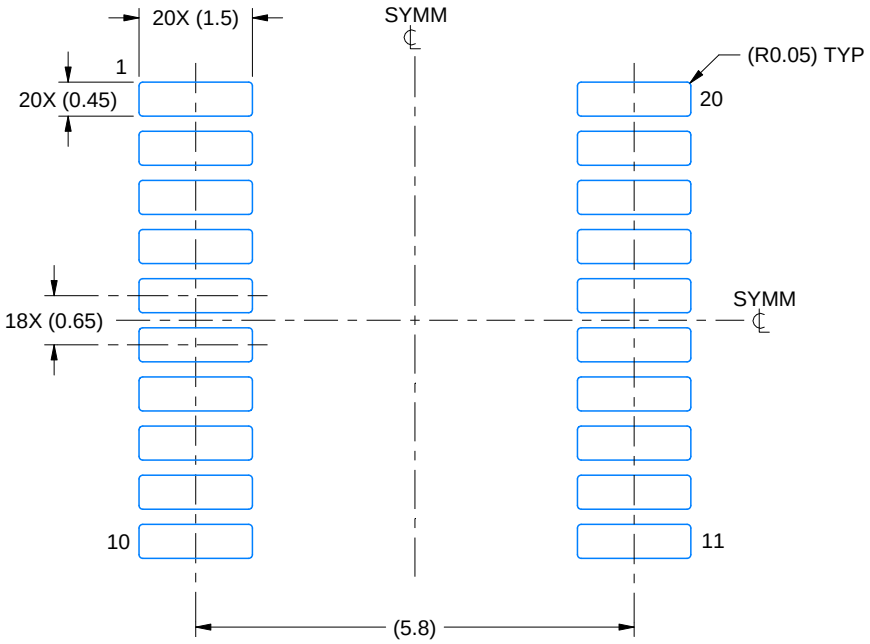
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

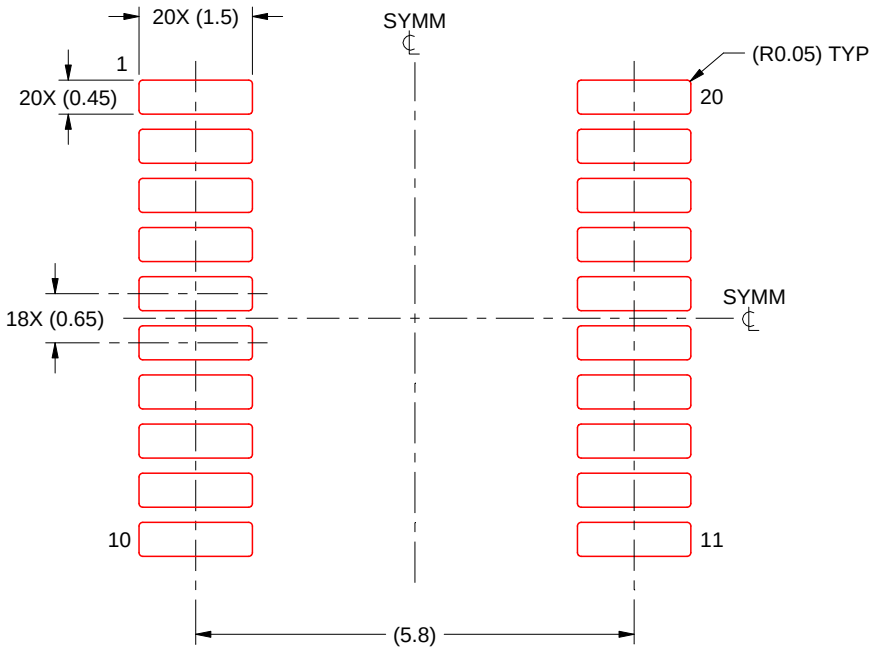



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

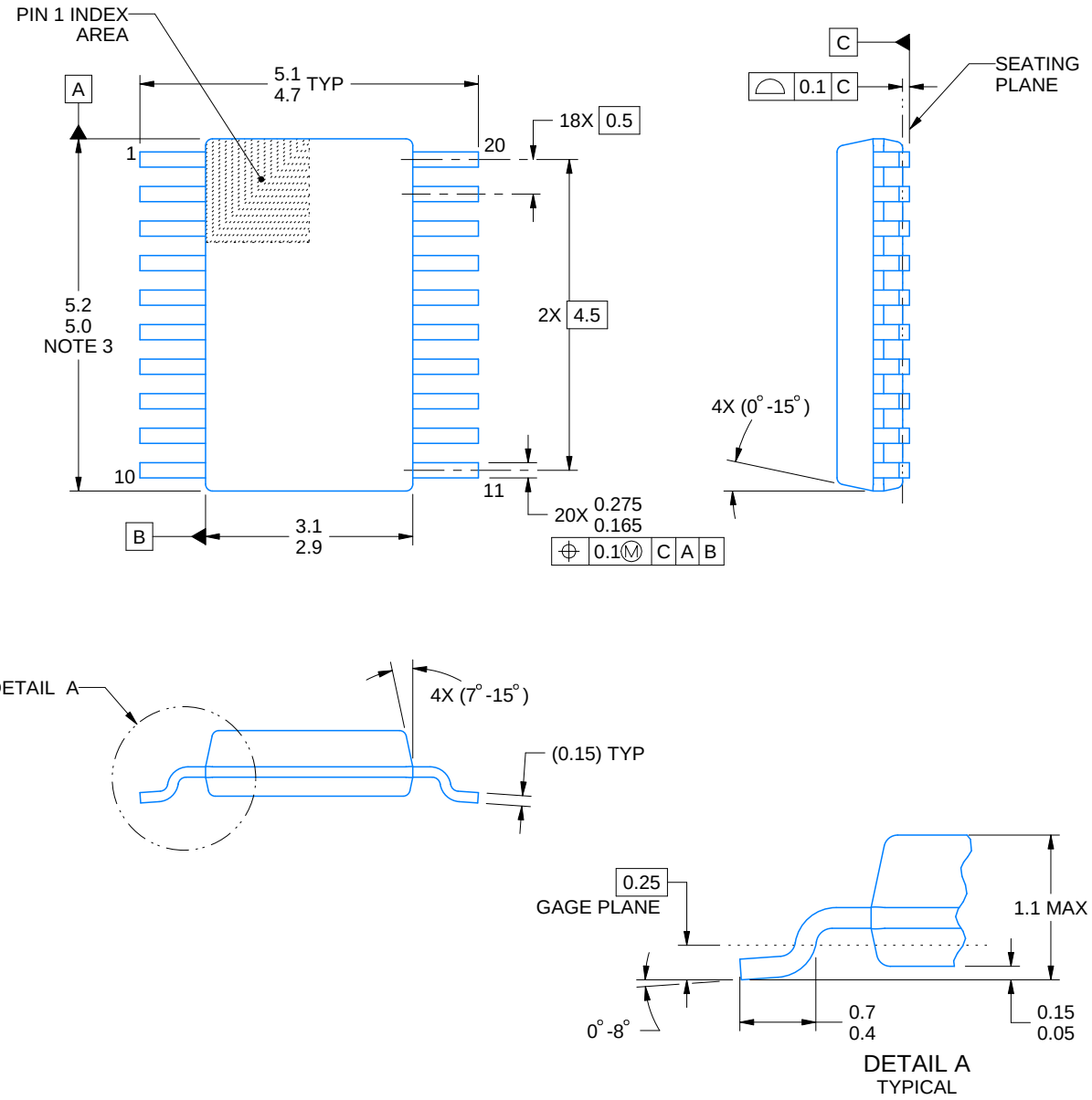
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DGS0020A

## VSSOP - 1.1 mm max height

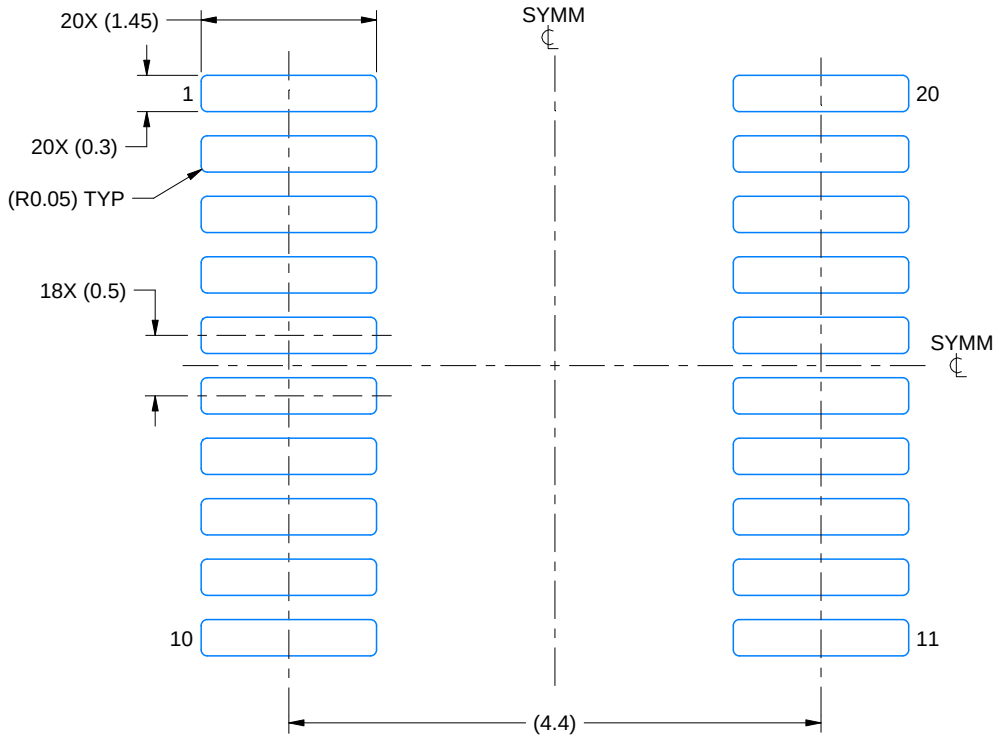
SMALL OUTLINE PACKAGE



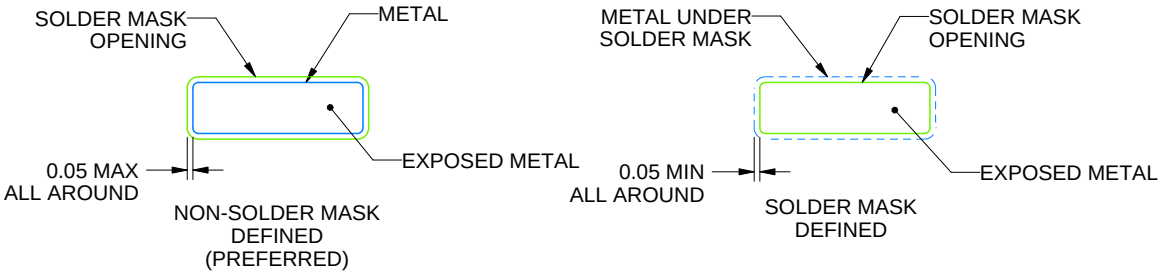

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
SCALE: 16X

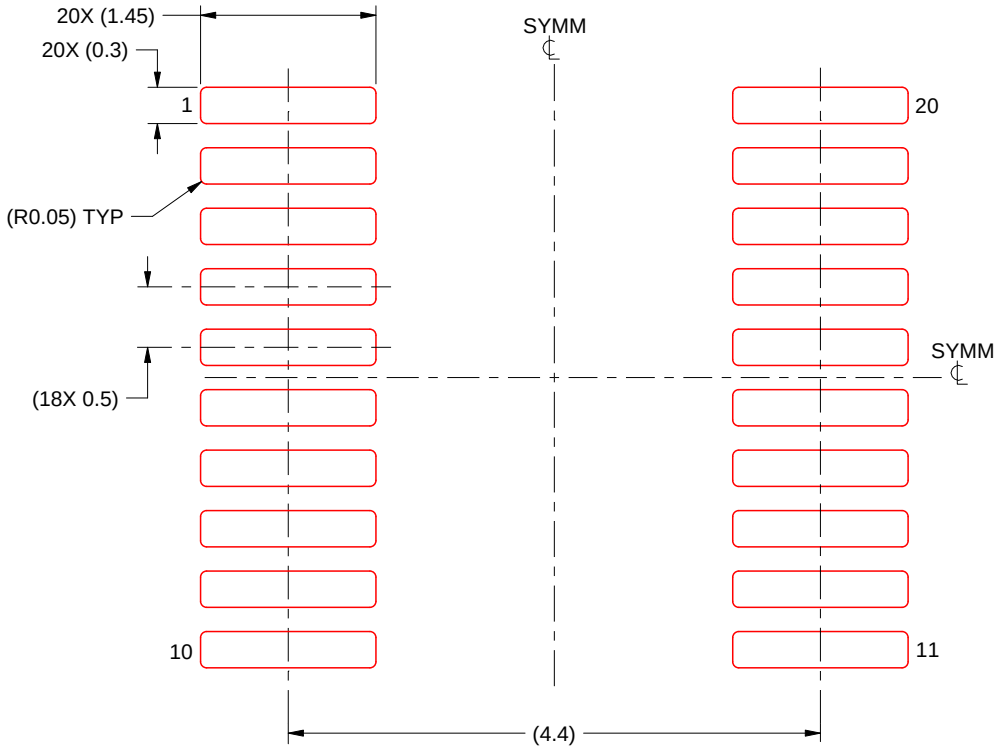



SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

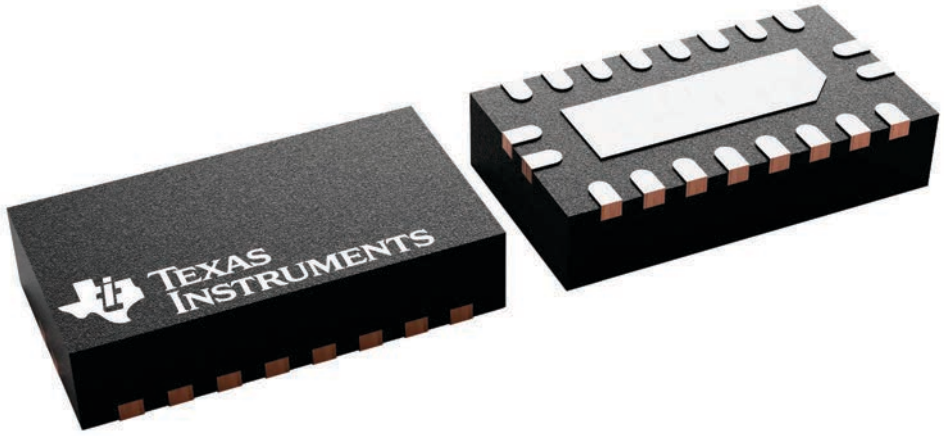
## RKS 20

## VQFN - 1 mm max height

**2.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

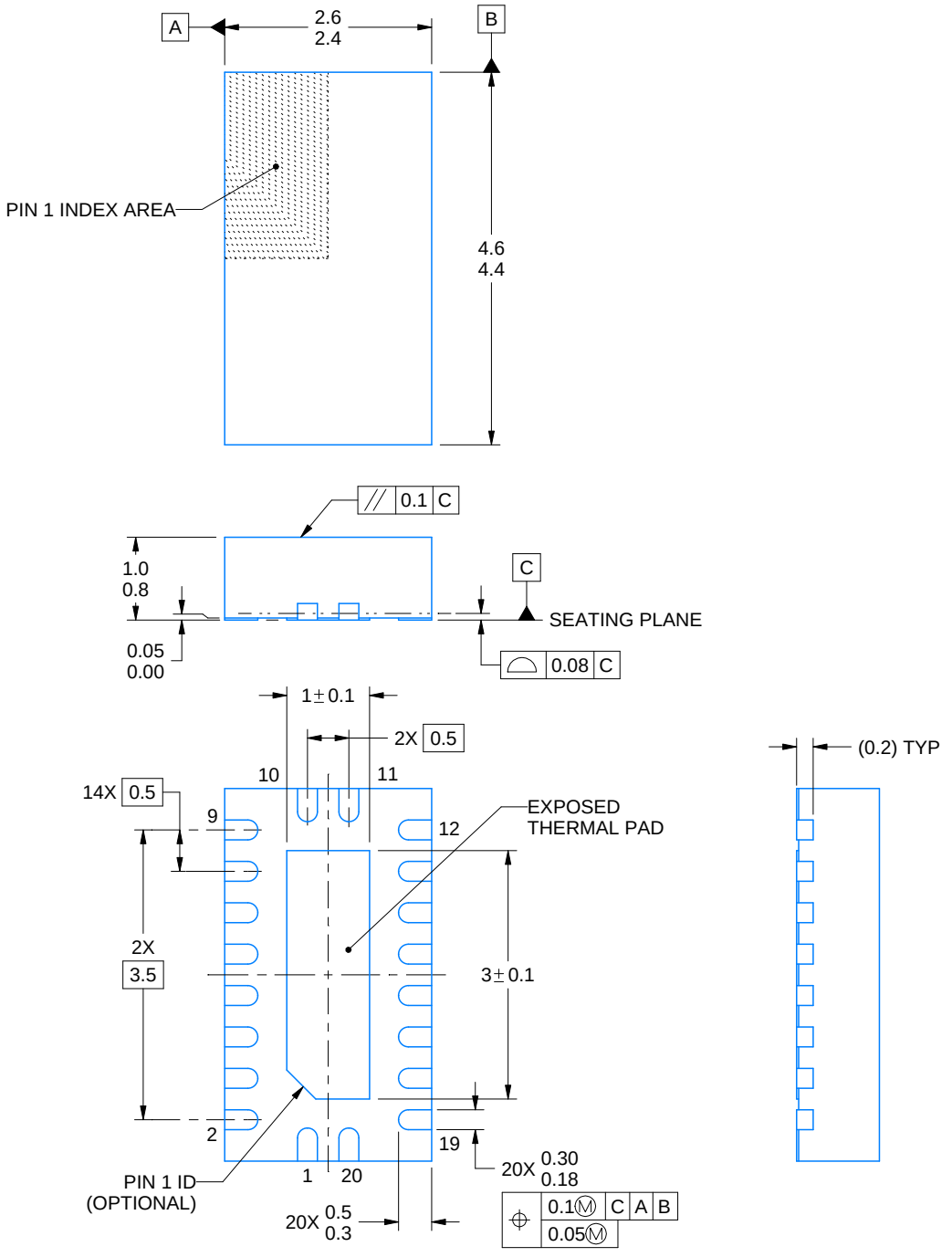


# PACKAGE OUTLINE

## RKS0020A

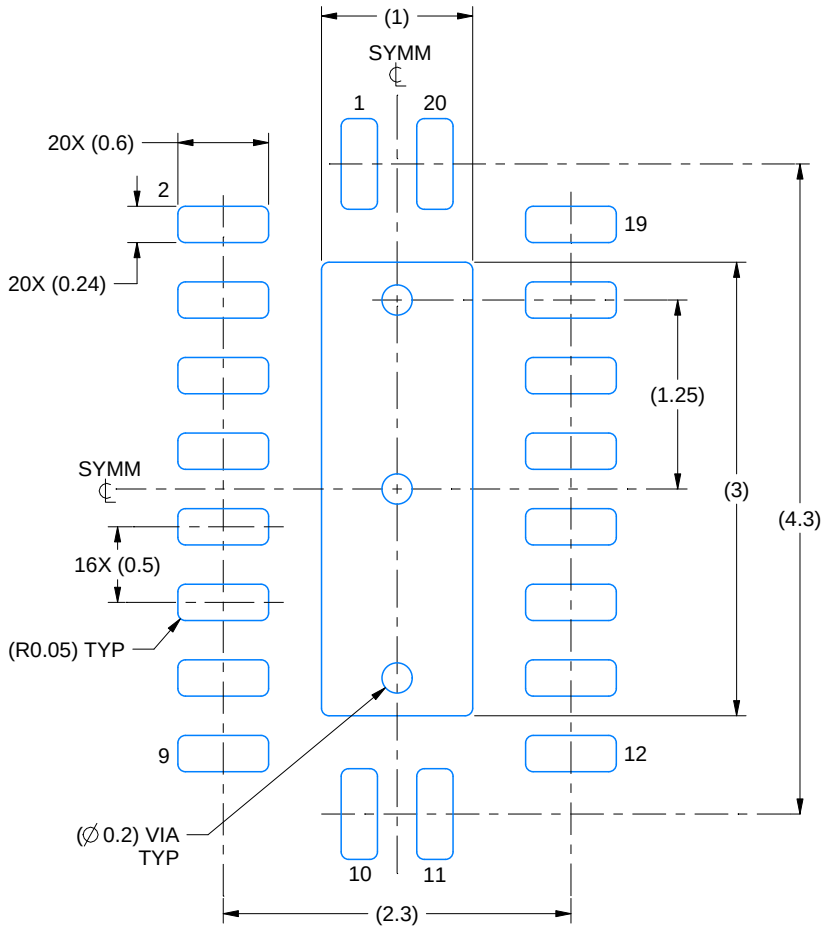
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

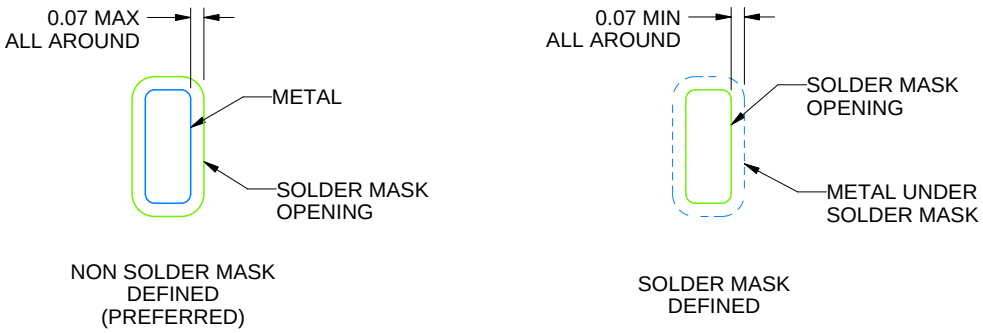



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:20X

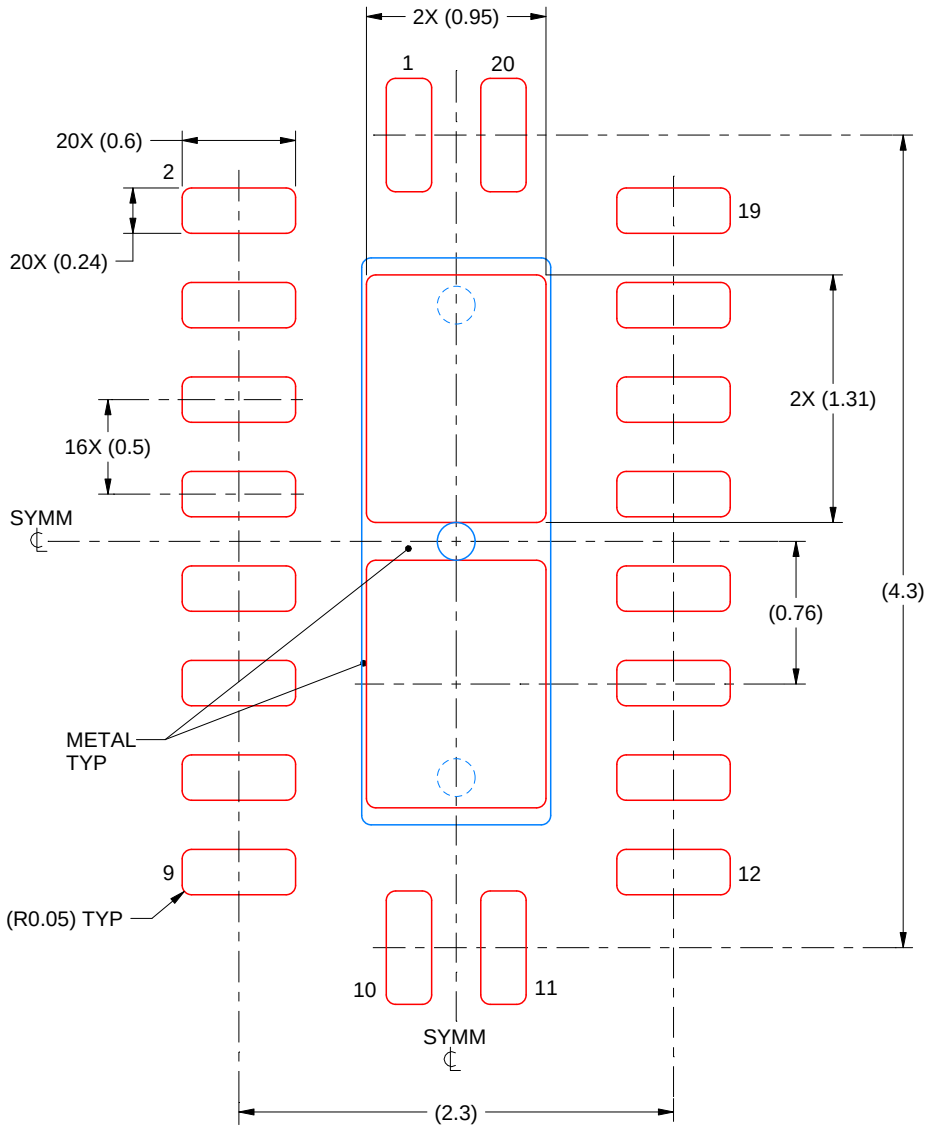



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025