SN74LV4040B-EP Enhanced Product, 12-Bit Asynchronous Binary Counters

1 Features

- 2V to 5.5V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce) <0.8V at V_{CC} = 3.3V, T_A = 25°C
- Typical V_{OHV} (Output VOH Undershoot) 2.3V at V_{CC} = 3.3V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- High On-Off Output-Voltage Ratio
- Low Crosstalk Between Switches
- Individual Switch Controls
- Extremely Low Input Current
- I_{off} Supports Partial-Power-Down Mode Operation
- Operating ambient temperature: -55°C to +125°C
- Supports defense and aerospace applications:
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Extended product life cycle
  - Product traceability

2 Applications

- Clock division
- Binary counting

3 Description

The SN74LV4040B-EP is a 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN74LV4040B-EP is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when powered down.

Package Information

PART NUMBER	PACKAGE [1]	PACKAGE SIZE [2]	BODY SIZE (NOM)[3]
SN74LV4040B-EP	PW (TSSOP, 16)	5mm x 6.4mm	5mm x 4.4mm

1. For more information, see Section 12
2. The package size (length × width) is a nominal value and includes pins, where applicable.
3. The body size (length × width) is a nominal value and does not include pins.

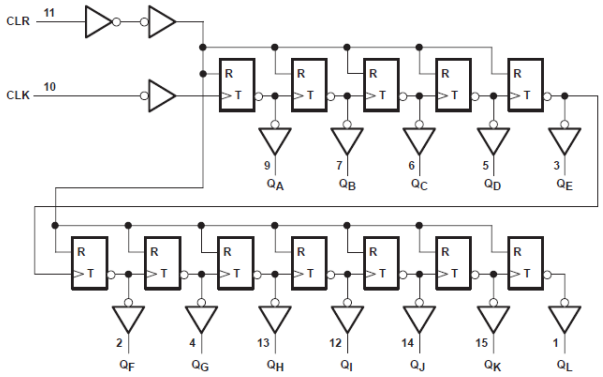


Figure 3-1. Simplified Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

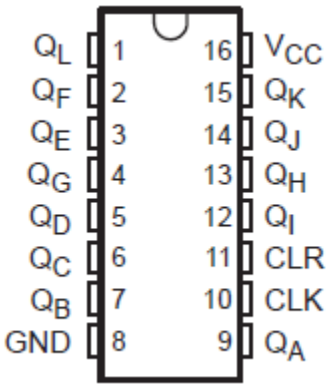


Figure 4-1. SN74LV4040B-EP PW Package (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Q_L	1	O	Q_L output
Q_F	2	O	Q_F output
Q_E	3	O	Q_E output
Q_G	4	O	Q_G output
Q_D	5	O	Q_D output
Q_C	6	O	Q_C output
Q_B	7	O	Q_B output
GND	8	-	Ground
Q_A	9	O	Q_A output
CLK	10	I	Clock, falling edge triggered
CLR	11	I	Clear, active high
Q_I	12	O	Q_I output
Q_H	13	O	Q_H output
Q_J	14	O	Q_J output
Q_K	15	O	Q_K output
V_{CC}	16	-	Positive supply

1. I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	7	V
V_O	Output voltage range		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current(2)	V_I < 0		−20	mA
I_{OK}	Output clamp current(2)	V_O < 0		−50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		-65	150	℃

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2V	1.5		V
		V_{CC} = 2.3V to 5.5V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2V		0.5	V
		V_{CC} = 2.3V to 5.5V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_O	Output current (high or low level)	V_{CC} = 2V		±50	μA
		V_{CC} = 2.3V to 2.7V		±2	mA
		V_{CC} = 3V to 3.6V		±6	
		V_{CC} = 4.5V to 5.5V		±12	
Δt/Δv	Input transition rise/fall time	V_{CC} = 2.3V to 2.7V		200	ns
		V_{CC} = 3V to 3.6V		100	
		V_{CC} = 4.5V to 5.5V		20	
T_A	Operating free-air temperature		-55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to *Implications of Slow or Floating CMOS Inputs*

5.4 Thermal Information

THERMAL METRIC#none#		PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	81.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

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5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = −50µA	2V to 5.5V	V_{CC} − 0.1			V
	I_{OH} = −2mA	2.3V	2			
	I_{OH} = −6mA	3V	2.48			
	I_{OH} = −12mA	4.5V	3.8			
V_{OL}	I_{OL} = 50µA	2V to 5.5V			0.1	V
	I_{OL} = 2mA	2.3V			0.4	
	I_{OL} = 6mA	3V			0.44	
	I_{OL} = 12mA	4.5V			0.55	
I_I	V_I = 5.5V or GND	0 to 5.5V			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5V			20	µA
I_{off}	V_I or V_O = 0 to 5.5V	0			5	µA
C_i	V_I = V_{CC} or GND	3.3V		1.9		pF

5.6 Timing Requirements, V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	7		ns
		CLR high	6.5		
t_{su}	Setup time	CLR inactive before CLK↓	6.5		

5.7 Timing Requirements, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	5		ns
		CLR high	5		
t_{su}	Setup time	CLR inactive before CLK↓	5		

5.8 Timing Requirements, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	CLK high or low	5		ns
		CLR high	5		
t_{su}	Setup time	CLR inactive before CLK↓	5		

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5.9 Switching Characteristics, V_{CC} = 2.5V ± 0.2V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
f_{max}			C_L = 50pF	35	95		MHz
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50pF	1	10.5	28	ns
t_{PHL}				1	10.5	28	
t_{PHL}	CLR	Any Q	C_L = 50pF	1	11.7	28	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50pF		1.7	11.1	

5.10 Switching Characteristics, V_{CC} = 3.3V ± 0.3V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
f_{max}			C_L = 50pF	50	130		MHz
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50pF	1	7.5	17.5	ns
t_{PHL}				1	7.5	17.5	ns
t_{PHL}	CLR	Any Q	C_L = 50pF	1	9	18.5	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50pF		1.2	5	ns

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5.11 Switching Characteristics, V_{CC} = 5V ± 0.5V

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	MIN	TYP	MAX	UNIT
f_{max}			C_L = 50pF	80	185		MHz
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50pF		5.3	10.5	ns
t_{PHL}					5.3	10.5	ns
t_{PHL}	CLR	Any Q	C_L = 50pF		6.8	12	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50pF		0.8	3.5	ns

5.12 Noise Characteristics

V_{CC} = 3.3V, C_L = 50pF, T_A = 25°C

PARAMETER[1]		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		− 0.5	− 0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics for surface-mount packages only.

5.13 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50pF,	f = 10MHz	3.3V	11.9	pF
				5V	13.1	

6 Typical Characteristics

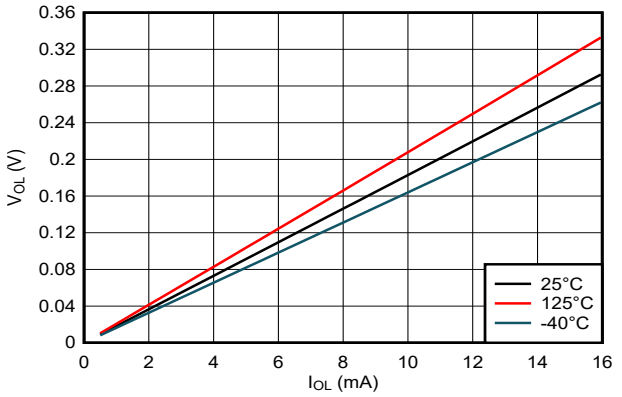


Figure 6-1. Output Voltage vs Current in LOW State; 5V Supply

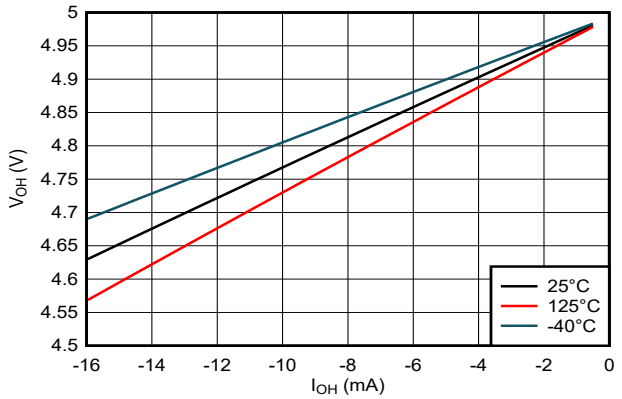


Figure 6-2. Output Voltage vs Current in HIGH State; 5V Supply

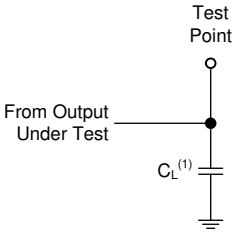
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7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured individually with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs

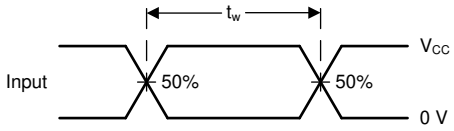


Figure 7-2. Voltage Waveforms, Pulse Duration

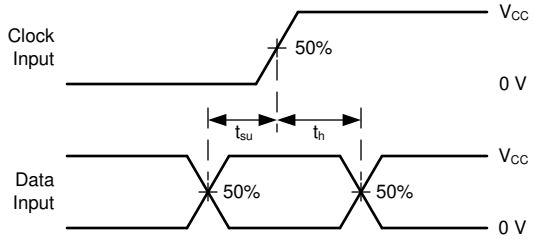
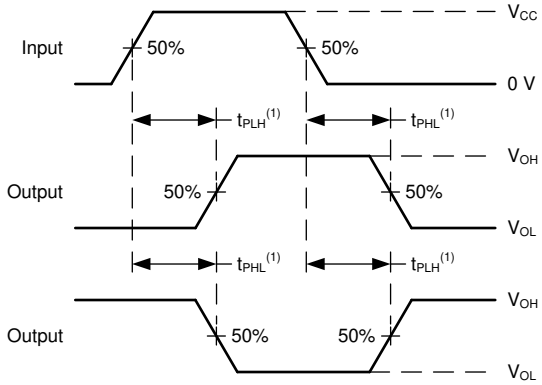
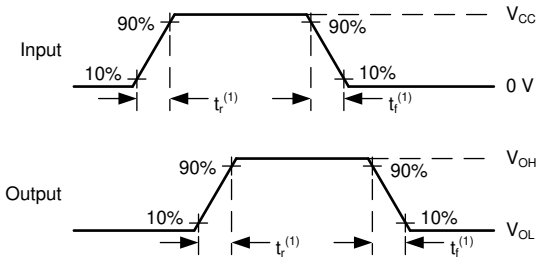


Figure 7-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Figure 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 7-5. Voltage Waveforms, Input and Output Transition Times

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8 Detailed Description

8.1 Overview

The SN74LV4040B-EP is a 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN74LV4040B-EP is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when powered down.

8.2 Functional Block Diagram

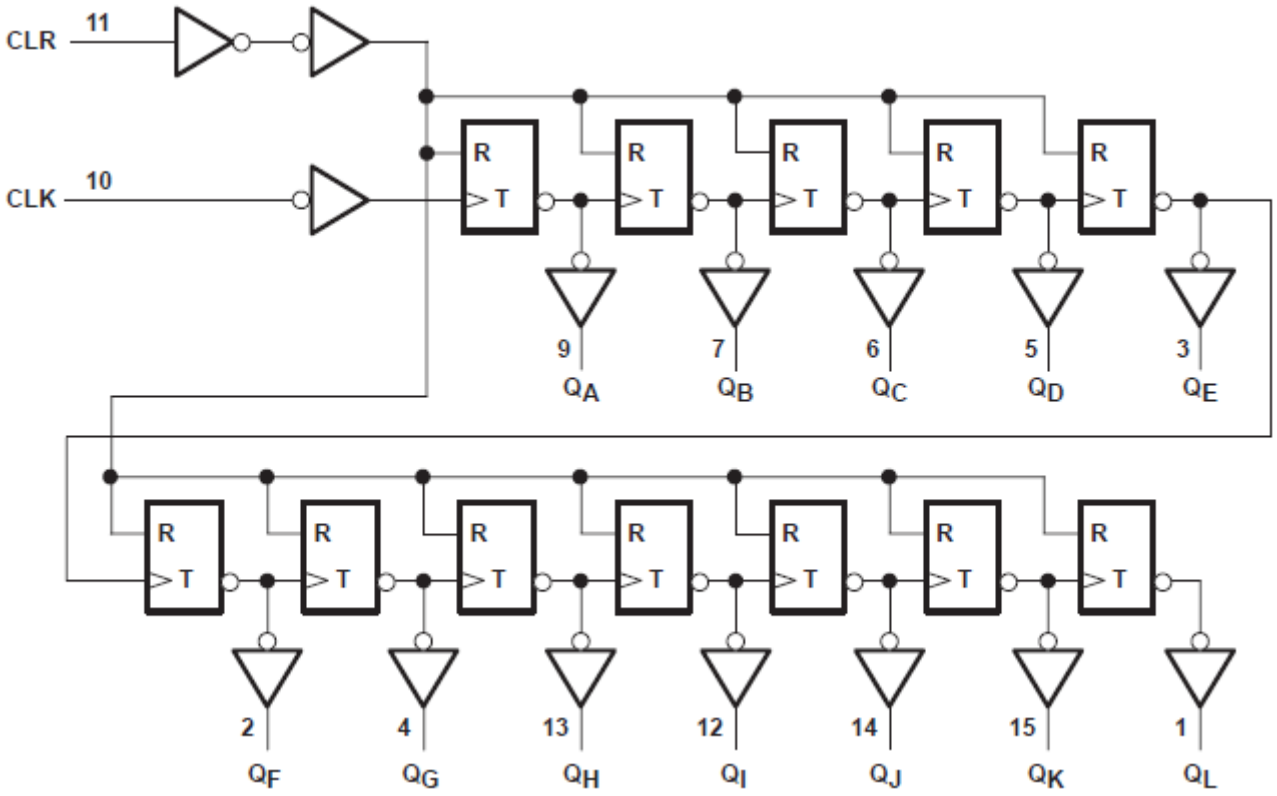


Figure 8-1. Logic Diagram (Positive Logic)

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8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

8.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10kΩ resistor, however, is recommended and will typically meet all requirements.

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74LV4040B-EP.

Table 8-1. Function Table

INPUTS(1)		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next count
X	H	All outputs L

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV4040B-EP can be used to provide a binary count or frequency division for up to 12 stages or a factor of 4096. The figure in the *Application Curve* section shows the binary states and outputs by clock inputs. Using these factors a frequency divider can be implemented as shown under *Typical Application*.

9.2 Typical Application

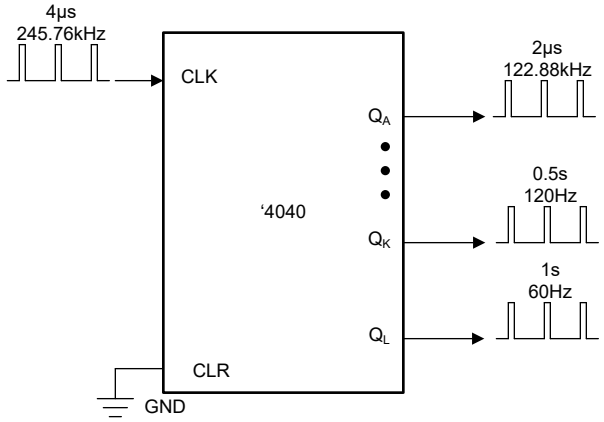


Figure 9-1. Typical Application Block Diagram

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9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device's electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV4040B-EP plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV4040B-EP plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LV4040B-EP can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LV4040B-EP can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

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9.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV4040B-EP (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LV4040B-EP has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Electrical Characteristics* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

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9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is ≤ 50pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV4040B-EP to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$)Ω. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the *CMOS Power Consumption and Cpd Calculation* application note.

9.2.3 Application Curves

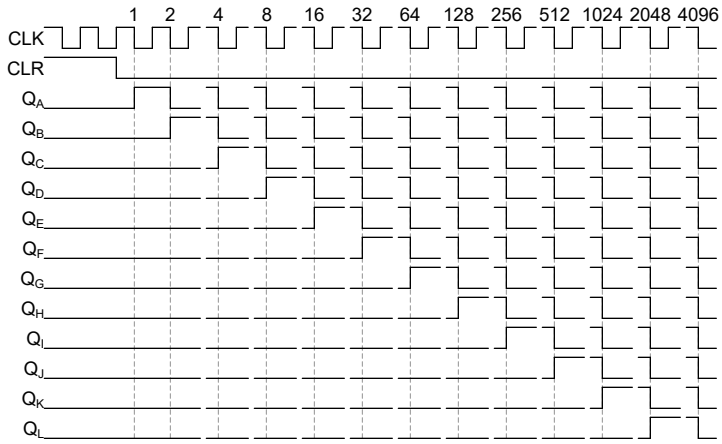


Figure 9-2. Logic Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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9.4.2 Layout Example

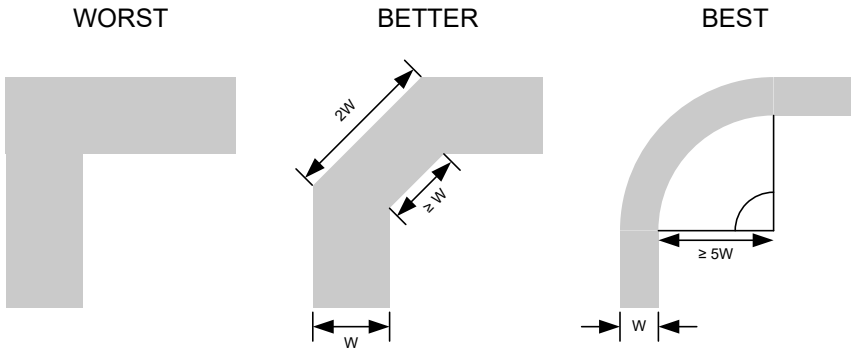


Figure 9-3. Example trace corners for improved signal integrity

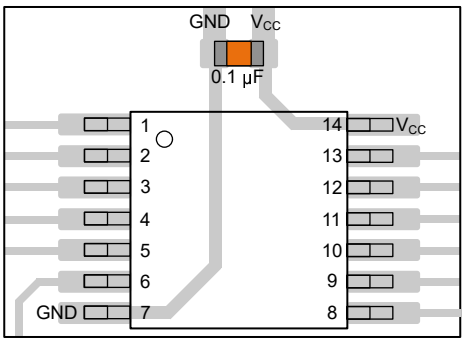


Figure 9-4. Example bypass capacitor placement for TSSOP and similar packages

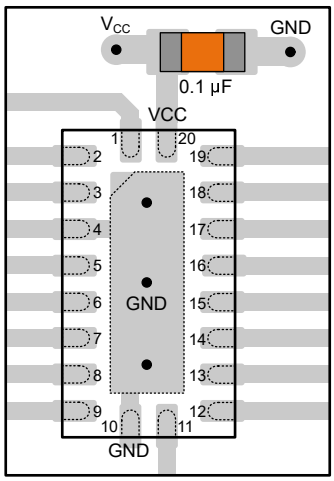


Figure 9-5. Example bypass capacitor placement for WQFN and similar packages

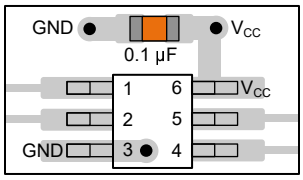


Figure 9-6. Example bypass capacitor placement for SOT, SC70 and similar packages

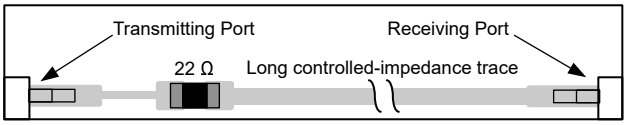


Figure 9-7. Example damping resistor placement for improved signal integrity

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2024) to Revision A (August 2025)	Page
• Updated Pin Configuration and Functions table	3

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV4040BMPWREP	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LW040B
SN74LV4040BMPWREP.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	See SN74LV4040BMPWREP	LW040B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

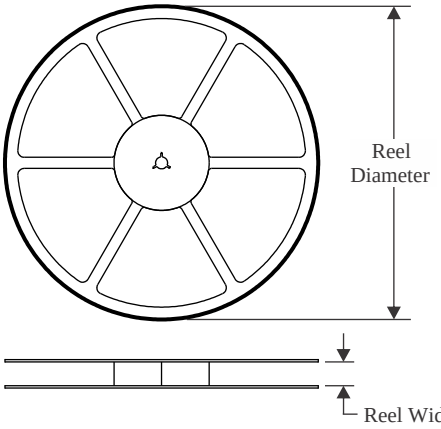
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

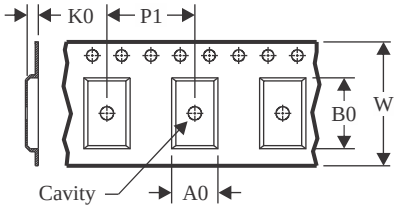
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

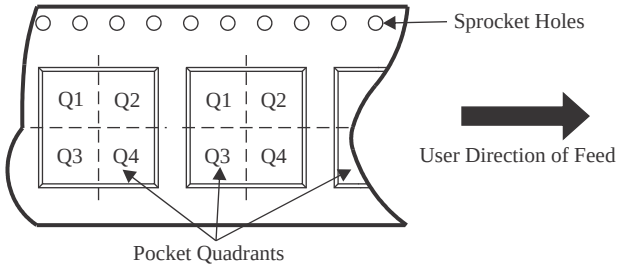


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

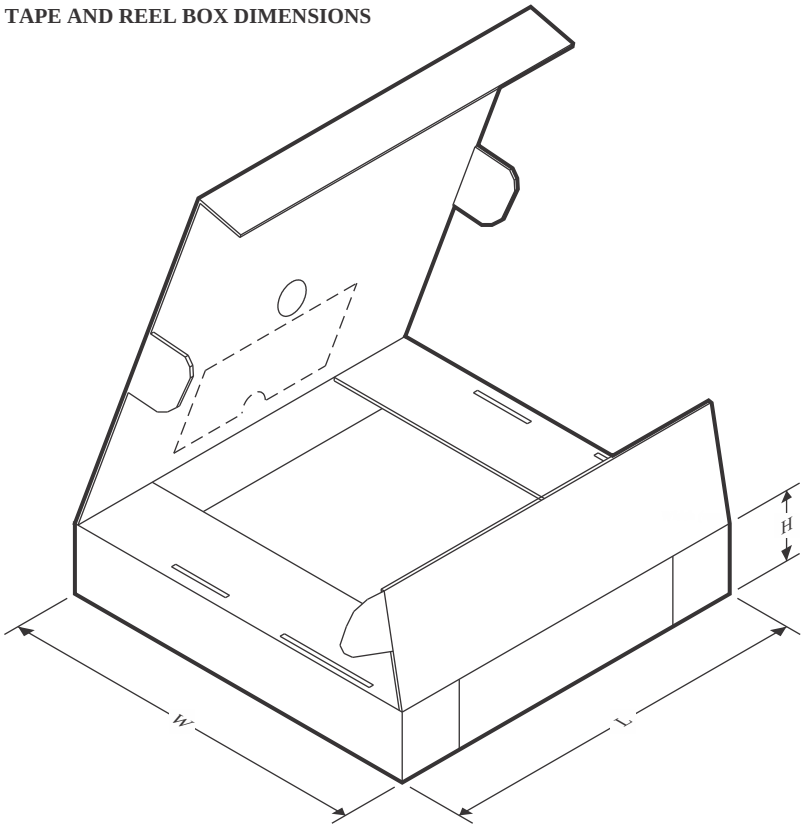
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV4040BMPWREP	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

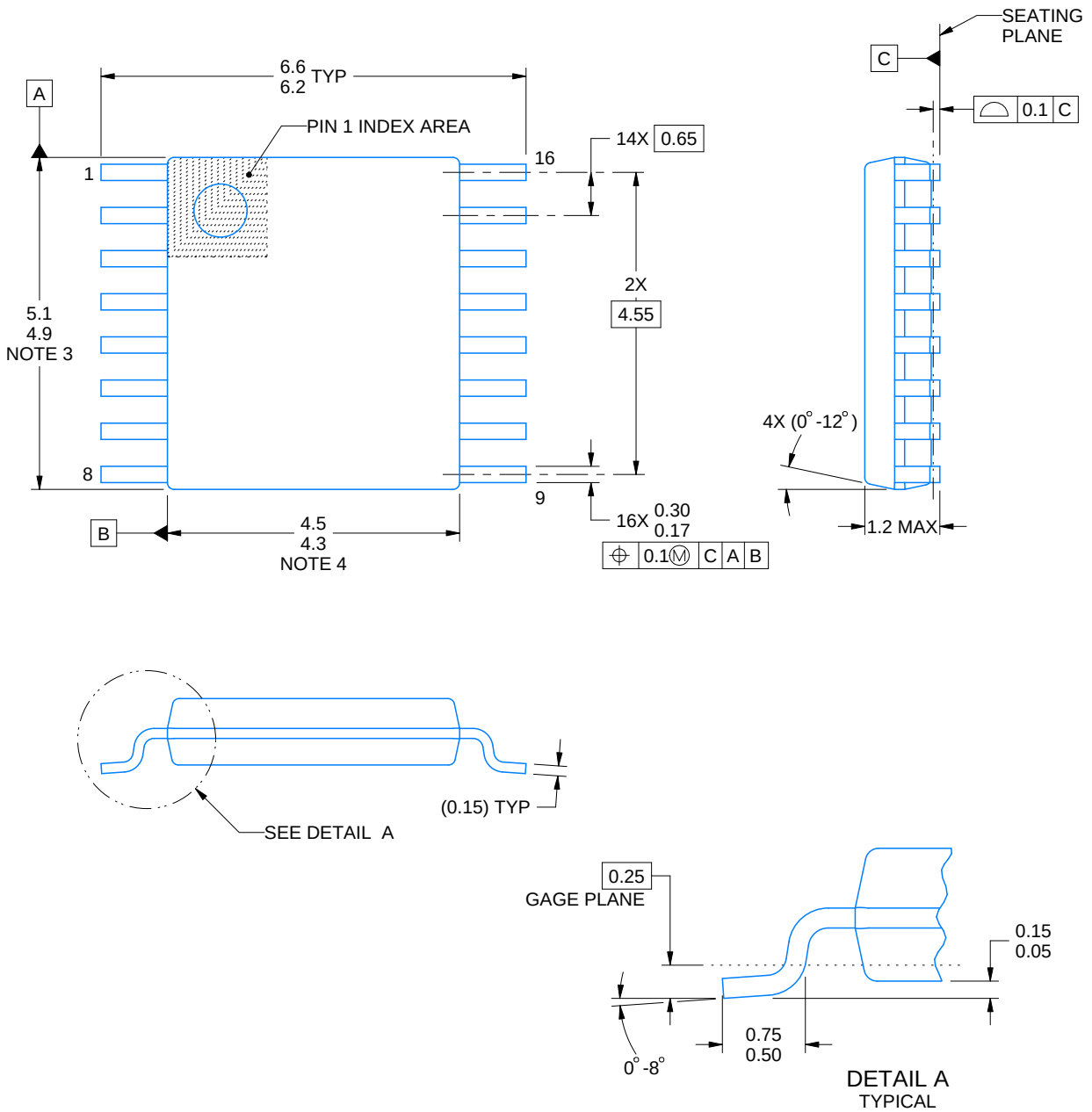
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV4040BMPWREP	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

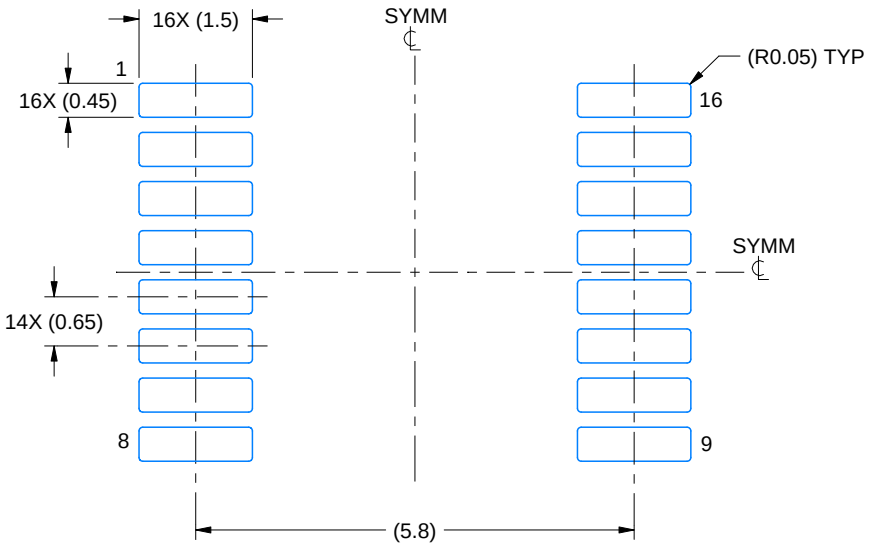
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

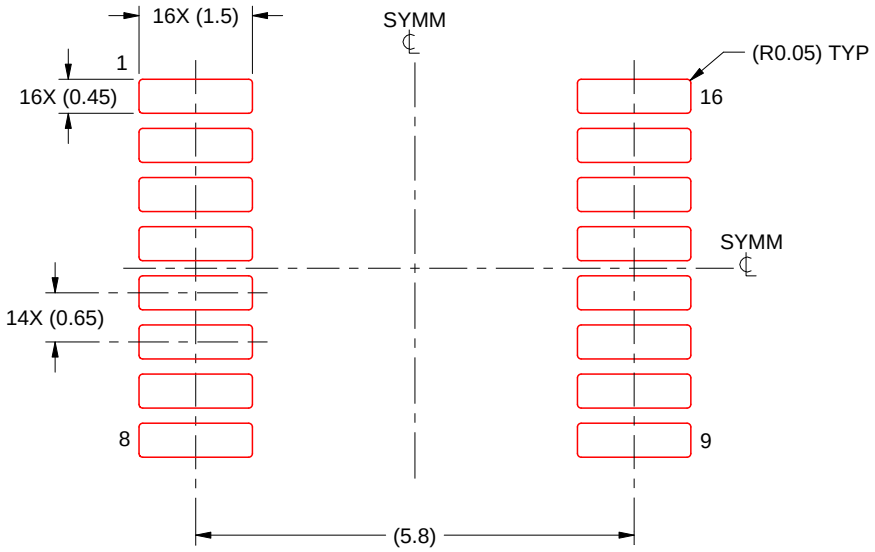


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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