

SN74LV540A Octal Buffers/Drivers with 3-State Outputs

1 Features

- V_{CC} operation of 2 V to 5.5 V
- Max t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Voltage operation on all ports
- I_{off} supports Partial-Power-Down Mode operation
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- Tests and Measurements
- Industrial Transports
- Patient Monitoring
- Wireless Infrastructure
- Network Switches
- Automotive Infotainment

3 Description

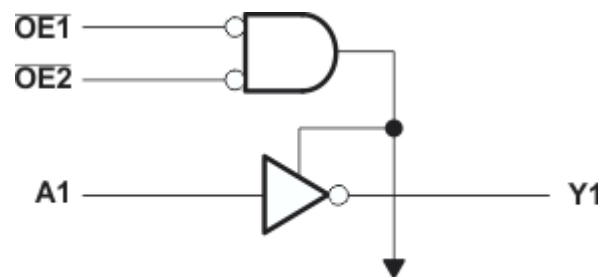
The SN74LV540A device is an octal buffer/driver designed for 2 V to 5.5 V V_{CC} operation.

This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74LV540A	RGY (VQFN, 20)	4.50 mm x 3.50 mm
	DB (SSOP, 20)	7.50 mm x 5.30 mm
	PW (TSSOP, 20)	6.50 mm x 4.40 mm
	DGV (TVSOP, 20)	5.00 mm x 4.40 mm
	DW (SOIC, 20)	12.80 x 7.50 mm
	NS (SOP, 20)	12.6 mm x 5.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



To Seven Other Channels

Figure 3-1. Simplified Schematic



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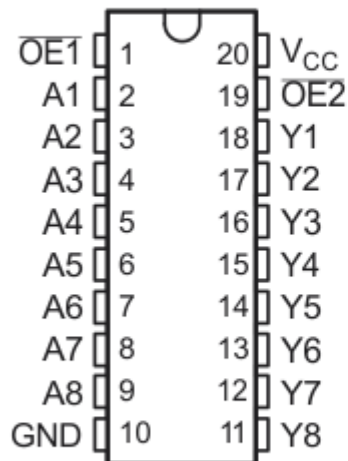
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4 Revision History

Changes from Revision I (December 2014) to Revision J (March 2023)	Page
• Updated structural layout of document to current standard, updated <i>Features</i> section, and added NS package to <i>Package Information</i> table.....	1
• Added $\pm$ to values in <i>ESD Ratings</i> section.....	4
• Updated thermal values for PW package from $R\theta_{JA} = 102.8$ to 128.2 , $R\theta_{JC}(\text{top}) = 36.8$ to 70.5 , $R\theta_{JB} = 53.8$ to 79.3 , $\Psi_{JT} = 2.5$ to 23.4 , $\Psi_{JB} = 53.3$ to 78.9 , all values in $^{\circ}\text{C/W}$	5
Changes from Revision H (April 2005) to Revision I (December 2014)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table.....	1
• Changed MAX operating temperature to 125°C in <i>Recommended Operating Conditions</i> table.	5

5 Pin Configuration and Functions

**SN74LV540A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)**



**SN74LV540A . . . RGY PACKAGE
(TOP VIEW)**

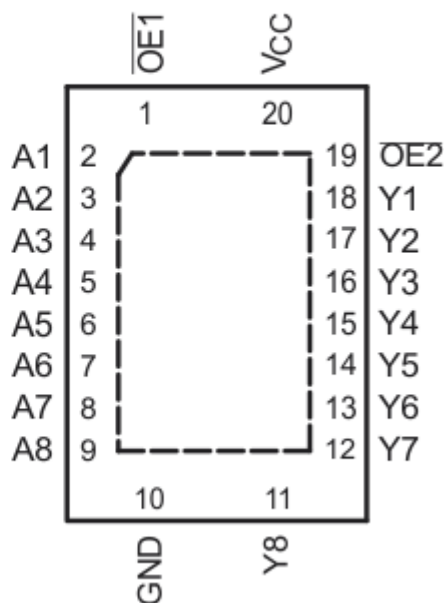


Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground Pin
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	$\overline{OE2}$	I	Output Enable 2
20	V _{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V _O	Output voltage range applied in the high or low state ⁽²⁾ (3)	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–20 mA
I _{OK}	Output clamp current	V _O < 0		–50 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35 mA
	Continuous current through V _{CC} or GND			±70 mA
T _{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±2000
		Machine Model (MM)	±200

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LV540A		UNIT
			MIN	MAX	
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2	
		V _{CC} = 3 V to 3.6 V		–8	mA
		V _{CC} = 4.5 V to 5.5 V		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 V to 2.7 V		2	
		V _{CC} = 3 V to 3.6 V		8	mA
		V _{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	ns/V
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV540A						UNIT
		DB	DGV	DW	NS	PW	RGY	
		20 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	96.0	116.1	79.8	77.1	128.2	35.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	57.7	31.3	45.8	43.6	70.5	43.3	
R _{θJB}	Junction-to-board thermal resistance	51.2	57.6	47.4	44.6	79.3	12.9	
Ψ _{JT}	Junction-to-top characterization parameter	19.4	1.0	18.5	17.2	23.4	0.9	
Ψ _{JB}	Junction-to-board characterization parameter	50.8	56.9	47.0	44.2	78.9	12.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	7.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			−40°C to 85°C		−40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = −50 μA	2 V to 5.5 V	V _{CC} − 0.1			V _{CC} − 0.1		V _{CC} − 0.1		V
	I _{OH} = −2 mA	2.3 V	2			2		2		
	I _{OH} = −8 mA	3 V	2.48			2.48		2.48		
	I _{OH} = −16 mA	4.5 V	3.8			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V	0.1			0.1		0.1		V
	I _{OL} = 2 mA	2.3 V	0.4			0.4		0.4		
	I _{OL} = 8 mA	3 V	0.44			0.44		0.44		
	I _{OL} = 16 mA	4.5 V	0.55			0.55		0.55		
I _I	V _I = 5.5 V or GND	0 to 5.5 V	±1			±1		±1		μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V	±5			±5		±5		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V	20			20		20		μA
I _{off}	V _I or V _O = 0 to 5.5 V	0	5			5		5		μA
C _i	V _I = V _{CC} or GND	3.3 V	2.5							pF
		5 V	2.5							

6.6 Switching Characteristics, $V_{CC} = 2.5\ \text{V} \pm 0.2\ \text{V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\ \text{pF}$	5.6 ⁽¹⁾	12 ⁽¹⁾		1	14.5	1	16	ns
t_{en}	$\overline{OE}$	Y		7.8 ⁽¹⁾	17.4 ⁽¹⁾		1	21	1	22.5	
t_{dis}	$\overline{OE}$	Y		5.7 ⁽¹⁾	16 ⁽¹⁾		1	19	1	20	
t_{pd}	A	Y	$C_L = 50\ \text{pF}$	7.9	16.8		1	18.5	1	20	ns
t_{en}	$\overline{OE}$	Y		10.1	22.2		1	25.5	1	27	
t_{dis}	$\overline{OE}$	Y		8.1	22.3		1	25.5	1	26.5	
$t_{sk(o)}$					2			2		3	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, $V_{CC} = 3.3\ \text{V} \pm 0.3\ \text{V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\ \text{pF}$	4.1 ⁽¹⁾	7 ⁽¹⁾		1	8.5	1	9.5	ns
t_{en}	$\overline{OE}$	Y		5.6 ⁽¹⁾	10.5 ⁽¹⁾		1	12.5	1	14	
t_{dis}	$\overline{OE}$	Y		4.2 ⁽¹⁾	10.5 ⁽¹⁾		1	12.5	1	13.5	
t_{pd}	A	Y	$C_L = 50\ \text{pF}$	5.8	10.5		1	12	1	13	ns
t_{en}	$\overline{OE}$	Y		7.3	14		1	16	1	17.5	
t_{dis}	$\overline{OE}$	Y		5.8	15.4		1	17.5	1	18.5	
$t_{sk(o)}$					1.5			1.5		2	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	3 ⁽¹⁾	5 ⁽¹⁾		1	6	1	7	ns
t_{en}	$\overline{OE}$	Y		4.1 ⁽¹⁾	7.2 ⁽¹⁾		1	8.5	1		
t_{dis}	$\overline{OE}$	Y		2.9 ⁽¹⁾	7 ⁽¹⁾		1	8	1	9	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.2	7		1	8	1	9	ns
t_{en}	$\overline{OE}$	Y		5.3	9.2		1	10.5	1	11.5	
t_{dis}	$\overline{OE}$	Y		3.5	8.8		1	10	1	11	
$t_{sk(o)}$					1			1		1.5	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER ⁽¹⁾		SN74LV540A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.3			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.97		V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	10	pF
		Outputs enabled		5 V	11	

6.11 Typical Characteristics

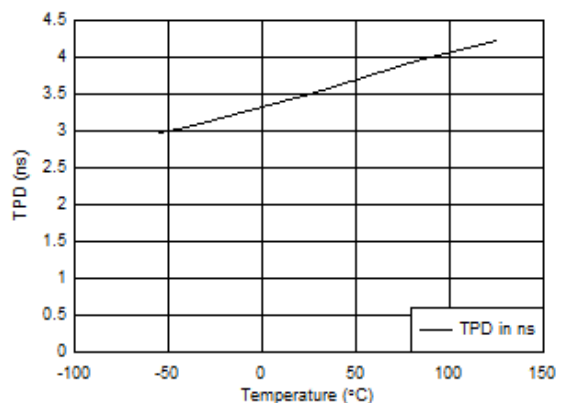


Figure 6-1. TPD vs Temperature

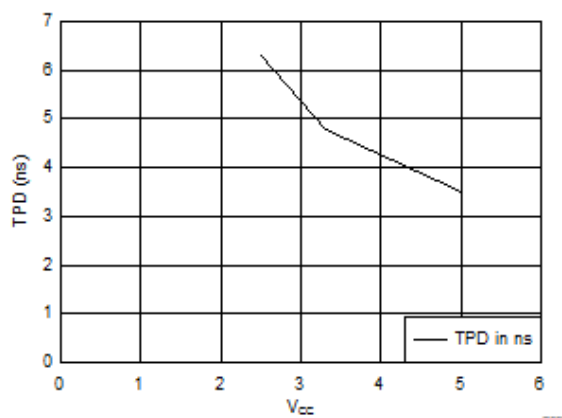
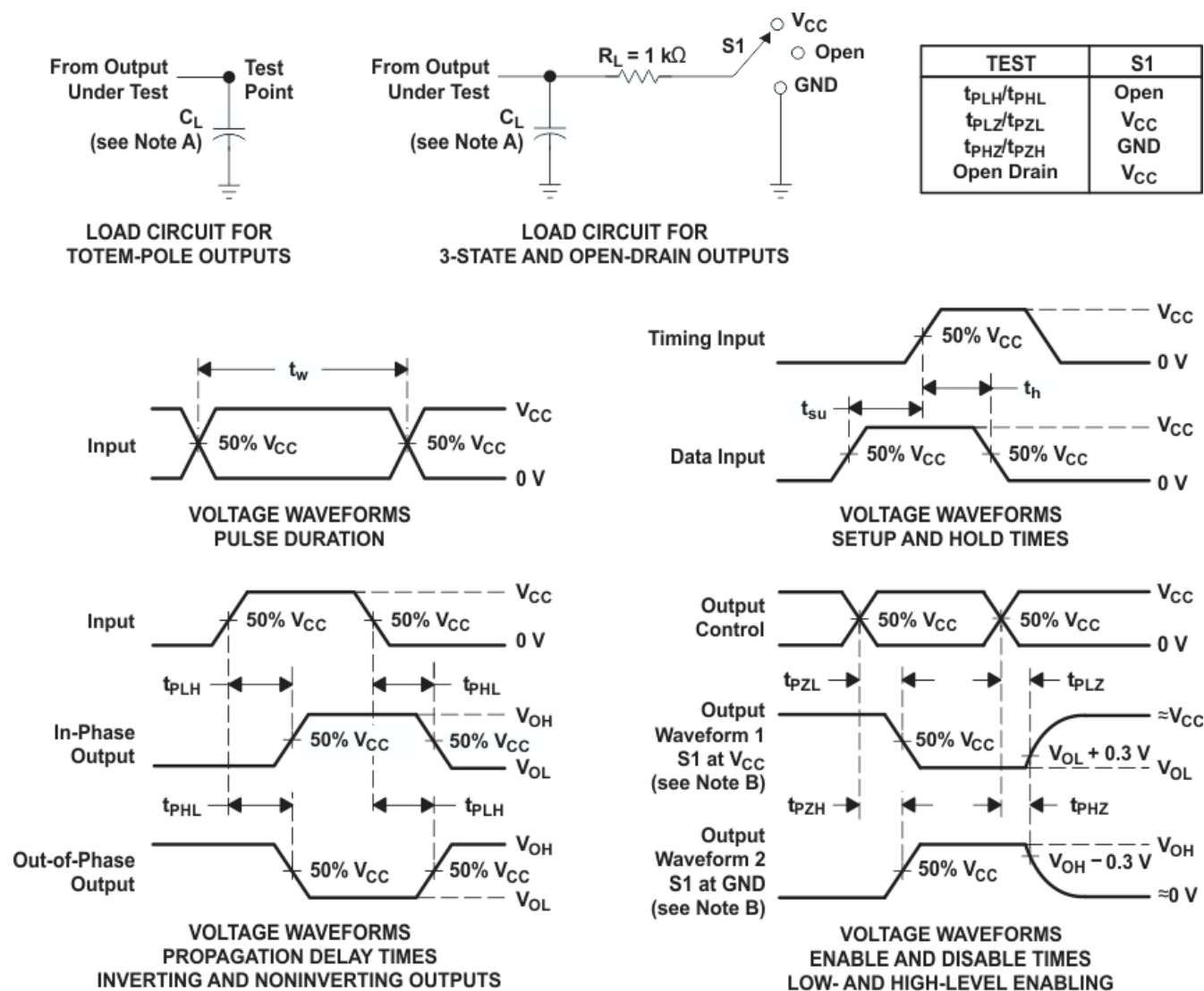


Figure 6-2. TPD vs V_{CC} at 25°C

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.

D. The outputs are measured one at a time, with one input transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PHL} and t_{PLH} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

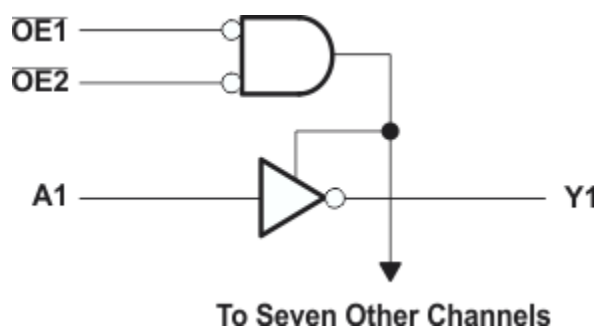
The SN74LV540A device is an octal buffer/driver designed for 2 V to 5.5 V V_{CC} operation.

This device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that, if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down-voltage translation
 - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

8.4 Device Functional Modes

**Table 8-1. Function Table
(Each Buffer/Driver)**

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV540A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC} . This feature makes it ideal for translating down to the V_{CC} level. [Figure 9-2](#) shows the reduction in ringing compared to higher drive parts such as AC.

9.2 Typical Application

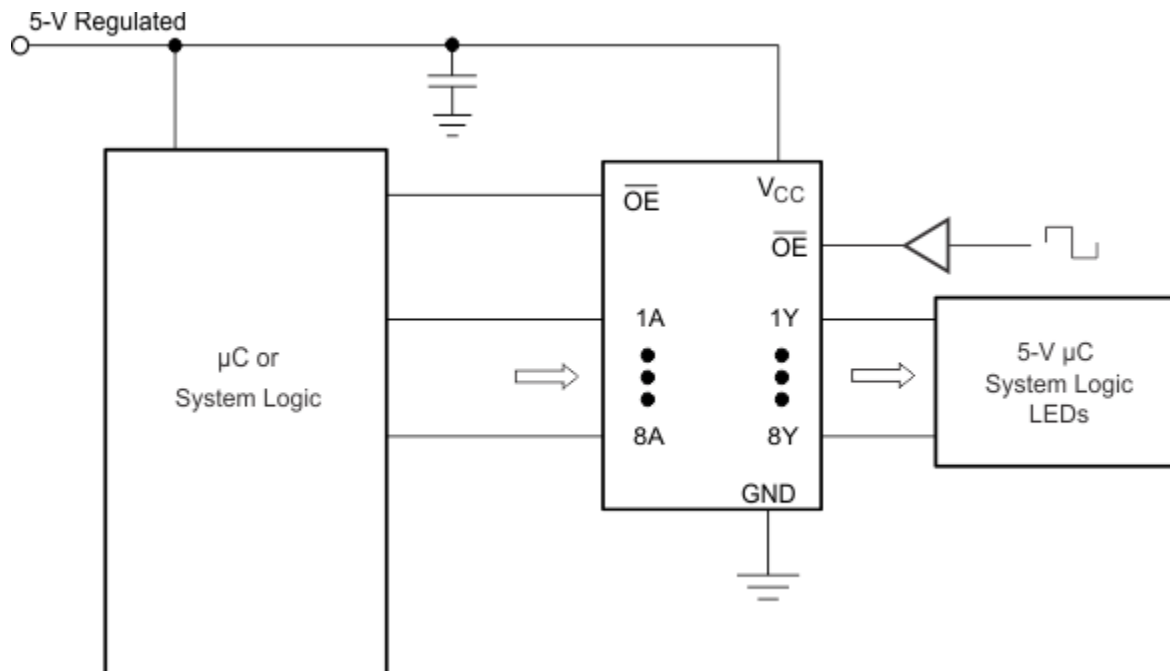


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended Input Conditions
 - For rise time and fall time specifications, see $\Delta t/\Delta V$ in the [Recommended Operating Conditions](#) table.
 - For specified High and low levels, see V_{IH} and V_{IL} in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend Output Conditions
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

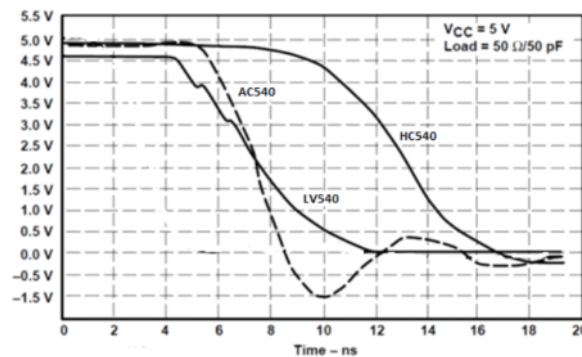


Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 9-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

9.4.2 Layout Example

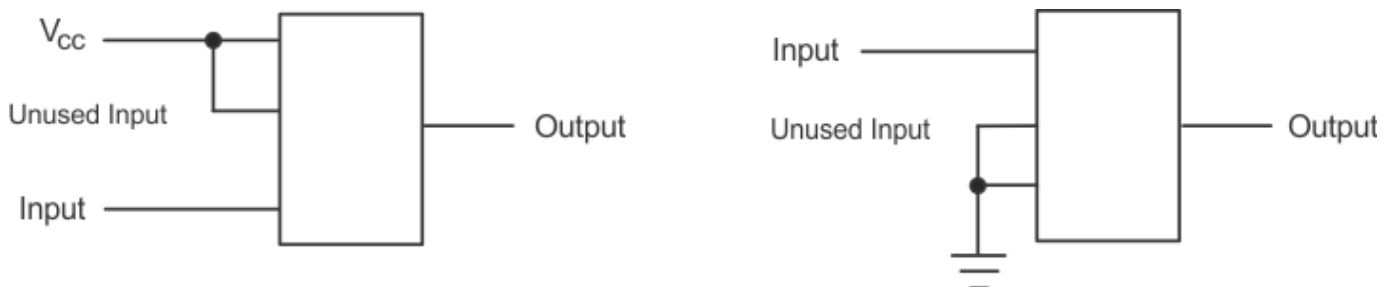


Figure 9-3. Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV540A	Click here	Click here	Click here	Click here	Click here

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV540ADBR	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ADBR.A	NRND	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ADGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ADGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV540A
SN74LV540ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ANSR	Last Time Buy	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV540A
SN74LV540ANSR.A	Last Time Buy	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV540A
SN74LV540APW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 125	LV540A
SN74LV540APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV540A
SN74LV540ARGYR	Last Time Buy	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV540A
SN74LV540ARGYR.A	Last Time Buy	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV540A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

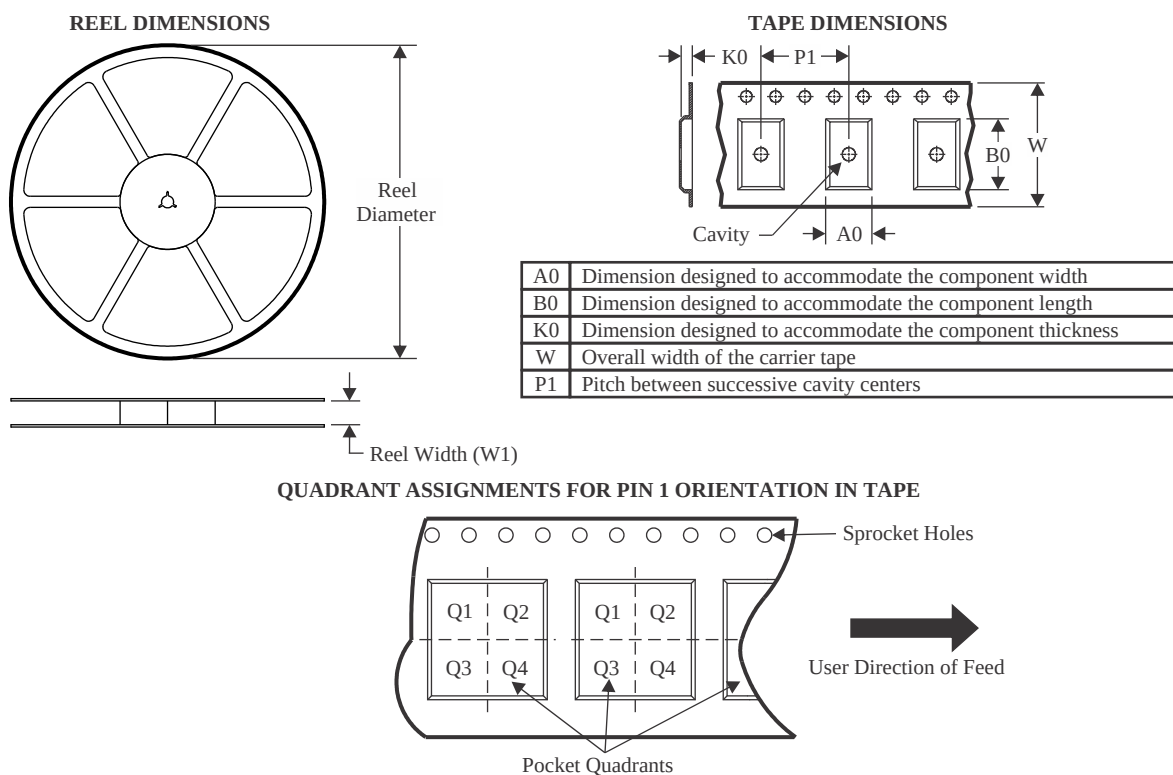
(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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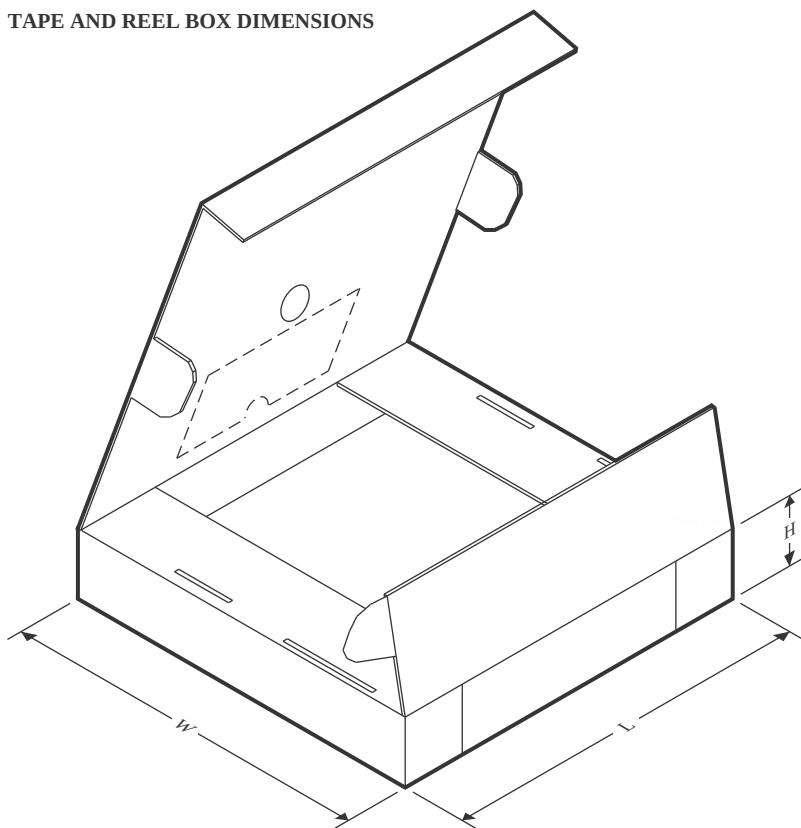
TAPE AND REEL INFORMATION



*All dimensions are nominal

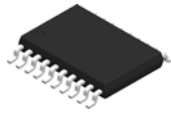
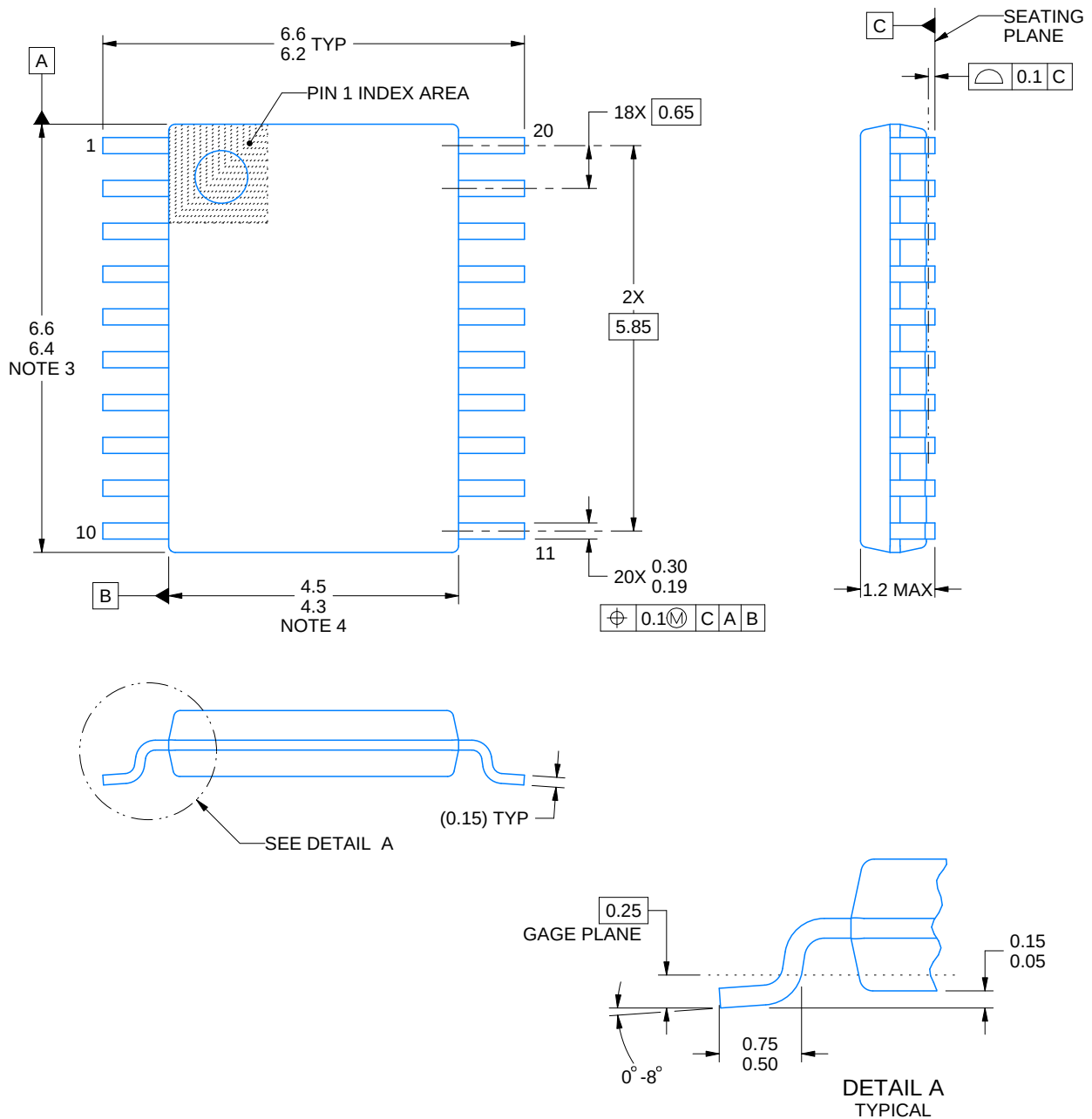
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV540ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV540ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV540ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV540ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV540APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV540ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV540ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV540ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LV540ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV540ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV540APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV540ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0



4220206/A 02/2017

NOTES:

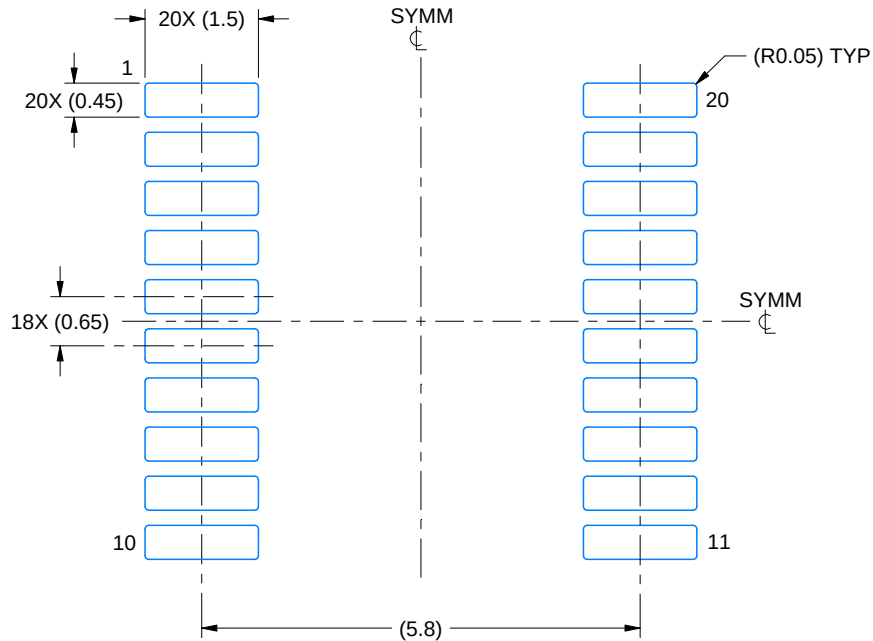
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

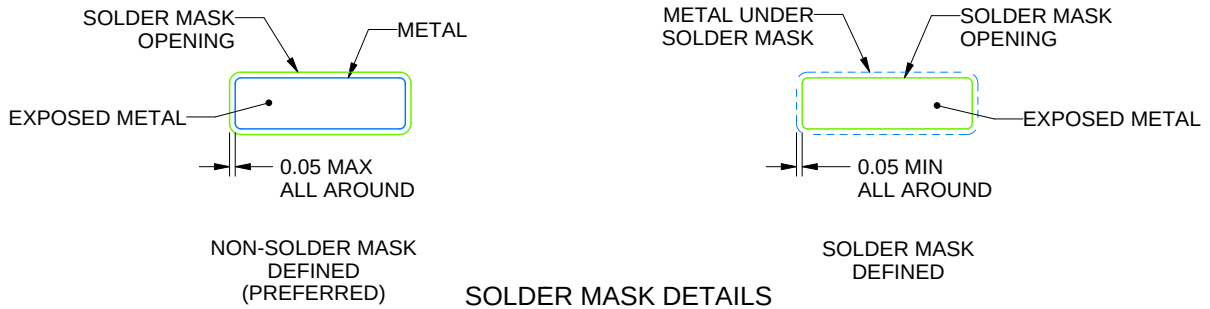
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

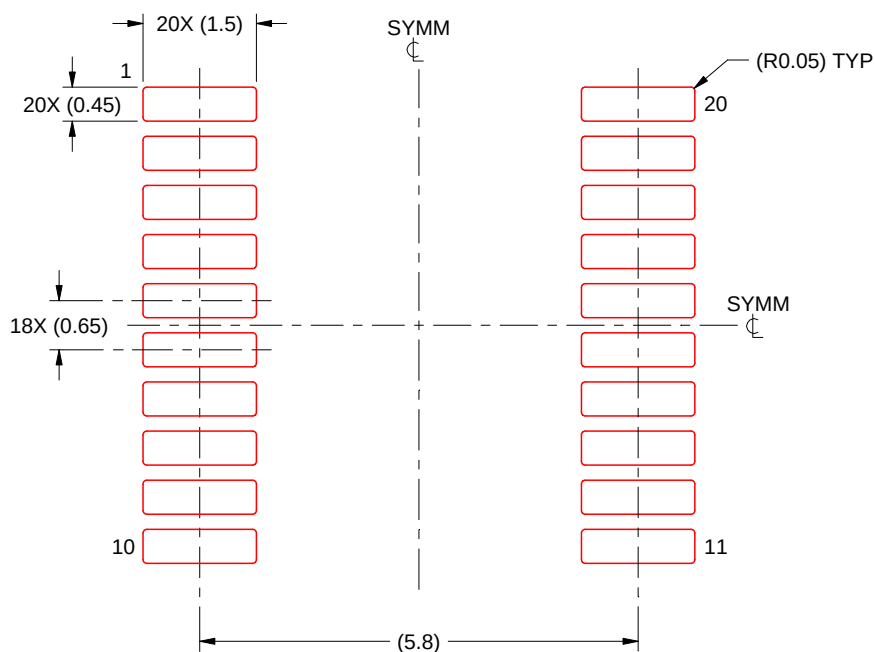
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

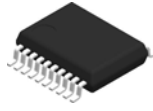
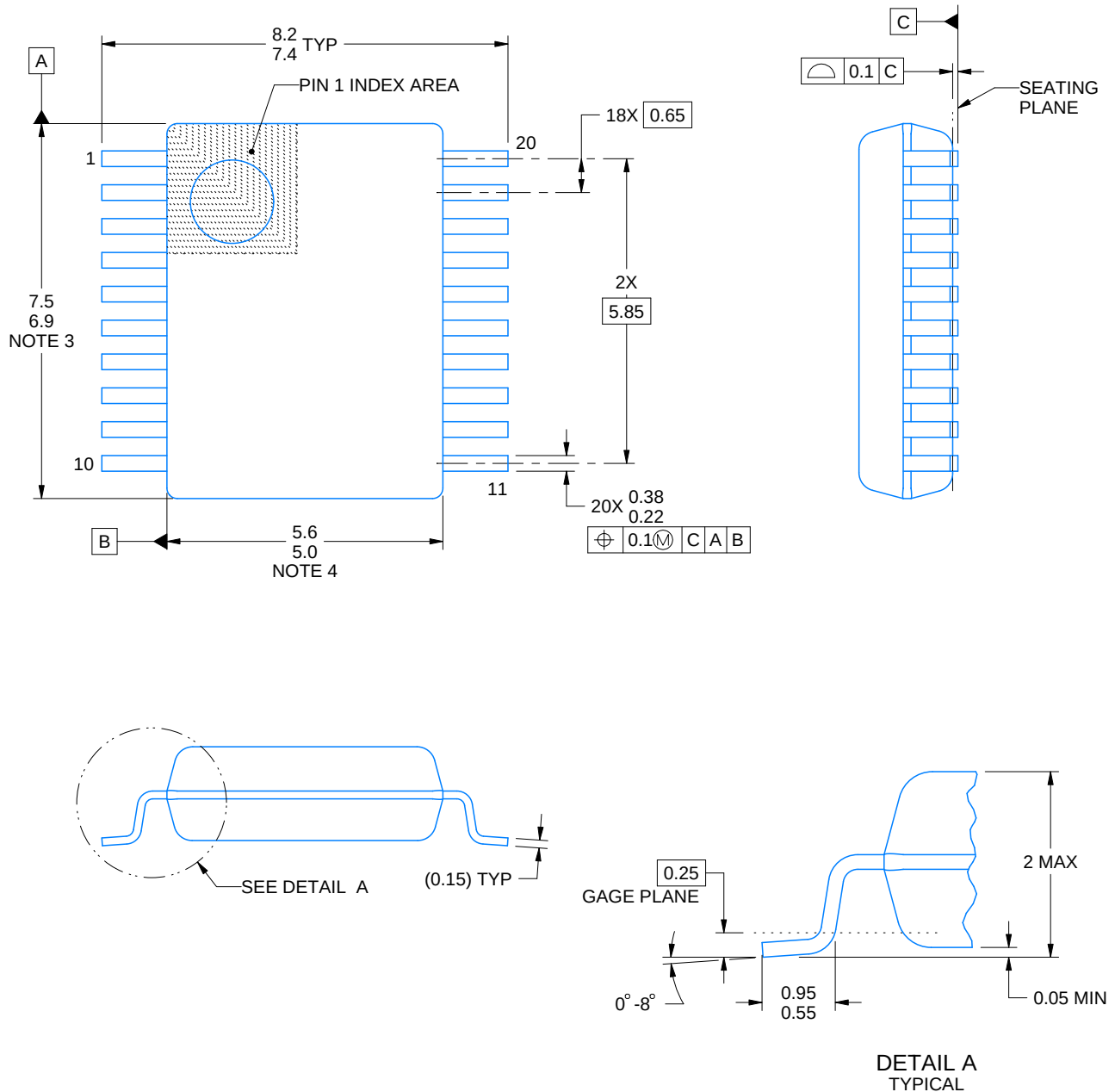


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

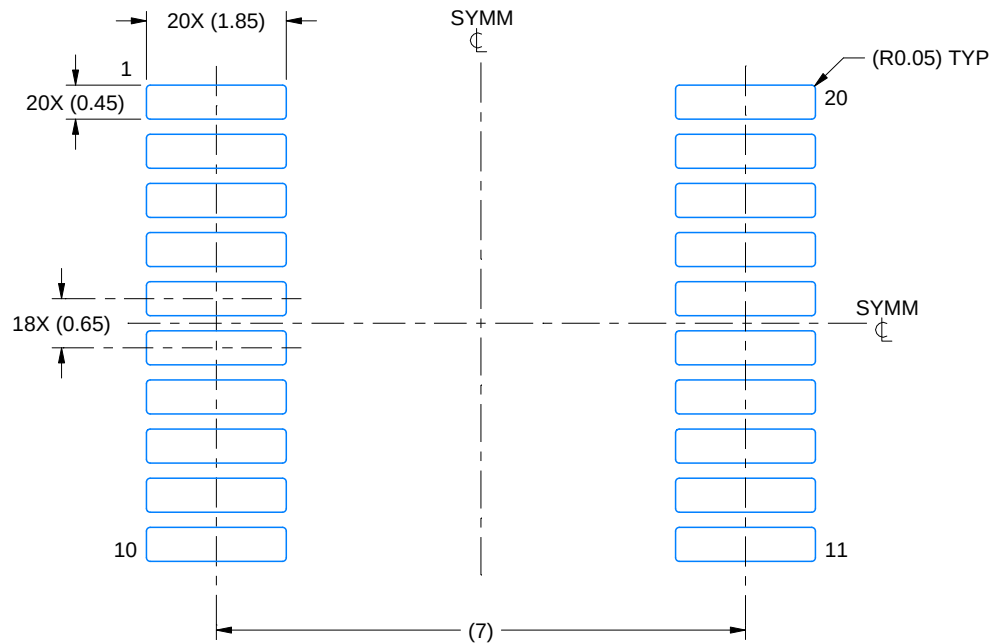
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

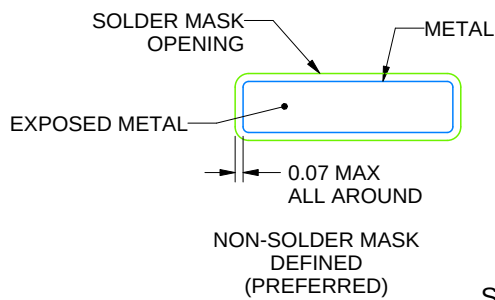
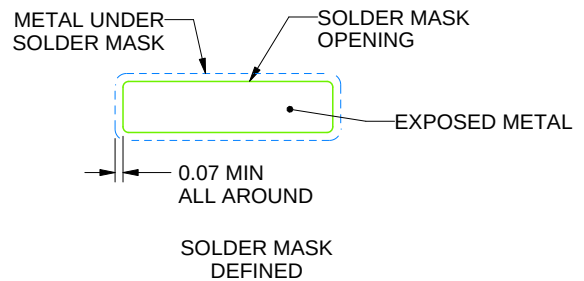
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

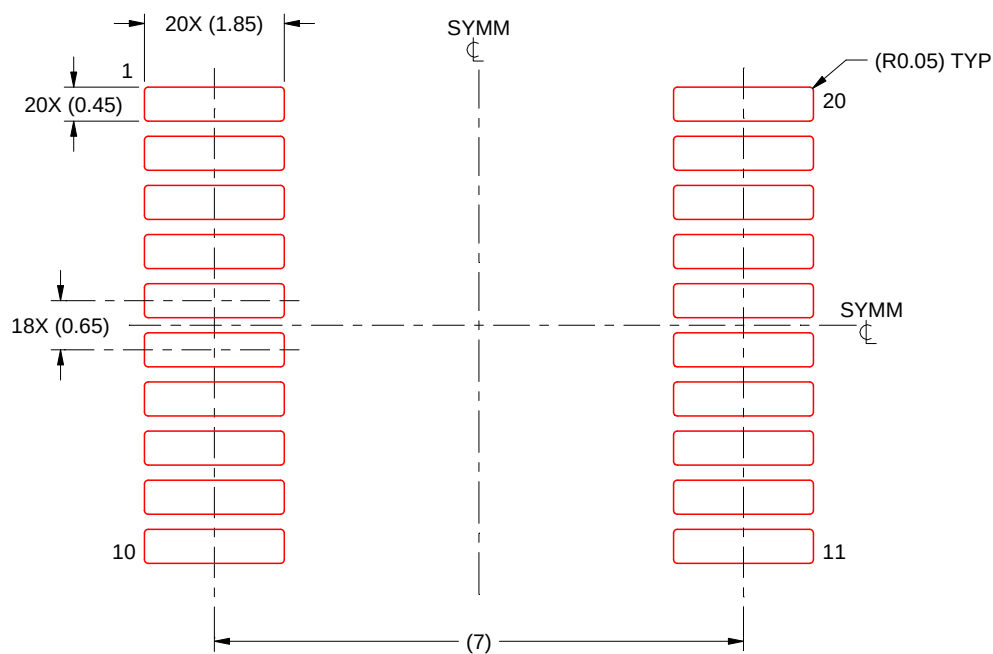
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

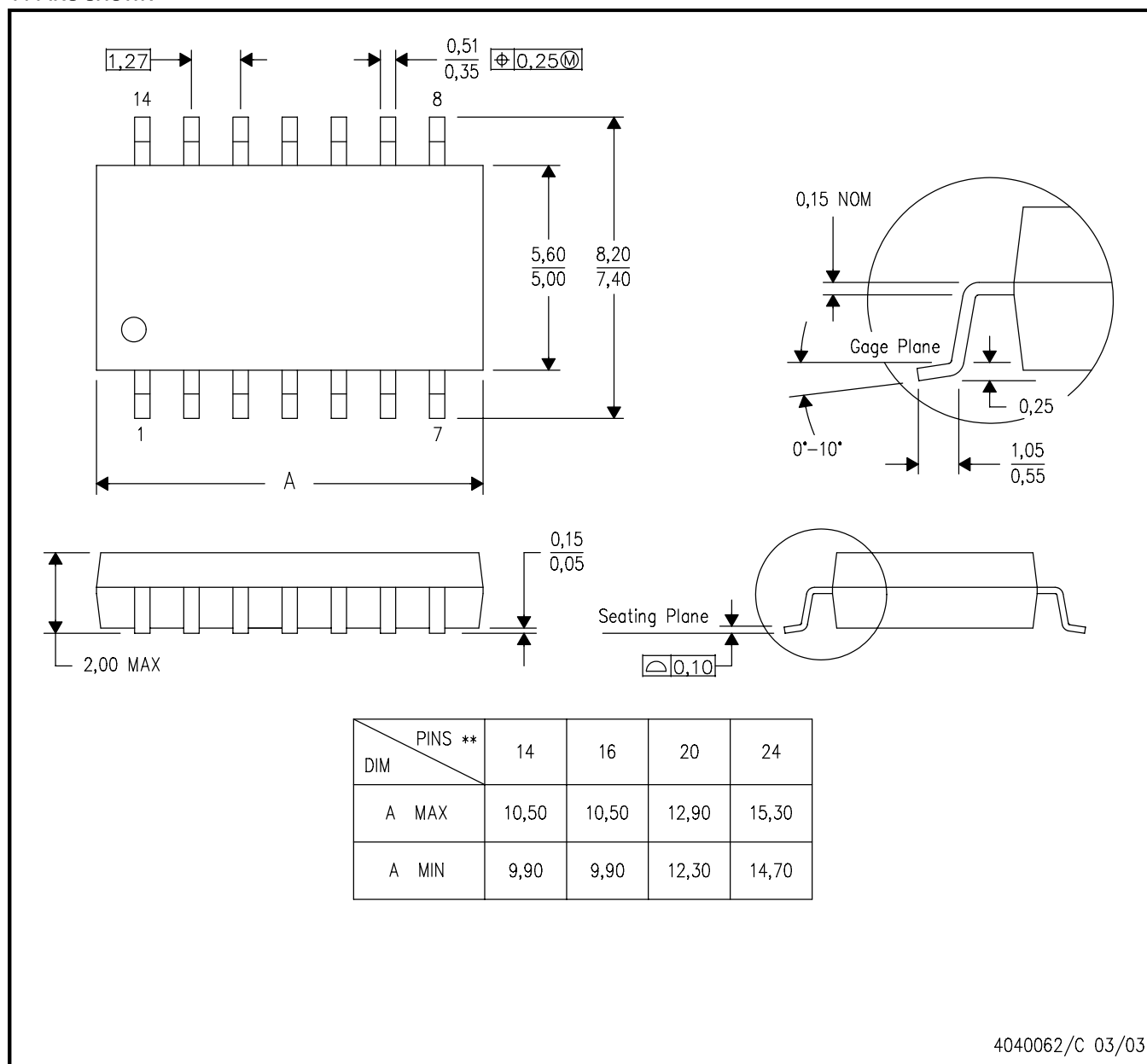
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

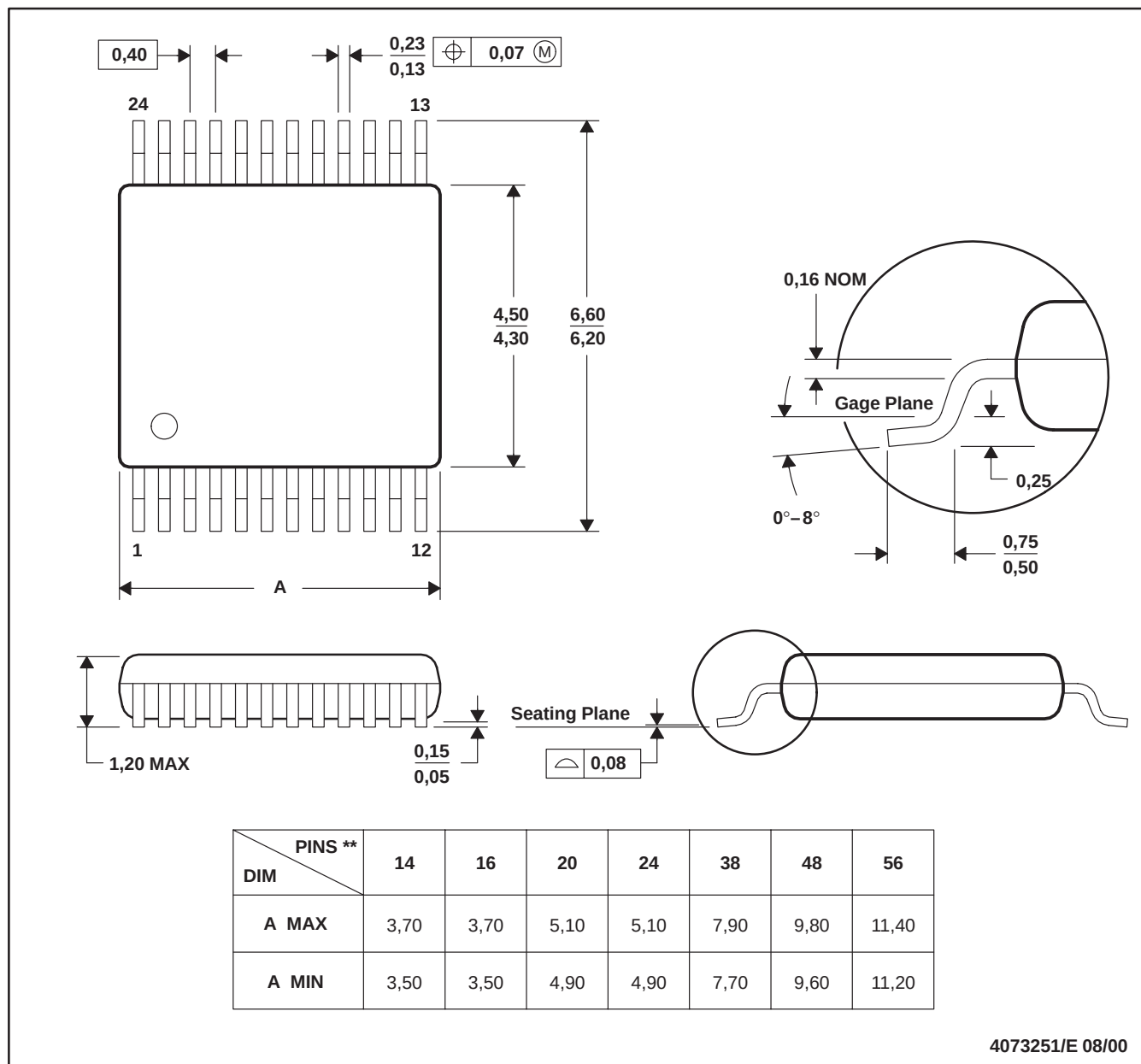


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

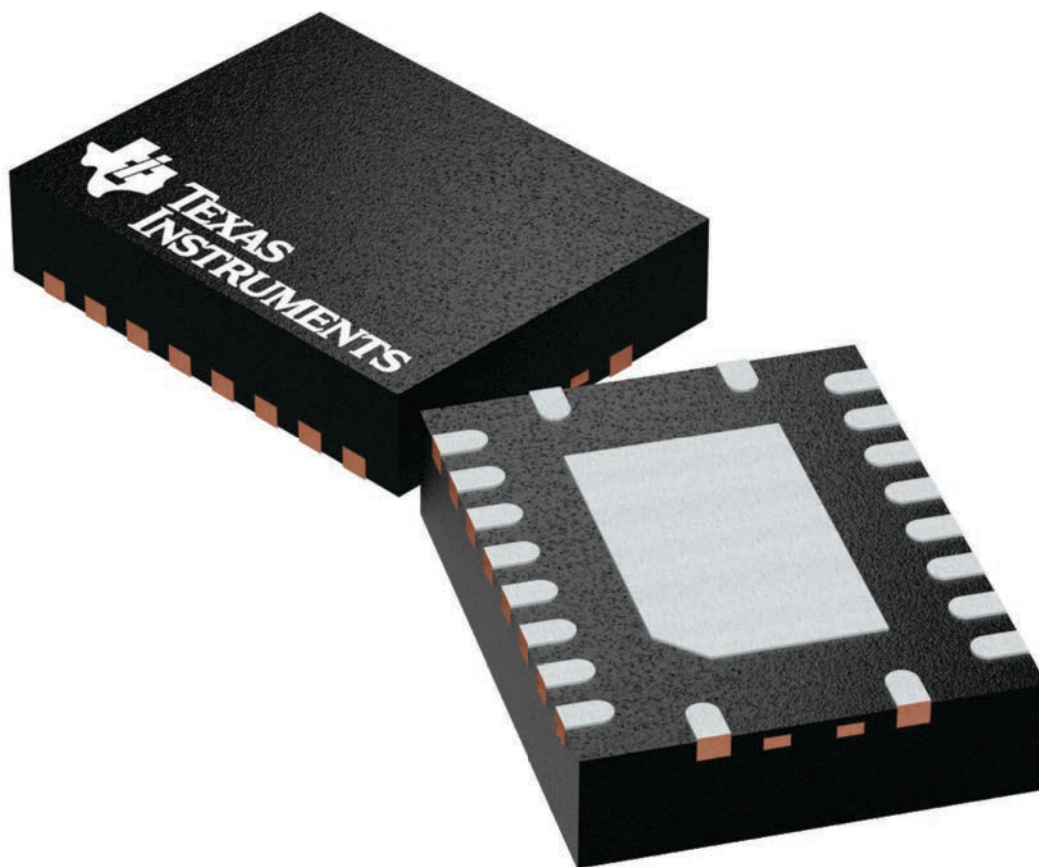
RGY 20

VQFN - 1 mm max height

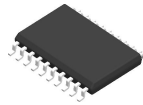
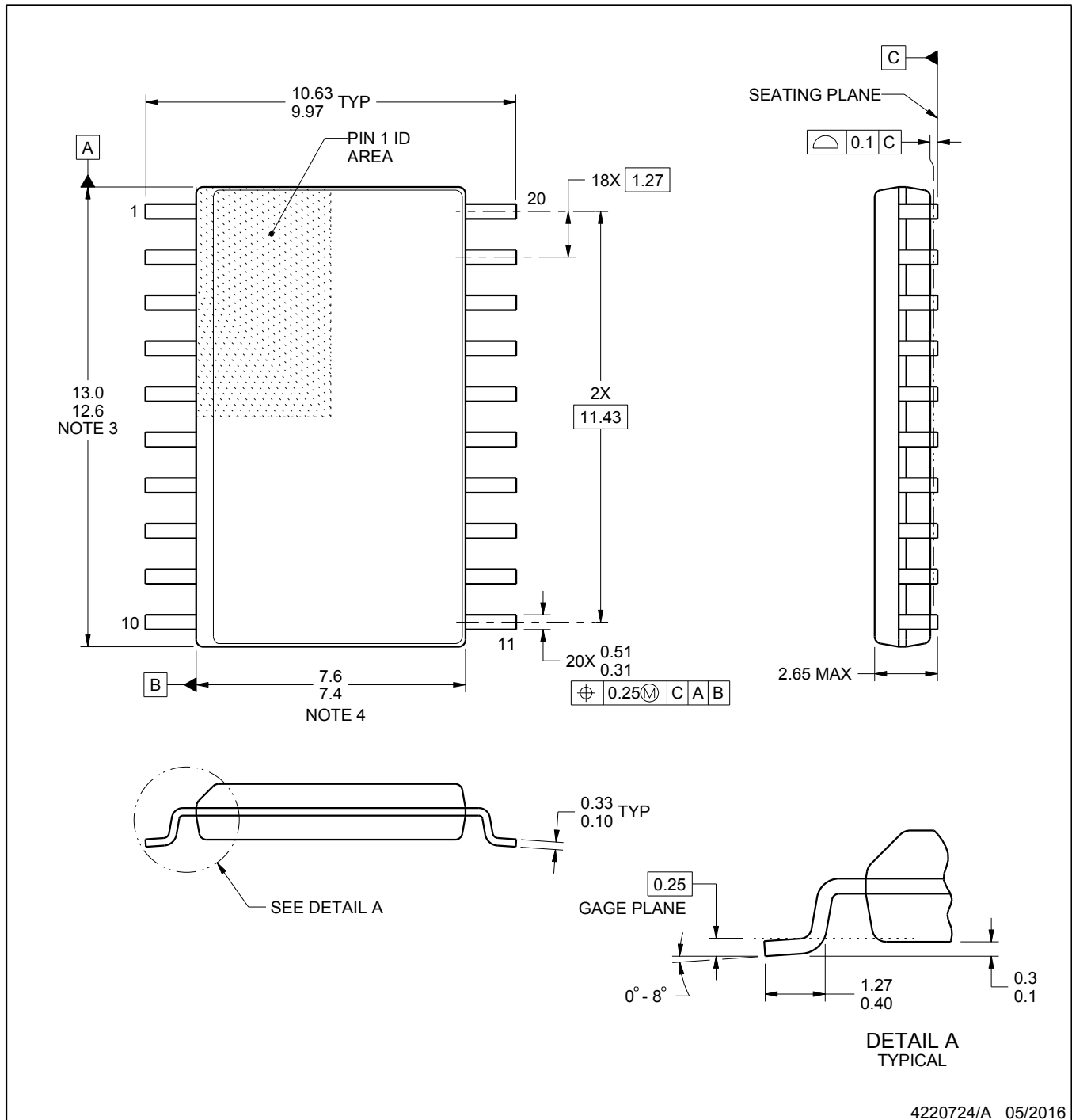
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4220724/A 05/2016

NOTES:

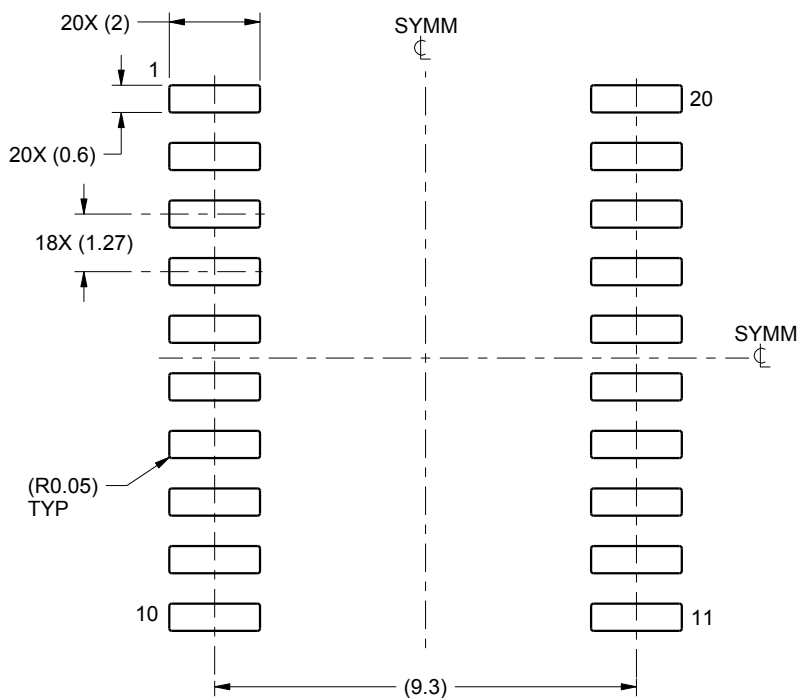
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

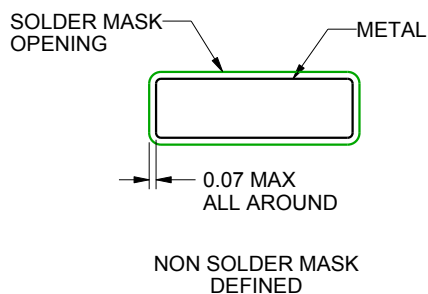
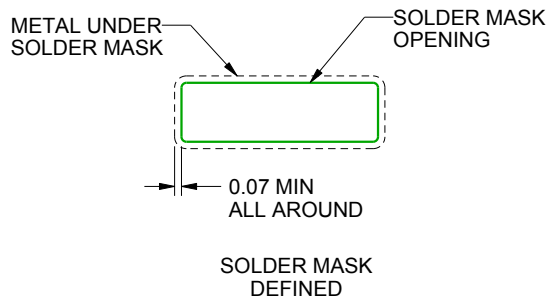
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

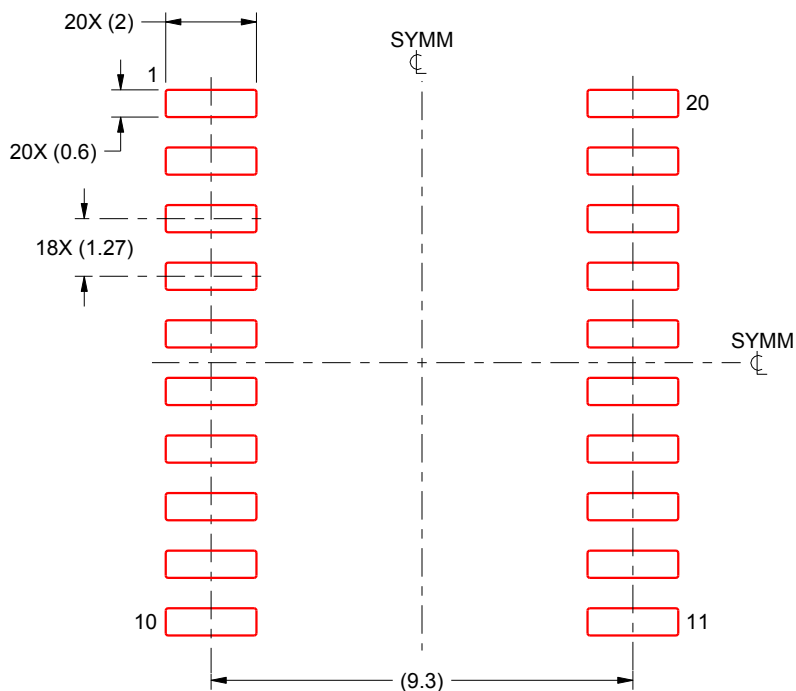
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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